MAX202 5-V Dual RS-232 Line Driver and Receiver With ±15-kV ESD Protection

1 Features

- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- ESD Protection for RS-232 Bus Pins: ±15-kV Human-Body Model
- Operates at 5-V V_{CC} Supply
- Operates Up to 120 kbit/s
- Two Drivers and Two Receivers
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Battery-Powered Systems
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

3 Description

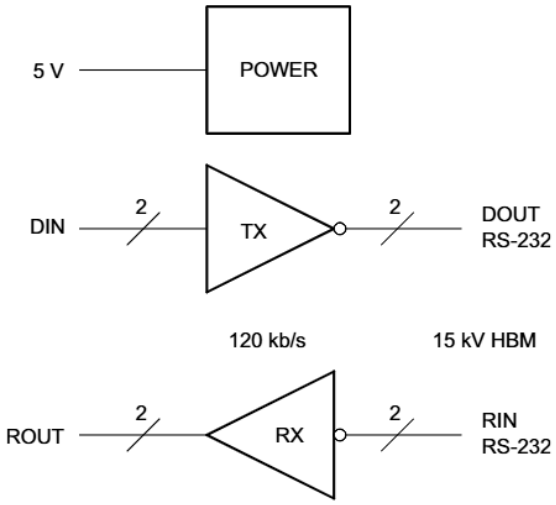
The MAX202 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The device operates at data signaling rates up to 120 kbit/s and a maximum of 30-V/µs driver output slew rate.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MAX202CD MAX202ID	SOIC (16)	9.90 mm × 3.91 mm
MAX202CDW MAX202IDW	SOIC WIDE (16)	10.30 mm × 7.50 mm
MAX202CPW MAX202IPW	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2007) to Revision F	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Removed the *Ordering Information* table; see POA at the end of the data sheet	1
• Changed values in the *Thermal Information* table to align with JEDEC standards	4

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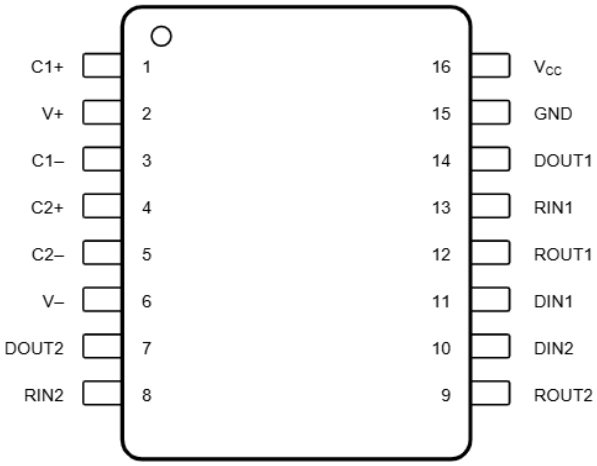
5 Pin Configuration and Functions

D, DW, or PW Package
16-Pin SOIC or TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	C1+	—	Positive lead of C1 capacitor
2	V+	O	Positive charge pump output for storage capacitor only
3	C1–	—	Negative lead of C1 capacitor
4	C2+	—	Positive lead of C2 capacitor
5	C2–	—	Negative lead of C2 capacitor
6	V–	O	Negative charge pump output for storage capacitor only
7	DOUT2	O	RS-232 line data output (to remote RS-232 system)
8	RIN2	I	RS-232 line data input (from remote RS-232 system)
9	ROUT2	O	Logic data output (to UART)
10	DIN2	I	Logic data input (from UART)
11	DIN1	I	Logic data input (from UART)
12	ROUT1	O	Logic data output (to UART)
13	RIN1	I	RS-232 line data input (from remote RS-232 system)
14	DOUT1	O	RS-232 line data output (to remote RS-232 system)
15	GND	—	Ground
16	V_{CC}	—	Supply voltage, connect to external 5-V power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)		–0.3	6	V
Positive charge pump voltage, V+(2)		V_{CC} – 0.3	14	V
Negative charge pump voltage, V–(2)		–14	0.3	V
Input voltage, V_I	Drivers	–0.3	V+ + 0.3	V
	Receivers		±30	
Output voltage, V_O	Drivers	V– – 0.3	V+ + 0.3	V
	Receivers	–0.3	V_{CC} + 0.3	
Short-circuit duration, D_{OUT}		Continuous		
Operating junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 7, 8, 13, and 14	±15000	V
			All other pins	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted(1); see Figure 10)

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage (D_{IN})		2			V
V_{IL}	Driver low-level input voltage (D_{IN})				0.8	V
V_I	Driver input voltage (D_{IN})		0		5.5	V
	Receiver input voltage		–30		30	
T_A	Operating free-air temperature	MAX202C	0		70	°C
		MAX202I	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ±0.5 V.

6.4 Thermal Information

THERMAL METRIC(1)		MAX202			UNIT
		D (SOIC)	DW (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.2	76.8	101	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	39.6	36.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.9	41.5	45.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.7	12.6	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.6	40.9	45.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see Figure 10)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 5 V		8	15	mA
DRIVER SECTION						
V_{OH}	High-level output voltage	D_{OUT} at R_L = 3 kΩ to GND, D_{IN} = GND	5	9		V
V_{OL}	Low-level output voltage	D_{OUT} at R_L = 3 kΩ to GND, D_{IN} = V_{CC}	–5	–9		V
I_{IH}	High-level input current	V_I = V_{CC}		0	200	µA
I_{IL}	Low-level input current	V_I at 0 V		0	–200	µA
I_{OS}(3)	Short-circuit output current	V_{CC} = 5.5 V, V_O = 0 V		±10	±60	mA
r_O	Output resistance	V_{CC}, V+, and V– = 0 V, V_O = ±2 V	300			Ω
RECEIVER SECTION						
V_{OH}	High-level output voltage	I_{OH} = –1 mA	3.5	V_{CC} – 0.4		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)		0.2	0.5	1	V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

6.6 Switching Characteristics

over recommended ranges of suply voltage and operating free-air temperature (unless otherwise noted; see Figure 10)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
DRIVER SECTION						
	Maximum data rate	C_L = 50 pF to 1000 pF, R_L = 3 kΩ to 7 kΩ one D_{OUT} switching, see Figure 6	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	C_L = 2500 pF, R_L = 3 kΩ, all drivers loaded, see Figure 6		2		µs
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	C_L = 2500 pF, R_L = 3 kΩ, all drivers loaded, see Figure 6		2		µs
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 to 2500 pF, R_L = 3 kΩ to 7 kΩ, see Figure 7		300		ns
SR(tr)	Slew rate, transition region	C_L = 50 to 1000 pF, R_L = 3 kΩ to 7 kΩ, V_{CC} = 5 V, see Figure 6	3	6	30	V/µs
RECEIVER SECTION (SEE Figure 8)						
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	C_L = 150 pF		0.5	10	µs
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	C_L = 150 pF		0.5	10	µs
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF		300		ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

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6.7 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

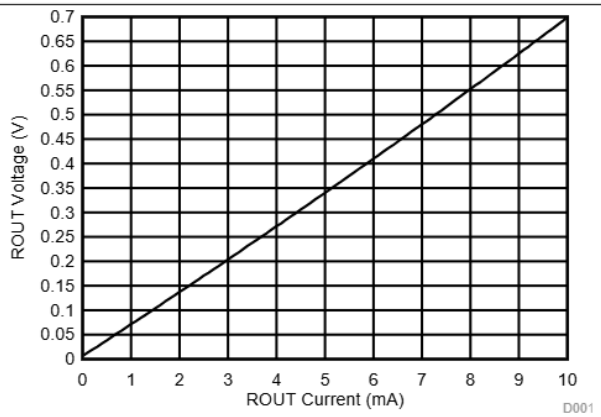

Figure 1. Receiver VOL vs Output Current

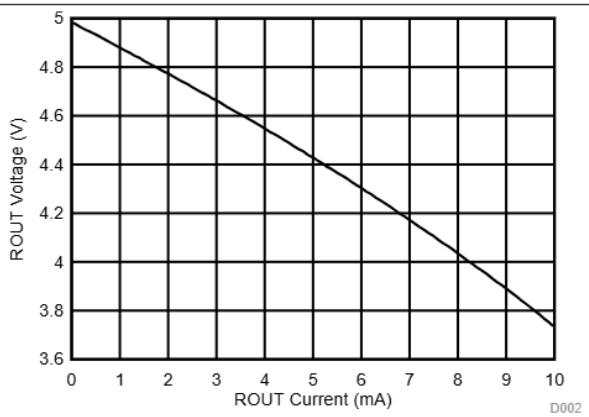

Figure 2. Receiver VOH vs Output Current

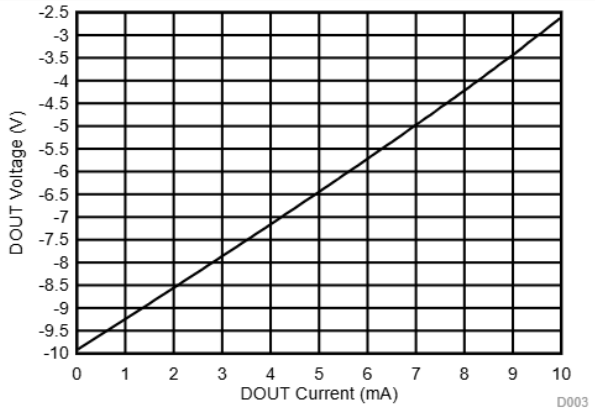

Figure 3. Driver VOL vs Output Current

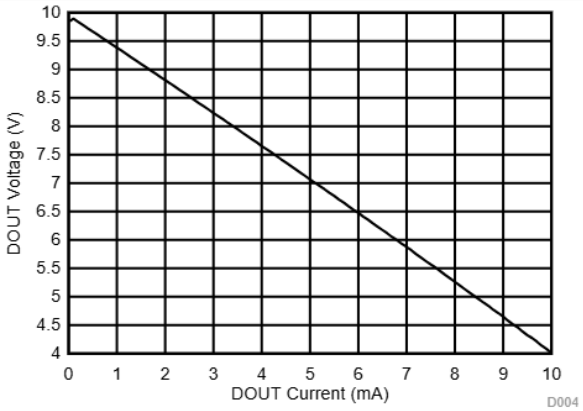

Figure 4. Driver VOH vs Output Current

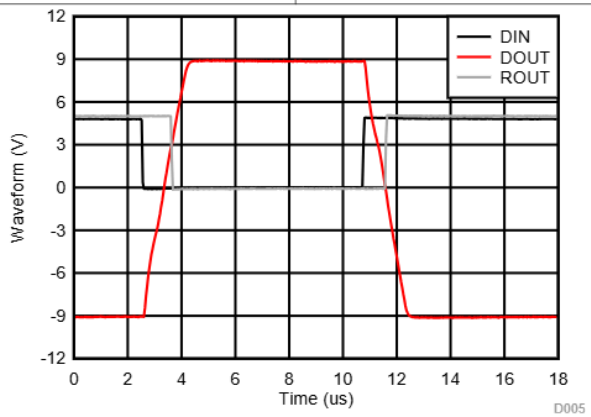

Figure 5. Driver and Receiver Loopback Waveforms

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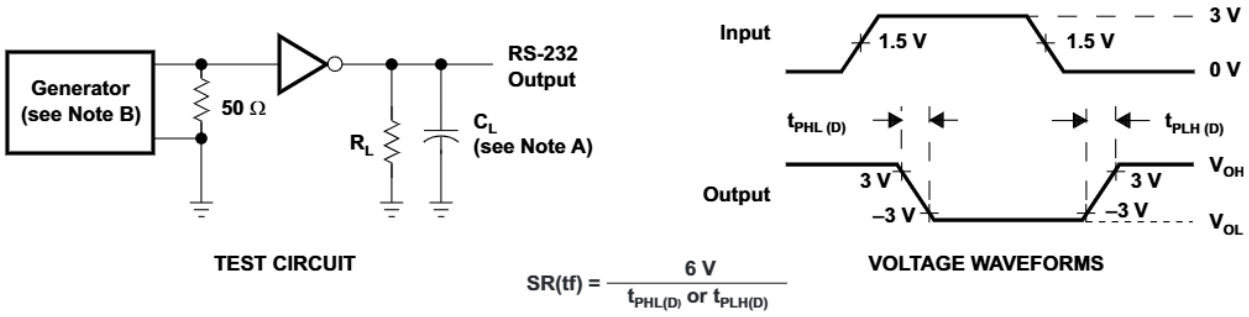
7 Parameter Measurement Information

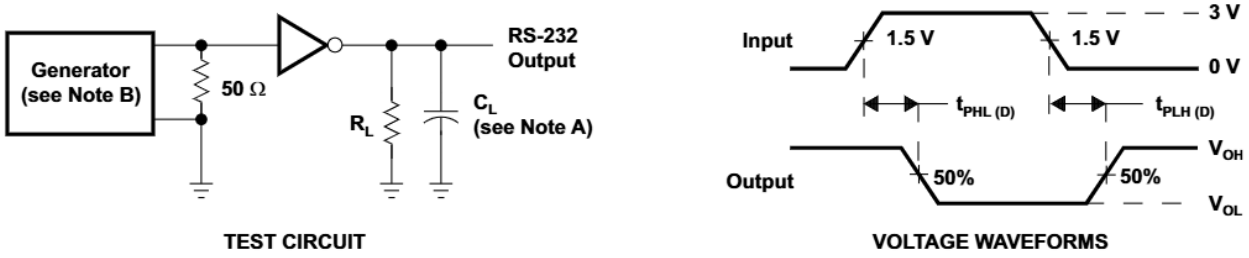


$$SR(tf) = \frac{6\ V}{t_{PHL(D)} \text{ or } t_{PLH(D)}}$$

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

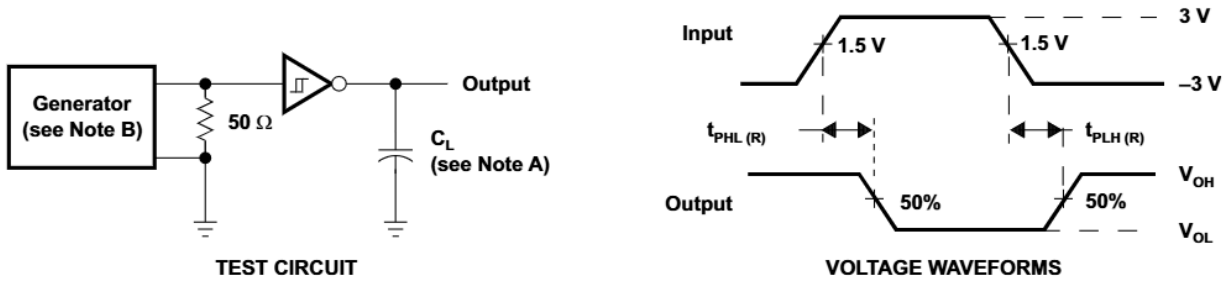
Figure 6. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 7. Driver Pulse Skew



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 8. Receiver Propagation Delay Times

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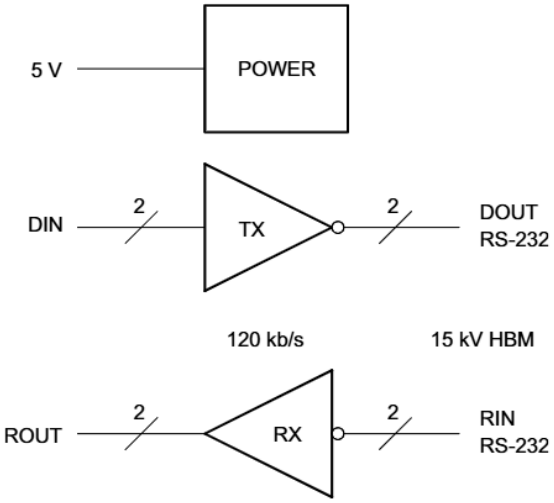
8 Detailed Description

8.1 Overview

The MAX202 device is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to ±30-V inputs and decode inputs as low as ±3 V. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Power

The power block increases and inverts the 5-V supply for the RS-232 driver using a charge pump that requires four 0.1-µF external capacitors.

8.3.2 RS-232 Driver

Two drivers interface standard logic levels to RS-232 levels. The driver inputs do not have internal pullup resistors. Do not float the driver inputs.

8.3.3 RS-232 Receiver

Two Schmitt trigger receivers interface RS-232 levels to standard logic levels. Each receiver has an internal 5-kΩ load to ground. An open input results in a high output on ROUT.

8.4 Device Functional Modes

8.4.1 V_{CC} Powered by 5-V

The device is in normal operation when powered by 5 V.

8.4.2 V_{CC} Unpowered

When MAX202 is unpowered, it can be safely connected to an active remote RS-232 device.

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Device Functional Modes (continued)

8.4.3 Truth Tables

Table 1 and Table 2 list the function for each driver and receiver (respectively).

Table 1. Function Table for Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Table 2. Function Table for Each Receiver(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

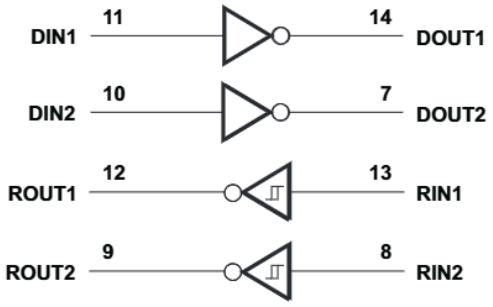


Figure 9. Logic Diagram (Positive Logic)

9 Application and Implementation

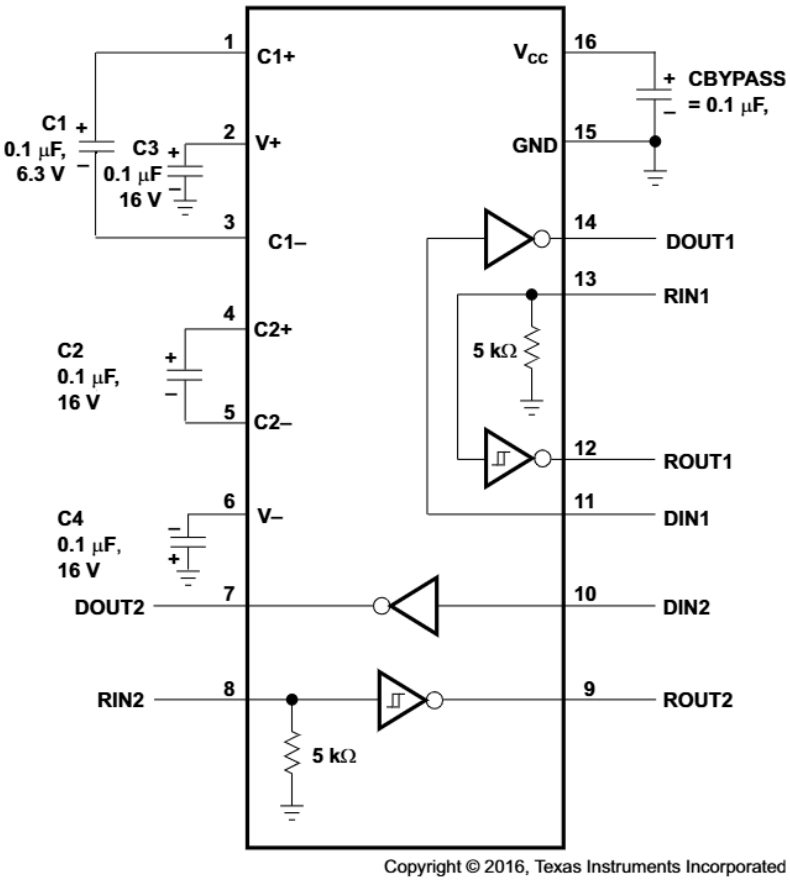
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

For proper operation, add capacitors as shown in Figure 10. Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

9.2 Typical Application



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A. C3 can be connected to V_{CC} or GND.

B. Resistor values shown are nominal.

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

Figure 10. Typical Operating Circuit and Capacitor Values

9.2.1 Design Requirements

- V_{CC} minimum is 4.5 V and maximum is 5.5 V.
- Maximum recommended bit rate is 120 kbps.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Capacitor Selection

The capacitor type used for C1 through C4 is not critical for proper operation. The MAX202 requires 0.1-µF capacitors. Capacitors up to 10 µF can be used without harm. Ceramic dielectrics are suggested for the 0.1-µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10 µF) to reduce the output impedance at V+ and V–.

Bypass V_{CC} to ground with at least 0.1 µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

9.2.2.2 ESD Protection

MAX202 devices have standard ESD protection structures incorporated on all pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV when powered down.

9.2.2.3 ESD Test Conditions

Stringent ESD testing is performed by TI based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

9.2.2.4 Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 11. Figure 12 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the device under test (DUT) through a 1.5-kΩ resistor.

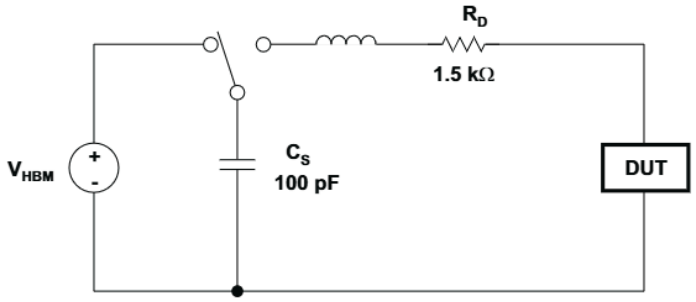


Figure 11. HBM ESD Test Circuit

Typical Application (continued)

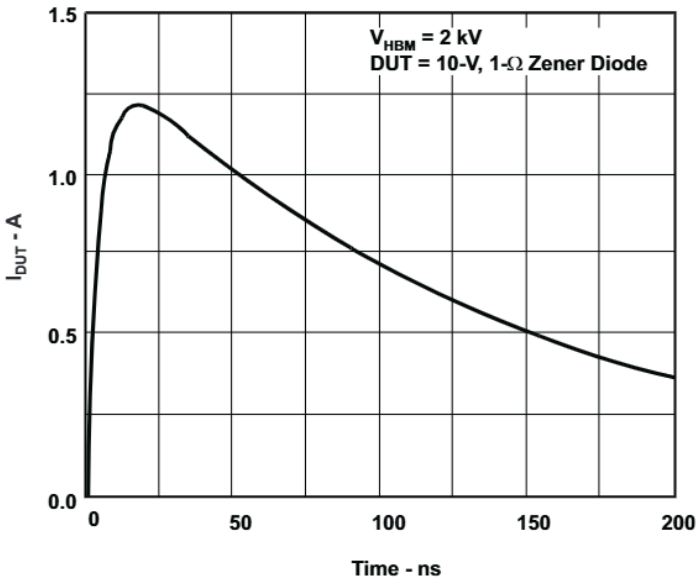
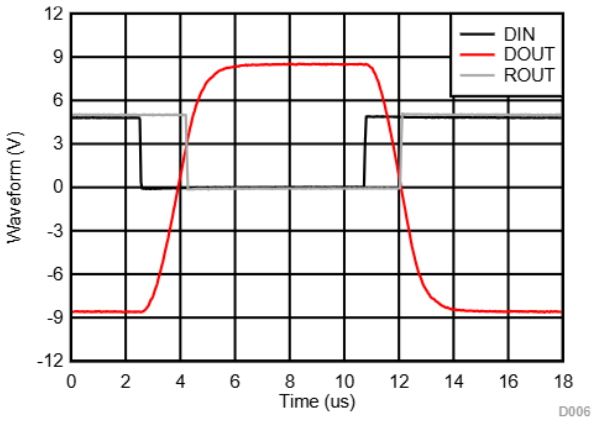


Figure 12. Typical HBM Current Waveform

9.2.3 Application Curve



120 kbit/s, 1-nF load

Figure 13. Driver and Receiver Loopback Signal

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10 Power Supply Recommendations

The V_{CC} voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} must be between 4.5 V and 5.5 V.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. For best ESD performance, make the impedance from MAX202 ground pin to the ground plane of the circuit board as low as possible. Use wide metal and multiple vias on both sides of ground pin.

11.2 Layout Example

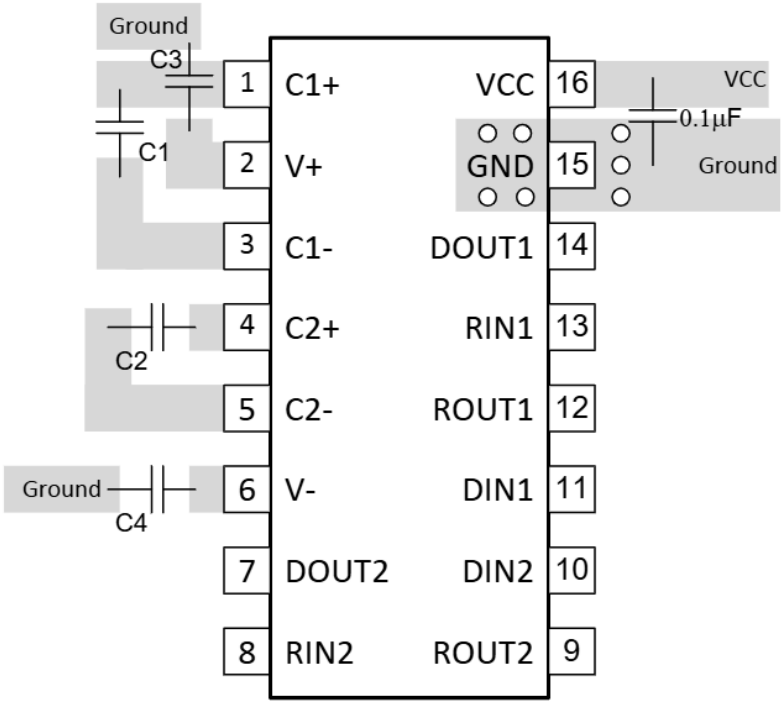

Figure 14. MAX202 Circuit Board Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX202CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX202C	Samples
MAX202CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX202C	Samples
MAX202CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX202C	Samples
MAX202CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX202C	Samples
MAX202CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX202C	Samples
MAX202CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA202C	Samples
MAX202CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA202C	Samples
MAX202ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB202I	Samples
MAX202IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB202I	Samples
MAX202IPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB202I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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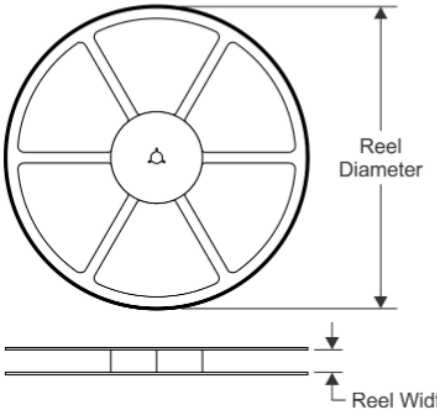
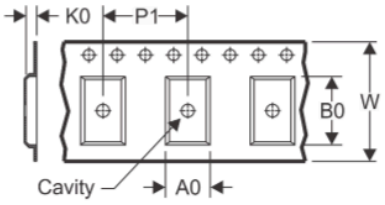
TAPE AND REEL INFORMATION

REEL DIMENSIONS

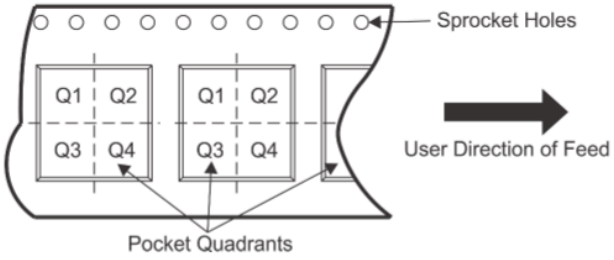


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

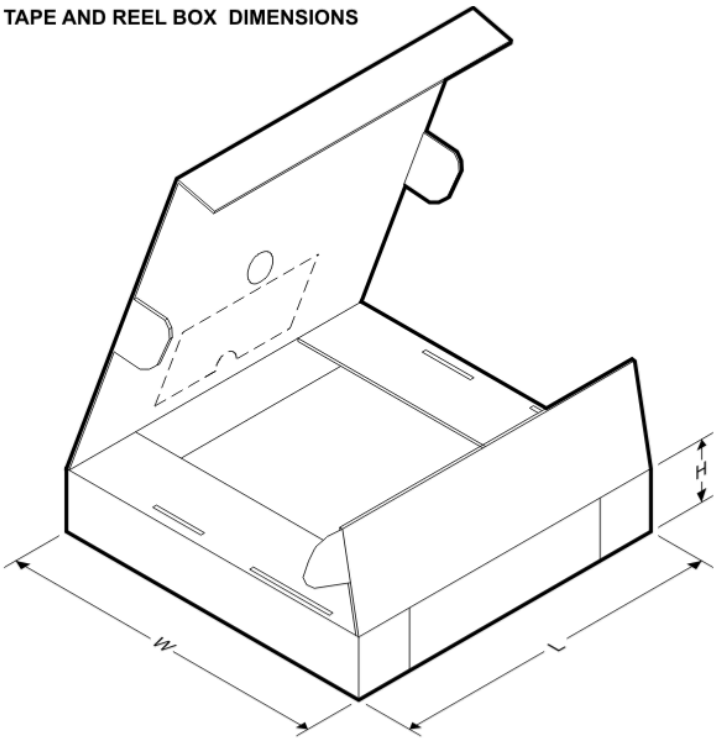
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX202CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX202CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX202CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX202IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX202IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX202IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

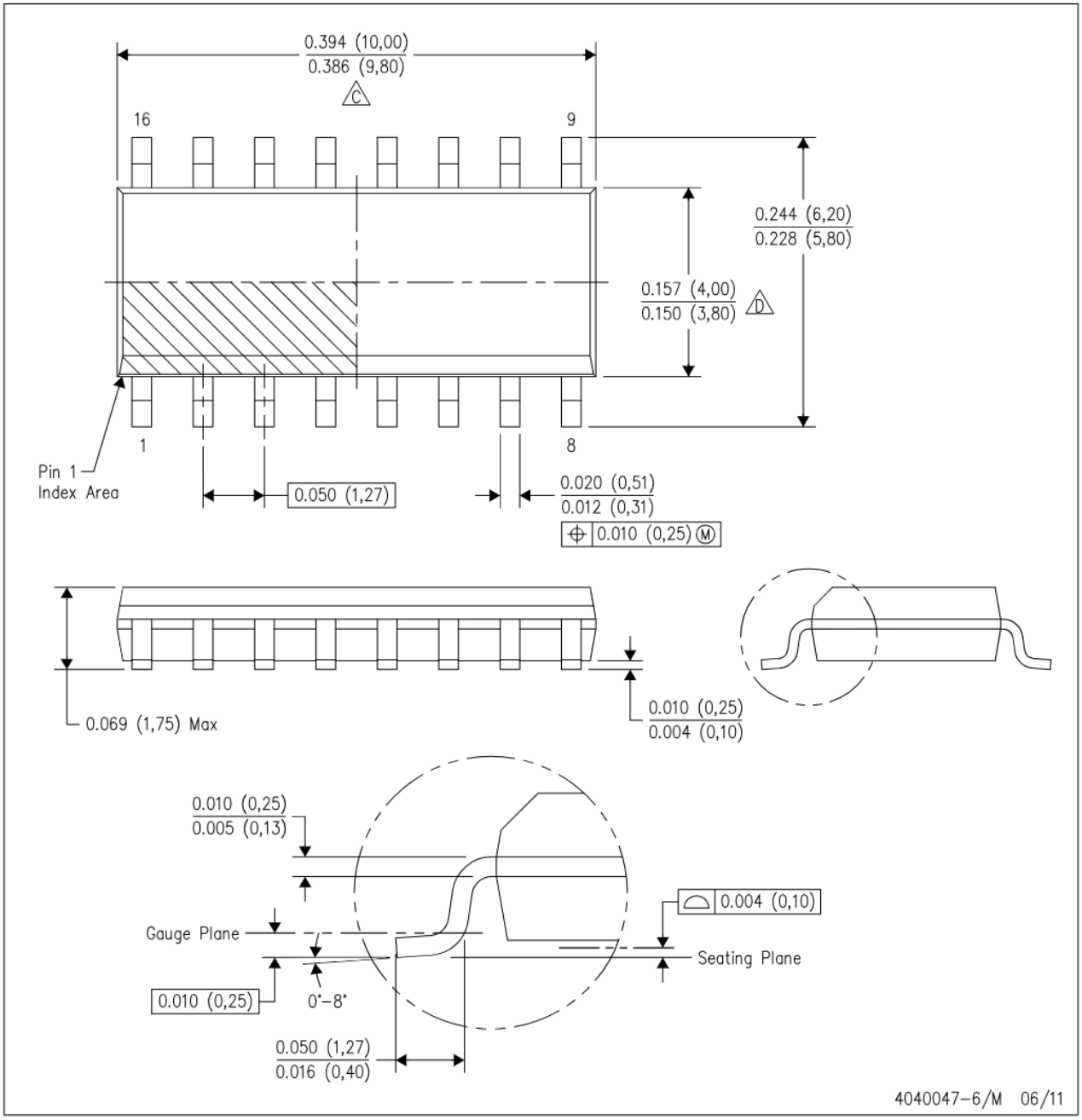
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

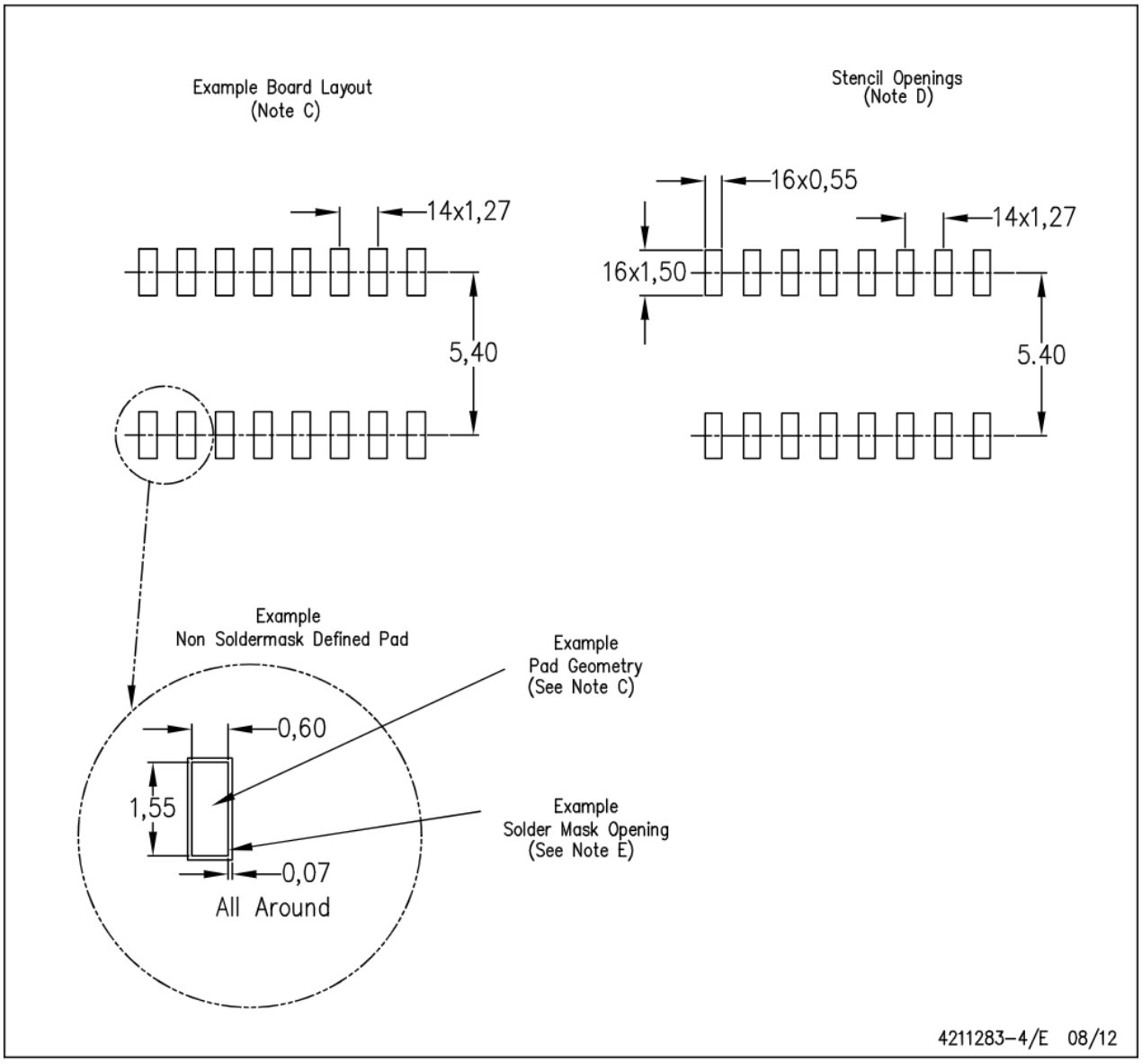
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX202CDR	SOIC	D	16	2500	333.2	345.9	28.6
MAX202CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX202CPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX202IDR	SOIC	D	16	2500	333.2	345.9	28.6
MAX202IDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX202IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



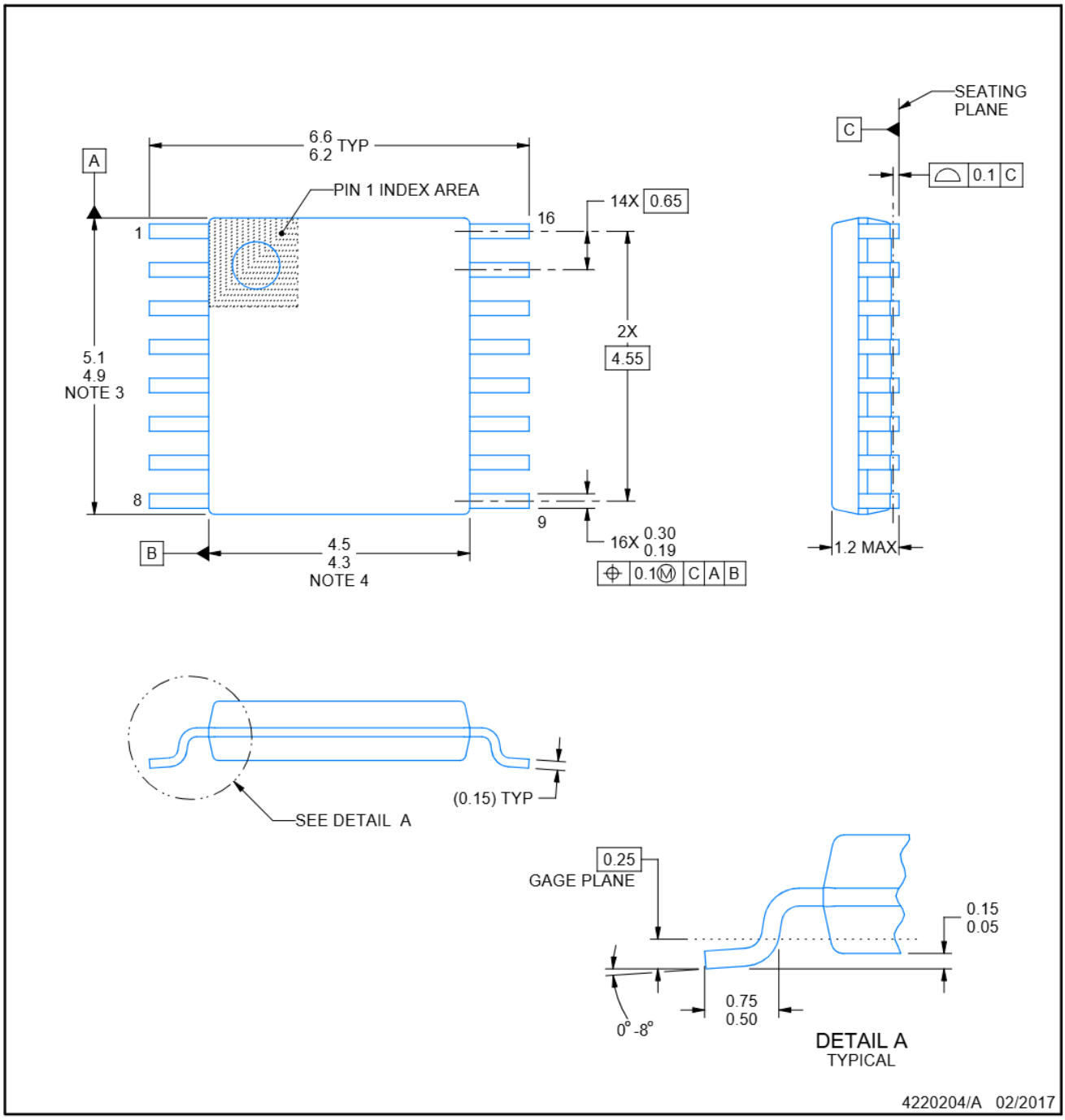
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

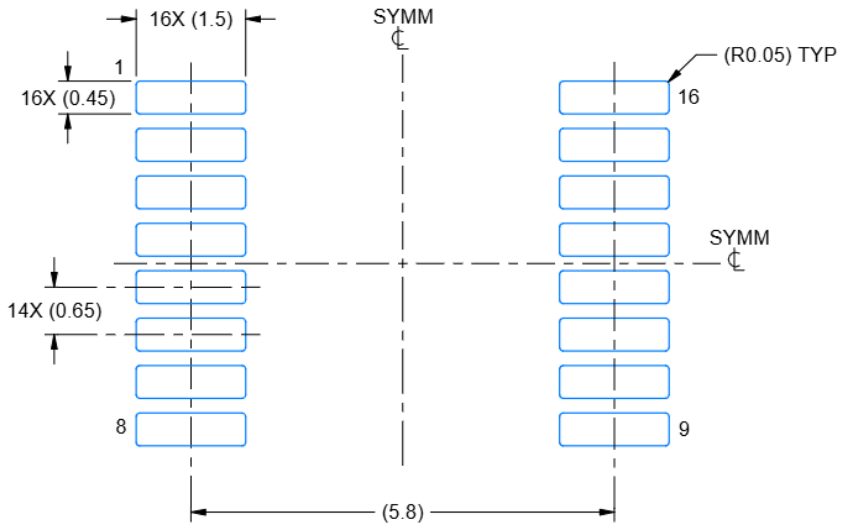
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

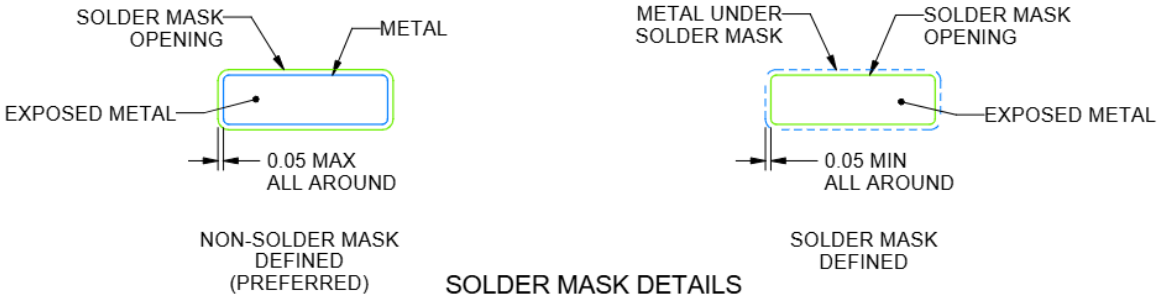


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

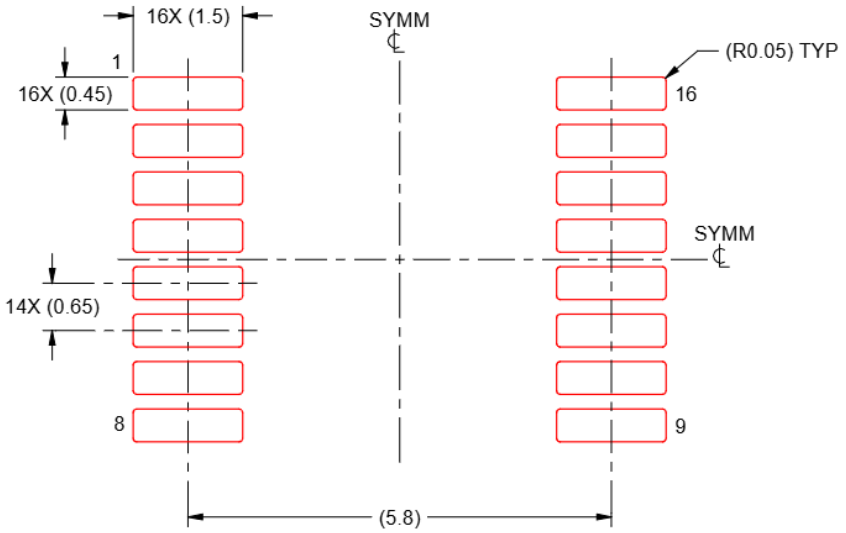


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

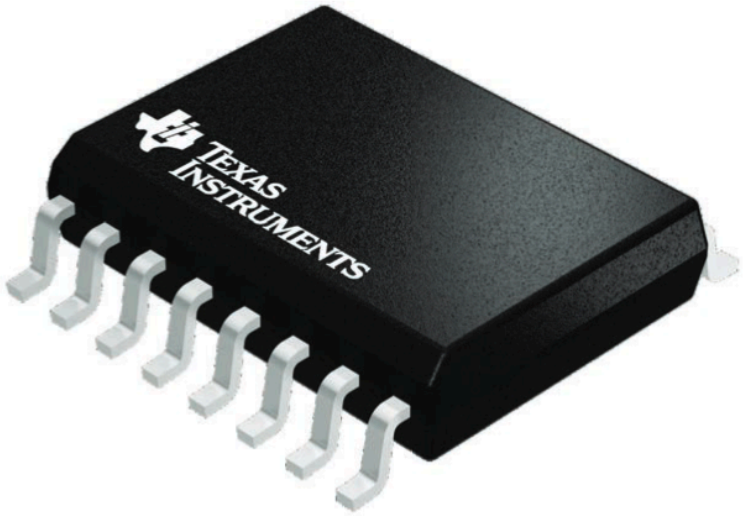
DW 16

SOIC - 2.65 mm max height

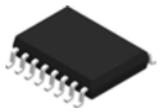
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

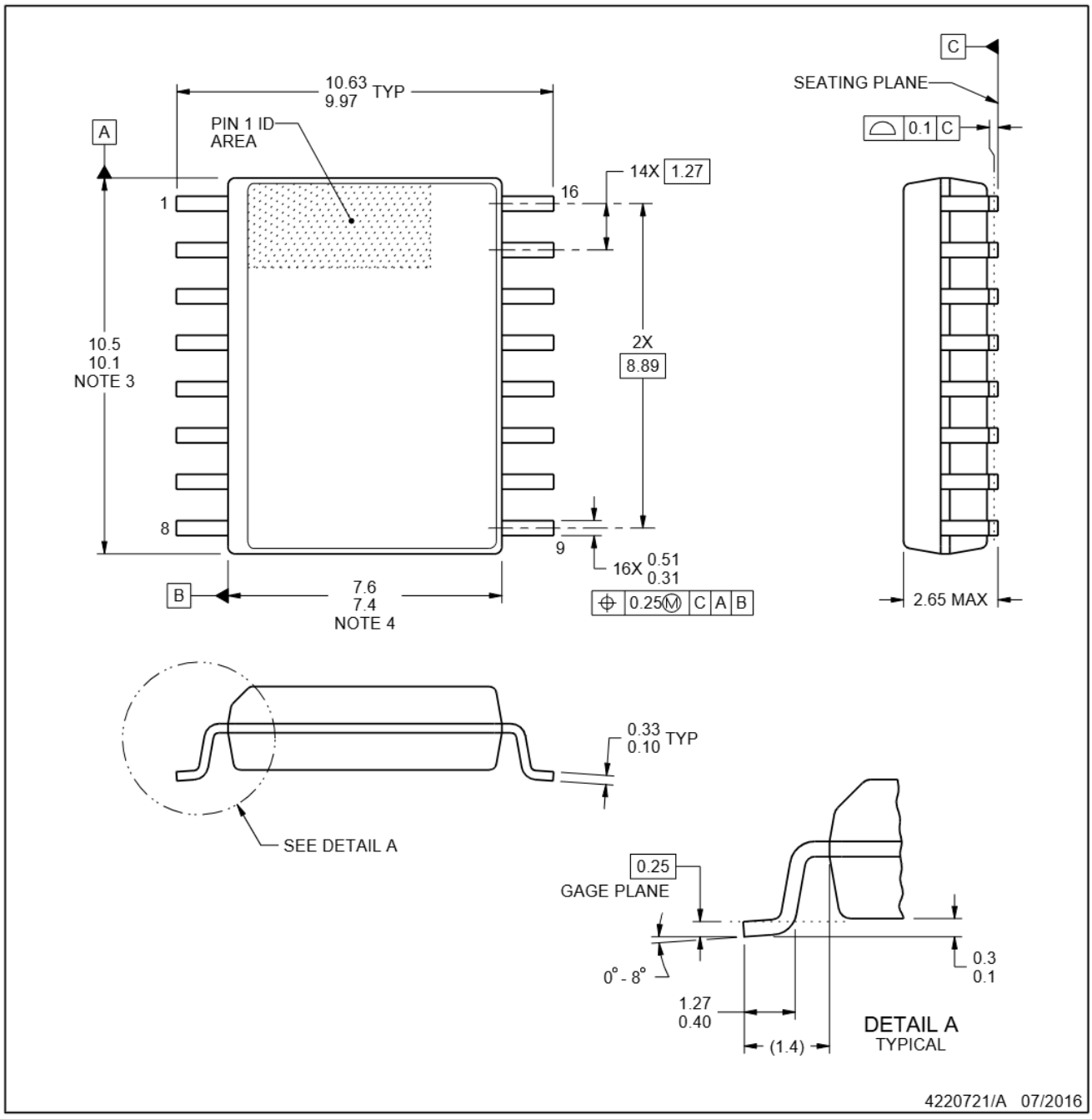


PACKAGE OUTLINE

DW0016A

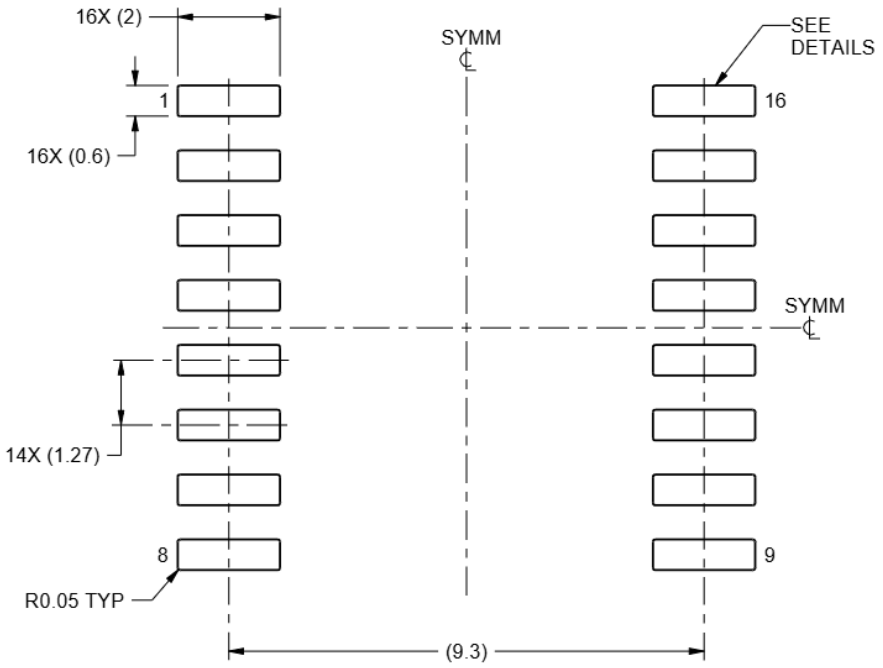
SOIC - 2.65 mm max height

SOIC

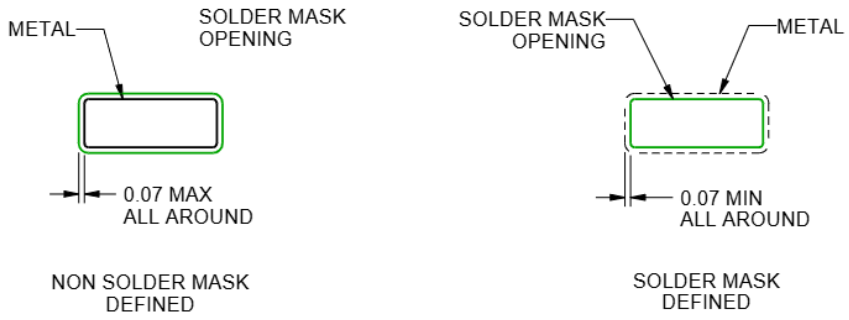


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

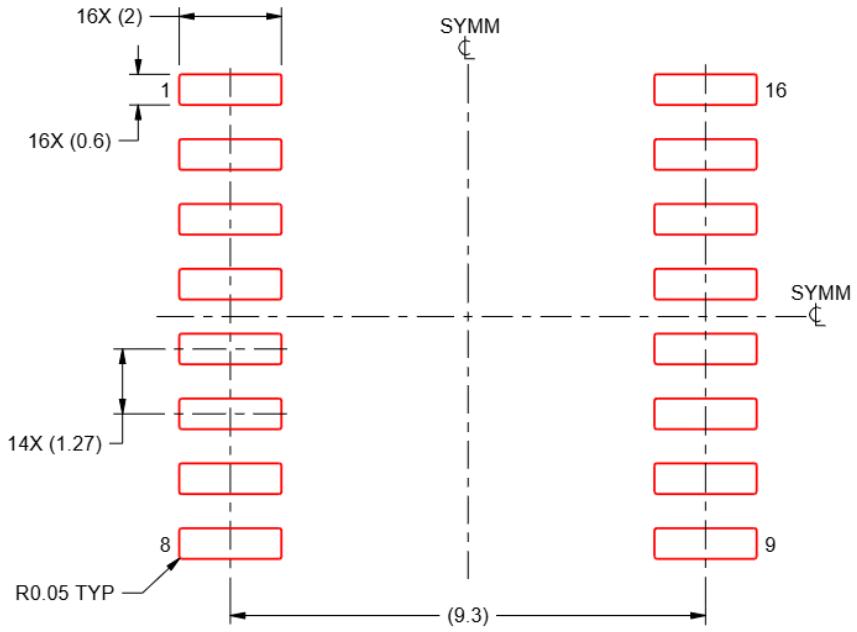


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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