上海冠显光电科技有限公司
Shanghai Top Display Optoelectronics Co., LTD

X6B1 Model
Datasheet

SHTDO

Revision 1.4
Feb.17,2025

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Revision History

Revision	Date	Description
1.0	Mar.31.2023	Initial Release Version.
1.1	Apr.28.2023	Modified some PINs
1.2	May.26.2023	Modified some PINs and footprint
1.3	Dec.25.2023	Modified some PINs of multifunction and Audio reference circuit
1.4	Feb.17.2025	Modified the structure and footprint of PCB

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1. Overview

1. High performance and low cost.
2. Short time to make an HMI product: PC software (“GIRAFFE”) to design UI and Communication.
3. Based on the RISC-V CPU architecture.
4. 24/18/16bit RGB/Dual LVDS/MIPI Interface, 16.7M/262K/65K colors, LCD’s resolution support to 1920x1080.
5. Supports 720P video playback, including H.264, H.263, MPEG1/2/4 decoder.
6. Integrated audio codec provides end users with a good audio experience.
7. 1 USB OTG.
8. Up to 7 UARTs, Baud rate up to 115200bps.
9. 1 IIC.
10. 2 CAN.
11. Up to 5 ADC of 12bit.
12. 1 DVP camera / 100M Ethernet/ WIFI + Bluetooth.
13. Support Resistive touch panel, Capacitive touch panel.
14. 1 Buzzer.
15. 1 Speaker.
16. 60M Bytes ROM inside for user to save UI and lager ROM is optional.

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2 Description

2.1 CPU Architecture

The X6B1 Model is based on RISC-V CPU architecture.

2.2 Memory Subsystem

This section consists of internal memory and external memory:

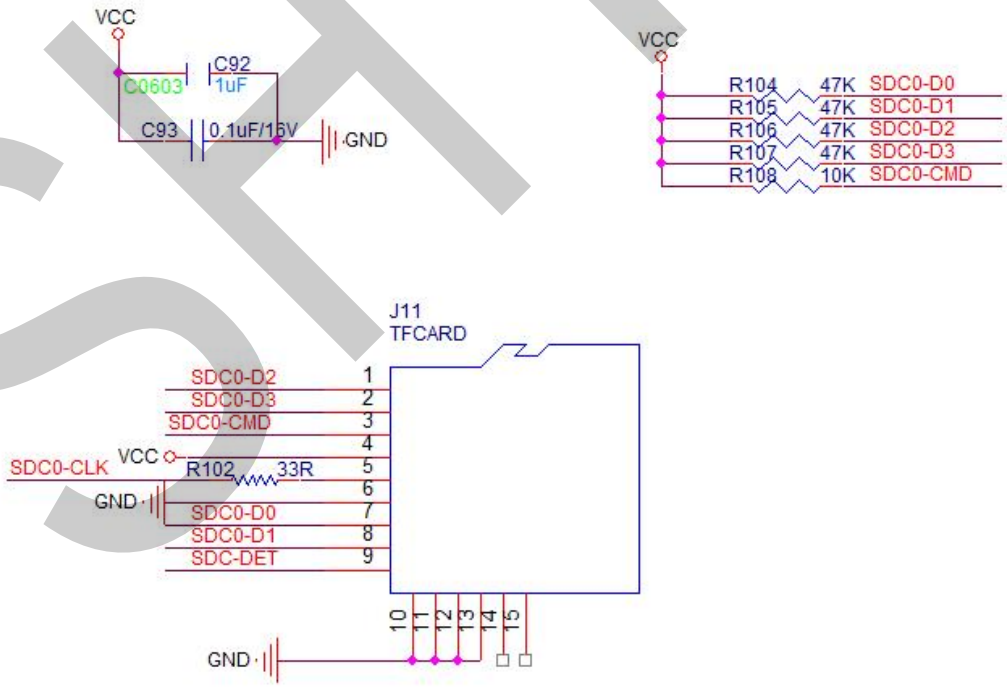
- ROM
- SD Interface

ROM

- Internal 128M Bytes memory, 60M Bytes left for users.
- Support Firmware download via USB OTG

SD Interface

- External memory
- Support secure digital memory protocol commands (up to SD3.0)
- Support secure digital I/O protocol commands (up to SDIO3.0)
- Support hardware CRC generation and error detection
- Support internal DMA controller
- Reference Design of SD



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2.3 Timer

This section includes:

- Timer

Timer

- Support watchdog reset inside
- Support audio and video synchronize counter

2.4 Display Subsystem

This section includes:

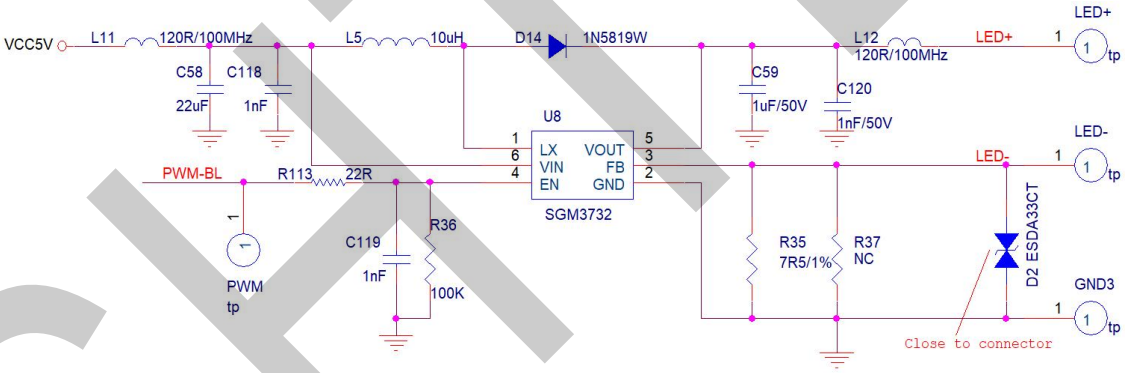
- Display Output
- Backlight Control
- LCD-VCC Control

Display Output

- RGB/LVDS/MIPI interface, up to 1920x1080@60Hz.

Backlight Control

- To adjust backlight brightness & power on/off backlight
- Reference design for backlight control



2.5 Video Engine

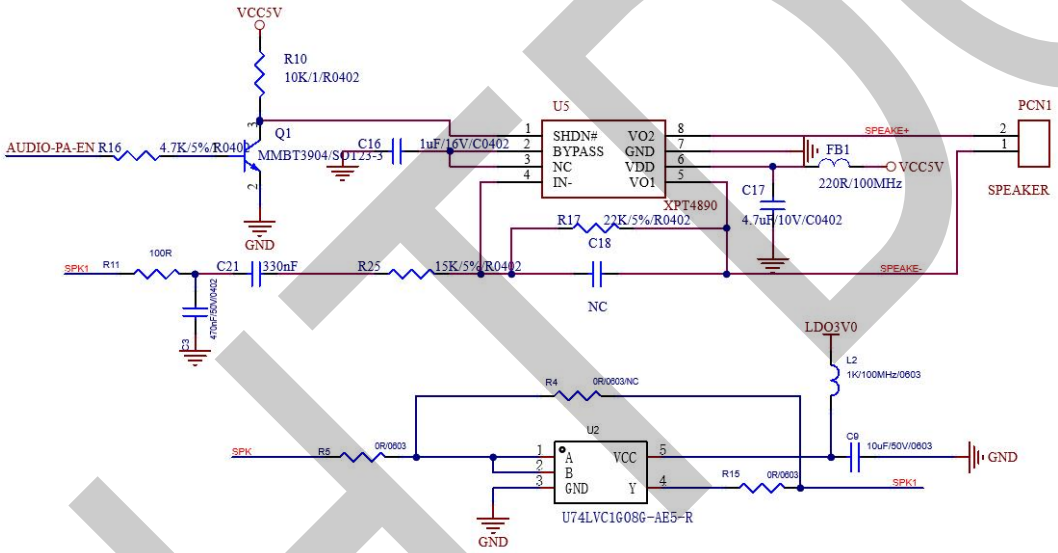
- Support H.265 MP@L4.1 up to 1920x1080@60fps decoding
- Support H.264 BP/MP/HP@L4.2 up to 1920x1080@60fps decoding
- Support format MPEG1 and MPEG2 up to 1920x1080@60fps decoding
- Support format MPEG4 SP/ASP GMC and H.263 including Sorenson Spark up to 1920x1080@60fps decoding
- Support MJPEG encode up 1920x1080@30fps
- Support JPEG encode size up to 8192 x8192
- Support JPEG decode size up to 16384 x16384

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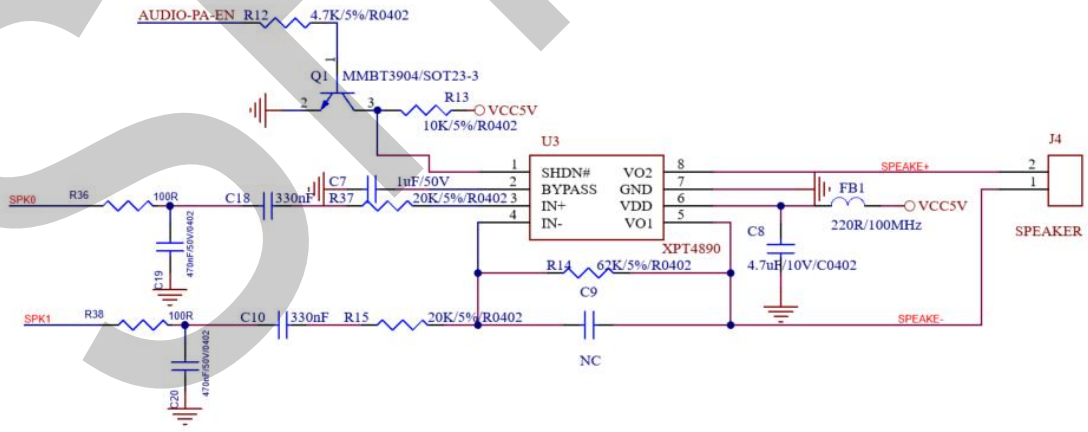
2.6 Audio Subsystem

Audio Codec

- Stereo Capless headphone drivers:
  - Up to 100dB DR
  - Supports DAC Sample Rates from 8KHz to 192KHz
- Support analog/ digital volume control
- audio inputs:
  - One analog microphone input
  - One digital microphone Bus
- One audio analog-to-digital(ADC) channel
  - 96dB SNR@A-weight
  - Supports ADC Sample Rates from 8KHz to48KHz
  - Support Auto Gain Control(AGC)
- Reference Design 1



- Reference Design 2



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2.7 System Peripherals

This section includes:

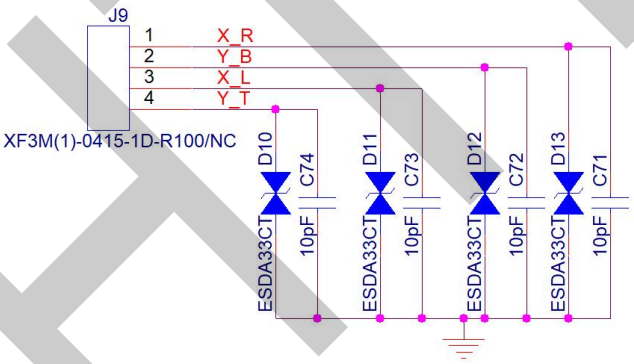
- **USB 2.0 OTG**
- **TP**
- **UART**
- **IIC**

USB 2.0 OTG

- Automated splitting/combining of packets for Bulk transfers
- Support point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Include automatic ping capabilities
- Soft connect/disconnect function
- Power Optimization and Power Management capabilities
- Include interface to an external Dedicated Central DMA controller. Data is transferred through Special bus for saving AHB bus bandwidth

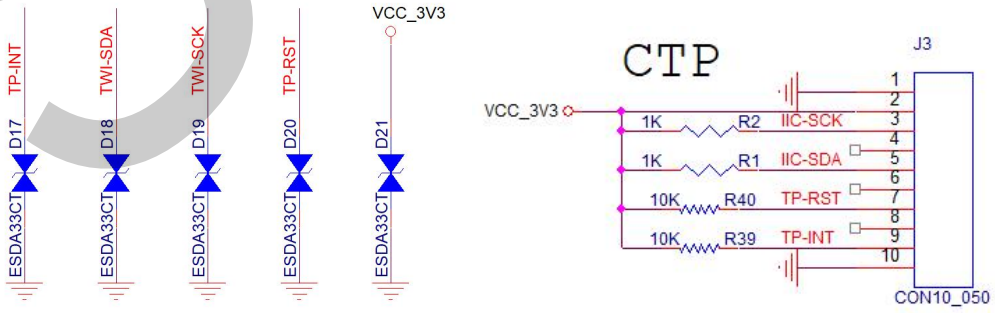
Resistive Touch Screen (RTP)

- 12-bit SAR type analog-to-digital converter
- 4-wire I/F
- Sampling frequency: 2MHz
- Median and averaging filter to reduce noise
- Support X, Y change function
- Reference Design



Capacitive Touch Screen (CTP)

- Reference Design

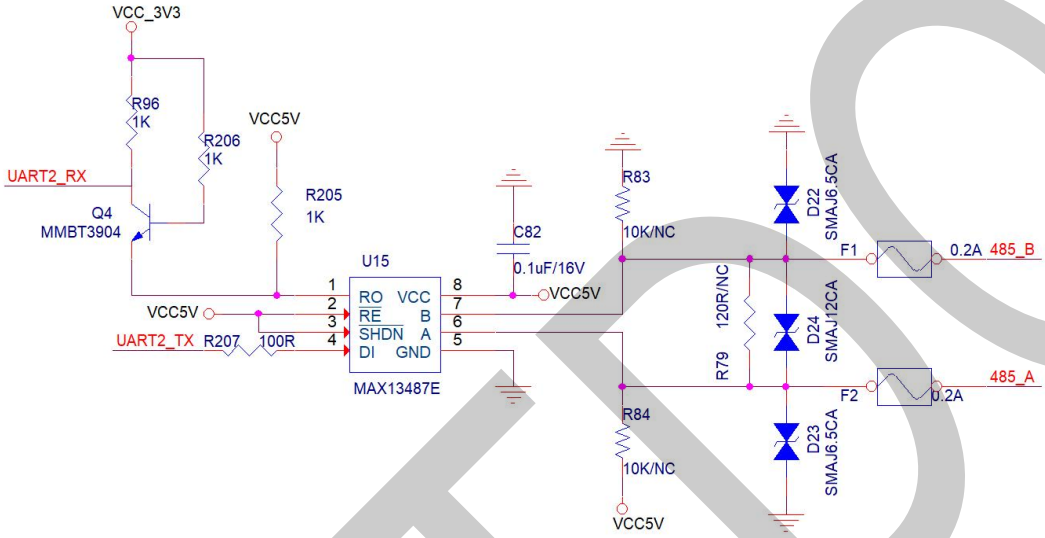


UART

- 1 UART for user
- Compatible with industry-standard 16550 UARTs
- Baud rate: up to 115200bps
- Data bits: 8, parity bit: none, stop bits:1
- 4096-Bytes receive data cache

485

- 485's reference Design



2.8 Firmware update

- **Via USB OTG**
- **Via TF card**

Update firmware via USB

- Download the firmware to 1 U disk, and then plug in and restart.

Update firmware via TF card

- Download the firmware to a TF card, and then plug in and restart.

Update firmware via USB OTG connected to PC

- First open the update software, then select the firmware image, last connect to PC while holding the download key, the software will begin downloading automatically.
- Reference Design for download key.



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3 PIN Description

3.1 Pin Table

Following table describes the X6B1 pin characteristics from seven aspects: *Pin Num, Pin Name, Default Function, Type, Reset* State, Default Pull Up/Down and so on.

(1). ***Default function*** defines the default function of each pin, especially for pins with multiplexing functions; (2). ***Pin types*** : O for output, I for input, I/O for input/output, A for analog, AI for analog input, AO for analog output, AI/O for analog input/output, OD for Open-Drain, P for power and G for ground;

1. ***Reset state*** defines the state of the terminal at reset: Z for high-impedance.
2. ***Default Pull up/down*** defines the presence of an internal pull up or pull down resistor. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;

Pin Num(1)	Default Function	Function 2	Function 3	Pin Type(2)	Reset State(3)	Default Pull Up/ Down(4)	Description
LCD							
67	LVDS0-V3P	MIPI-D3P	LCD_DE	I/O	Disabled	-	If single chanel LVDS is used, only use LVDS0 chanel; If dual chanel LVDS is used, LVDS0 is the ODD chanel and LVDS1 is the EVEN chanel.
68	LVDS0-V3N	MIPI-D3N	LCD_VS	I/O	Disabled	-	
69	LVDS0-CKP	MIPI-D2P	LCD_HS	I/O	Disabled	-	
70	LVDS0-CKN	MIPI-D2N	LCD_DCLK	I/O	Disabled	-	
71	LVDS0-V2P	MIPI-CKP	LCD_D23	I/O	Disabled	-	
72	LVDS0-V2N	MIPI-CKN	LCD_D22	I/O	Disabled	-	
73	LVDS0-V1P	MIPI-D1P	LCD_D21	I/O	Disabled	-	
74	LVDS0-V1N	MIPI-D1N	LCD_D20	I/O	Disabled	-	
75	LVDS0-V0P	MIPI-D0P	LCD_D19	I/O	Disabled	-	
76	LVDS0-V0N	MIPI-D0N	LCD_D18	I/O	Disabled	-	
1	LVDS1-V3P		LCD_D17	I/O	Disabled	-	
2	LVDS1-V3N		LCD_D16	I/O	Disabled	-	
3	LVDS1-CKP		LCD_D15	I/O	Disabled	-	
4	LVDS1-CKN		LCD_D14	I/O	Disabled	-	
5	LVDS1-V2P		LCD_D13	I/O	Disabled	-	
6	LVDS1-V2N		LCD_D12	I/O	Disabled	-	
7	LVDS1-V1P		LCD_D11	I/O	Disabled	-	
8	LVDS1-V1N		LCD_D10	I/O	Disabled	-	
9	LVDS1-V0P		LCD_D9	I/O	Disabled	-	
10	LVDS1-V0N		LCD_D8	I/O	Disabled	-	
11	LCD_D7		LCD_D7				
12	LCD_D6		LCD_D6				
SD card							

13	SDC-D1	WIFI-D1		I/O	Disabled	-	For TF card or WIFI .
14	SDC-D0	WIFI-D0		I/O	Disabled	-	
15	SDC-CLK	WIFI-CLK		I/O	Disabled	-	
16	SDC-CMD	WIFI-CMD		I/O	Disabled	-	
17	SDC-D3	WIFI-D3		I/O	Disabled	-	
18	SDC-D2	WIFI-D2		I/O	Disabled	-	
19	SDC-DET	WIFI-PWR-EN		I/O	Disabled	-	
20	1V8			P		-	1.8V output
21	3V3			P		-	3.3V output
22	3V3			P		-	3.3V output
23	MAC0_RXD1	BT-WAKE		I/O	Disabled	-	For Ethernet network or Bluetooth
24	MAC0_RXD0	BT-HOST-WAKE		I/O	Disabled	-	
25	MAC0_CRS_DV	WIFI-PWR-ON		I/O	Disabled	-	
26	MAC0_REFCLK	WIFI-HOST-WAKE		I/O	Disabled	-	
27	MAC0_TXD1	WIFI-32K		I/O	Disabled	-	
28	MAC0_TXD0	BT_PWR_ON		I/O	Disabled	-	
29	EPHY0-RST	BT-TX		I/O	Disabled	-	
30	MAC0_TXEN	BT-RX		I/O	Disabled	-	
31	MAC0_MDC	BT-RXS		I/O	Disabled	-	
32	MAC0_MDIO	BT-CTS		I/O	Disabled	-	
33	EPHY0-25M	SPK0		I/O	Disabled	-	
GPIO							
34	SPK1			A	-	-	Audio signal
35	VCC			P			3.3~5.5V input
36	VCC			P			3.3~5.5V input
37	GND			G		-	
38	GND			G		-	
39	UART-TX			I/O	Disabled	-	For UART or 485, 3.3V TTL
40	UART-RX			I/O	Disabled	-	
41	TWI3_SCK	CAN0_TX		I/O	Disabled	-	-
42	TWI3_SDA	CAN0_RX		I/O	Disabled	-	-
43	BEEP			I/O	-	-	Active buzzer signal
44	LCD-PWM			I/O	Disabled	-	To enable/disable or dim the LCD's backlight.
45	GND			G	-	-	-
46	RESET			I	Disabled	-	Low active
USB							
47	USB0-DM			A		-	To download

48	USB0-DP			A		-	firmware, UI, and so on.
GPIO							
49	NC			I/O	Disabled	-	-
50	LDO3V0_OUT			P	-	-	LDO type 3.0V output
51	DBGTX	UBOOT		I/O	Disabled	-	For the manufacture to DEBUG
52	DBGRX			I/O	Disabled	-	For the manufacture to DEBUG
53	AUDIO-PA-EN			I/O	Disabled	-	Automatically enable/disable audio amplifier, Logic high for shutdown
Touch Panel							
54	RTP_XP_RST	CTP_RST		I/O	Disabled	-	For RTP or CTP
55	RTP_YP_INT	CTP_INT		I/O	Disabled	-	
56	RTP_XN_SCK	CTP_SCK		I/O	Disabled	-	
57	RTP_YN_SDA	CTP_SDA		I/O	Disabled	-	
GPIO							
58	32K_OUT			OD	Disabled	-	OD output, need pull up resistor outside, the pull-up voltage cannot exceed 5V
59	VCOIN_RTC			P	Disabled	-	RTC power supply, only need to connect to coin battery
60	LCD_CS	UART5_TX		I/O	Disabled	-	
61	LCD_RST	UART5_RX		I/O	Disabled	-	
62	NC			-	-	-	
63	NC			-	-	-	
64	USB0-ID	DMIC_DATA		I/O	Disabled	-	
65		DMIC_CLK		I/O	Disabled	-	

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66	GND			G		-	

3.2 Detailed Pin Description

Pin Name	Description	Type
Audio Codec		
HPL	Headphone Left Output	AO
HPR	Headphone Right Output	AO
AVCC	Analog Power	P
AGND	Analog Ground	G
Touch Panel		
RTP_YT	Resistive touch Panel Y-axis top input	AI
RTP_YB	Resistive touch Panel Y-axis bottom input	AI
RTP_XR	Resistive touch Panel X-axis right input	AI
RTP_XL	Resistive touch Panel X-axis left input	AI
Miscellaneous Signal		
RESET#	Chip Reset Signal	I
PWM	Pulse Width Modulation Output	O
ADC		
ADC	ADC Input for Key Board or sensor	I
UART		
UART_TX	UART Data Transmit	O
UART_RX	UART Data Receive	I
SDC		
SDC_D[3:0]	SD/MMC/SDIO Data Bit[3:0]	I/O
SDC_CLK	SD/MMC/SDIO Clock	O
SDC_CMD	SD/MMC/SDIO Command	I/O
IIC(Open-Drain)		
IIC_SCL	IIC Clock	I/O
IIC_SDA	IIC Data	I/O

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4.Electrical Characteristics

4.1 Absolute Maximum Ratings

Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
T_{stg}	Storage Temperature	-40	120	°C
Hstg	Storage humidity level		90%	RH
MSL Level	3	-	-	-
$I_{I/O}$	In/Out current for input and output	-40	40	mA
$V_{I/O}$	I/O input voltage	-0.3	3.6	V
VCC	Power Supply for VCC	-0.3	5.5	V

4.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	85	°C
VCC	Power Supply	3.3	5.0	5.5	V
P	Model Power consumption		0.6	0.7	W

4.3 DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * 3.3	-	3.3 + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * 3.3	V
R_{PU}	Input pull-up resistance	50	100	150	KΩ
R_{PD}	Input pull-down resistance	50	100	150	KΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	3.3 -0.2	-	3.3	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

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4.4 Power Up/ Down Sequence

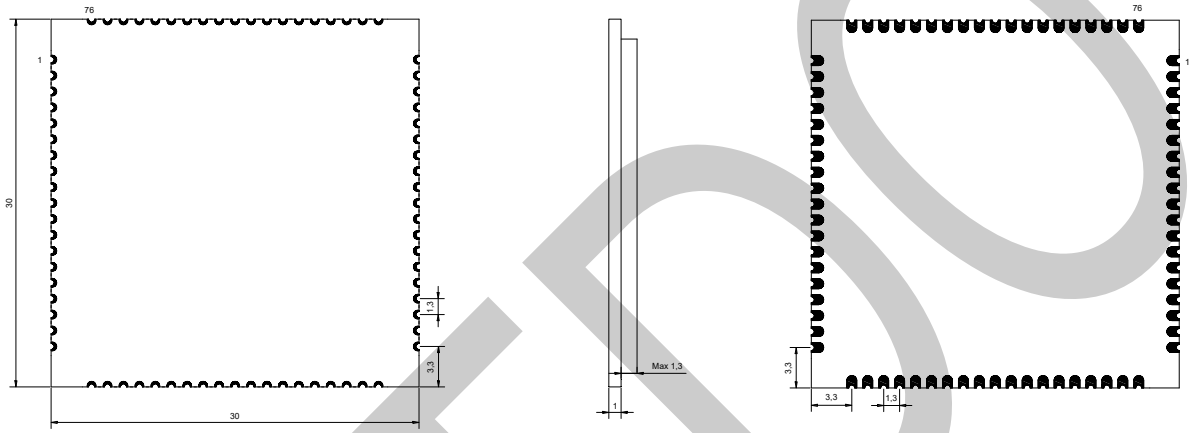
No special restrictions for power up/ down sequence.

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5. Package Dimension

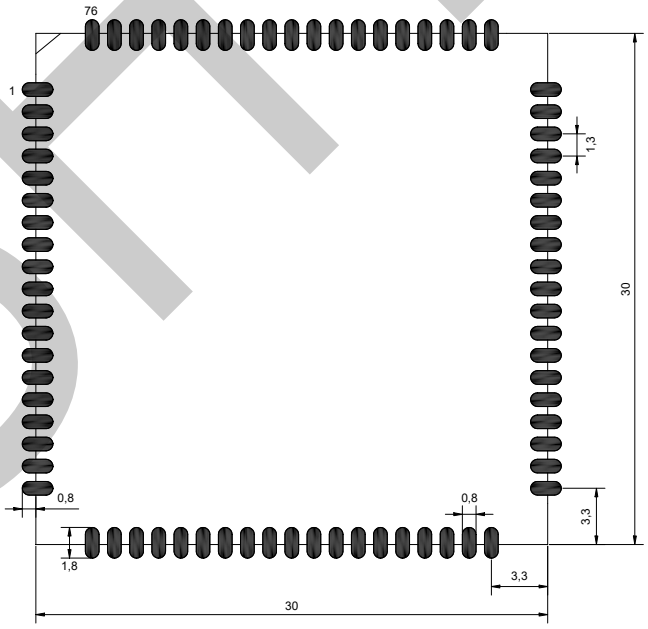
5.1 Structure

The following figure shows the top, bottom, and side views.



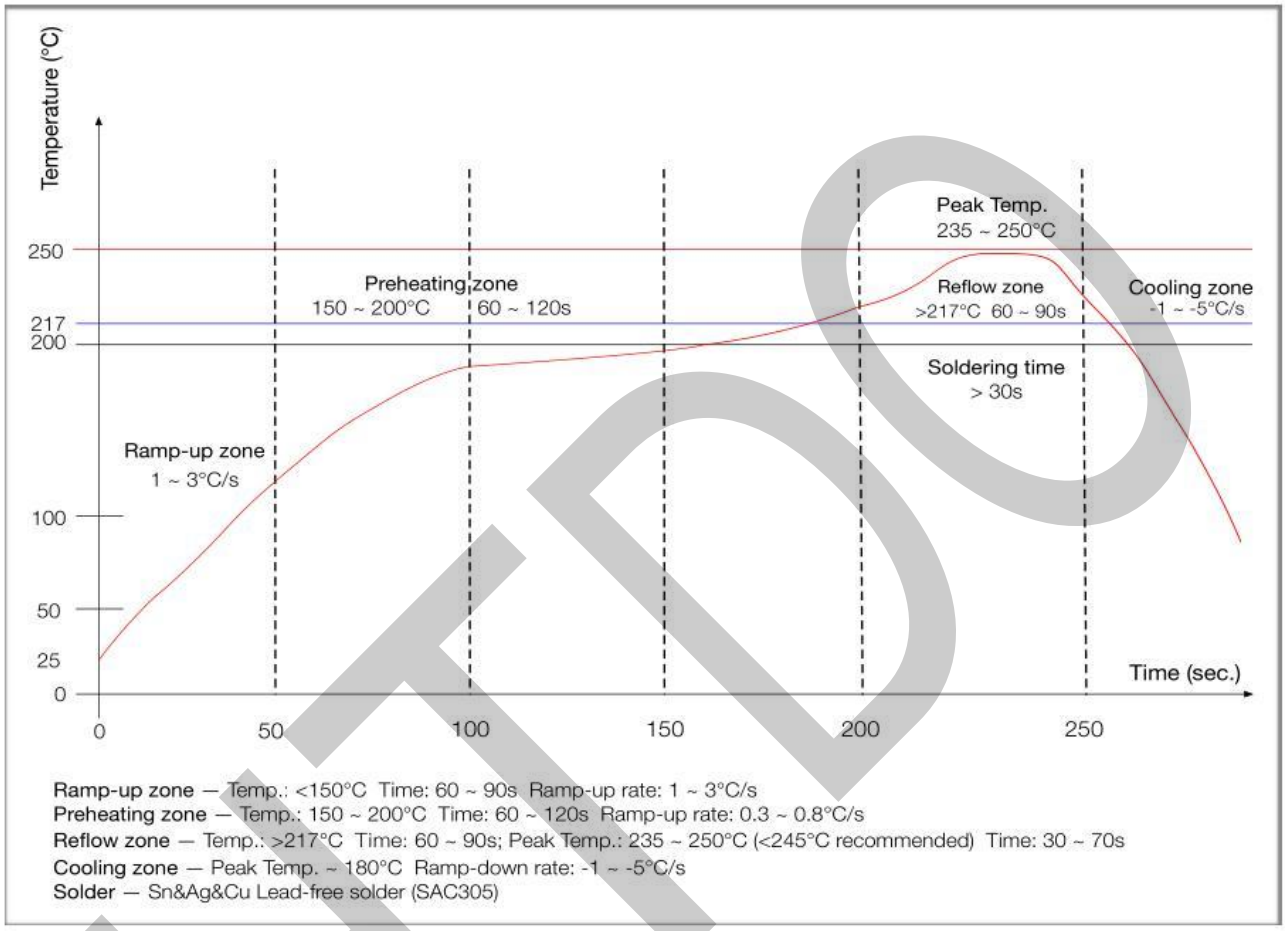
Top view Side view Bottom view

5.2 Recommended PCB footprint



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6. Reflow Profile



Ramp-up zone — Temp.: <150°C Time: 60 ~ 90s Ramp-up rate: 1 ~ 3°C/s
Preheating zone — Temp.: 150 ~ 200°C Time: 60 ~ 120s Ramp-up rate: 0.3 ~ 0.8°C/s
Reflow zone — Temp.: >217°C Time: 60 ~ 90s; Peak Temp.: 235 ~ 250°C (<245°C recommended) Time: 30 ~ 70s
Cooling zone — Peak Temp. ~ 180°C Ramp-down rate: -1 ~ -5°C/s
Solder — Sn&Ag&Cu Lead-free solder (SAC305)

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