Multipoint-LVDS Line Driver and Receiver

Features

- Exceeds the LVDS Standard TIA/EIA-644 for High-Speed Data Interchange
- Low-Voltage Differential 100-Ω (Typical) Line Receivers for Signaling Rates, up to 400-Mbps, 200-Mbps Clock
- 3.3-V Power Supply Design
- 6-ns Maximum Propagation Delay
- 0.1-ns Differential Skew (Typical)
- Accepts Small Swing (350 mV Typical) V_{ID}
- Supports Open, Short, and Terminated Input Fail-Safe
- Power-down High Impedance on LVDS Inputs
- Bus-Pin Protection: ±8-kV HBM Model
- –40°C to 85°C Operation Temperature Range

Applications

- Backplane Multipoint Data/Clock Transmission
- Cellular Base Stations
- Network Switches and Routers
- Industrial Control
- Communication Infrastructure

Description

The TPT9L484 is a 3.3-V 4-channel Low-Voltage Differential (LVDS) line receiver which supports 400-Mbps data rates. Receiver inputs are protected against ±8-kV ESD strikes without latch-up.

The TPT9L484 accepts low-voltage differential input signals as 350 mV typical and translates them to 3.3-V CMOS output levels. The receivers support a tri-state function that can be used for multi-channel outputs. The receivers also support open, shorted, and terminated (100 Ω) input fail-safe, withholding output at a high level. Its operating temperature range is from −40°C to +85°C. The device is available in the TSSOP16 package.

Typical Application Circuit

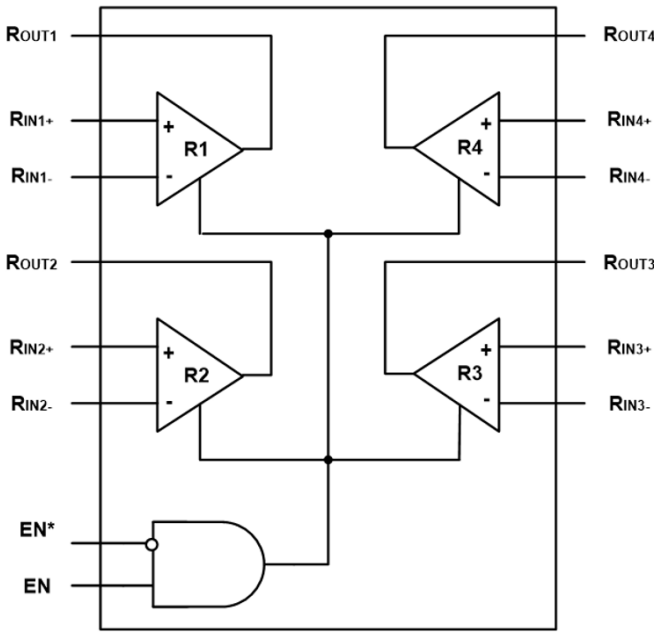


Table of Contents

Features **1**
Applications **1**
Description **1**
Typical Application Circuit **1**
Revision History **3**
Pin Configuration and Functions **4**
Specifications **6**
Absolute Maximum Ratings (1) 6
ESD, Electrostatic Discharge Protection 6
Recommended Operating Conditions 7
Thermal Information 7
Electrical Characteristics – DC Parameter 8
Electrical Characteristics – AC Parameter 9
Application and Implementation **10**
Typical Application 10
Tape and Reel Information **11**
Package Outline Dimensions **12**
TSSOP16 12
Order Information **13**
IMPORTANT NOTICE AND DISCLAIMER **14**

Revision History

Date	Revision	Notes
2018-12-14	Rev.Pre.0	Preliminary version.
2019-02-26	Rev.Pre.1	Added package information.
2019-06-06	Rev.Pre.2	Added electrical data.
2019-08-12	Rev.Pre.3	Updated electrical data.
2019-08-23	Rev.Pre.4	Updated package information.
2019-10-09	Rev.A.0	Initial release.
2020-01-04	Rev.A.1	Updated Functional Block Diagram and Pin Functions.
2024-12-24	Rev.A.2	Updated to a new datasheet format. Updated the POD.

Pin Configuration and Functions

TPT9L484L1-TSR
TSSOP16
Top View

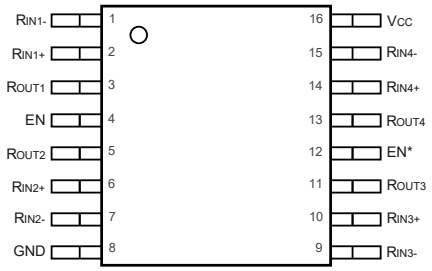


Table 1. Pin Functions: TPT9L484

Pin No.	Name	I/O	Description
1	R_{IN1-}	Bus Input	Inverting receiver input pin.
2	R_{IN1+}	Bus Input	Non-inverting receiver input pin.
3	R_{OUT1}	Output	Receiver output pin.
4	EN	Input	Active high enable pin, see details in Table 2.
5	R_{OUT2}	Output	Receiver output pin.
6	R_{IN2+}	Bus Input	Non-inverting receiver input pin.
7	R_{IN2-}	Bus Input	Inverting receiver input pin.
8	GND	Ground	Ground.
9	R_{IN3-}	Bus Input	Inverting receiver input pin.
10	R_{IN3+}	Bus Input	Non-inverting receiver input pin.
11	R_{OUT3}	Output	Receiver output pin.
12	EN*	Input	Active low enable pin, see details in Table 2.
13	R_{OUT4}	Output	Receiver output pin.
14	R_{IN4+}	Bus Input	Non-inverting receiver input pin.
15	R_{IN4-}	Bus Input	Inverting receiver input pin.
16	V_{CC}	Power	Power supply.

Function Table

Table 2. Truth Table

Enable		Inputs	Outputs
EN	EN*	$R_{IN+} - R_{IN-}$	R_{OUT}
L	H	X	Z

Enable		Inputs	Outputs
EN	EN*	$R_{IN+} - R_{IN-}$	R_{OUT}
All Other Combinations of Enable Inputs $V_{ID} \geq 0.1$ V H $V_{ID} \leq -0.1$ V L Full Fail-Safe Open/Short/Terminated H		$V_{ID} \geq 0.1$ V	H
		$V_{ID} \leq -0.1$ V	L
		Full Fail-Safe Open/Short/ Terminated	H

Specifications

Absolute Maximum Ratings (1)

Parameters		Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4	V
R_{IN+}, $R_{IN–}$	Input Voltage	–0.3	3.9	V
EN, EN*	Enable Input Voltage	–0.3	V_{CC} + 0.3	V
R_{OUT}	Output Voltage	–0.3	V_{CC} + 0.3	V
T_L	Lead Temperature, Soldering (4 s)		260	°C
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition		Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	Bus Pins	8	kV
			All Pins except Bus Pins	4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	All Pins	1	kV
EFT		IEC-61000-4-4	Bus Pins	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3	3.3	3.6	V
V_{IH}	High-Level Input Voltage	2		V_{CC}	V
V_{IL}	Low-Level Input Voltage	GND		0.8	V
$\|V_{ID}\|$	Magnitude of Differential Input Voltage	GND		V_{CC}	V
T_A	Operating Free-Air Temperature	–40	25	85	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP16	120	60	°C/W

Electrical Characteristics – DC Parameter

All test conditions: V_{CC} = 3.0 V to 3.6 V, T_A = −40°C to 85°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{TH}	Differential Input High Threshold	V_{CM} = 1.2 V, R_{IN+}, R_{IN-} pins			25	100	mV
V_{TL}	Differential Input Low Threshold			–100	–25		mV
V_{CMR}	Common-Mode Voltage Range	V_{ID} = 200-mV peak-to-peak, R_{IN+}, R_{IN-} pins		0.1		2.3	V
I_{IN}	Input Current	V_{CC} = 3.6 V or 0 V, R_{IN+}, R_{IN-} pins	V_{IN} = 2.8 V	–15		15	µA
			V_{IN} = 0 V	–15		15	µA
		V_{CC} = 0 V, V_{IN} = 3.6 V, R_{IN+}, R_{IN-} pins		–20	12.5	20	µA
V_{OH}	Output High Voltage	I_{OH} = –0.4 mA, V_{ID} = 200 mV, R_{OUT} pin		2.7	3.3		V
		I_{OH} = –0.4 mA, input terminated, R_{OUT} pin		2.7	3.3		V
		I_{OH} = –0.4 mA, input shorted, R_{OUT} pin		2.7	3.3		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = –200 mV, R_{OUT} pin			0.1	0.25	V
I_{OS}	Output Short-Circuit Current	Enabled, V_{OUT} = 0 V, R_{OUT} pin		−15	−80	−120	mA
I_{OZ}	Output Tri-State Current	Disabled, V_{OUT} = 0 V or V_{CC}		–10	±0.1	10	µA
V_{IH}	Input High Voltage	EN, EN* pins		2		V_{CC}	V
V_{IL}	Input Low Voltage	EN, EN* pins		GND		0.8	V
I_I	Input Current	V_{IN} = 0 V or V_{CC}, other input = V_{CC} or GND, EN, EN* pins		–10		10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = –18 mA, EN, EN* pins			–0.8		V
I_{CC}	No Load Supply Current	EN, EN* = V_{CC} or GND, inputs open, V_{CC} pin			15	20	mA
	Receivers Enabled	EN, EN* = 2.4 V or 0.5 V, inputs open, V_{CC} pin			15	20	mA
I_{CCZ}	No Load Supply Current	Receivers disabled, EN = GND, EN* = V_{CC}, inputs open, V_{CC} pin			6	10	mA

Electrical Characteristics – AC Parameter

All test conditions: V_{CC} = 3.0 V to 3.6 V, T_A = −40°C to 85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}	Differential Propagation Delay, High to Low (1)	C_L = 10 pF	3.2	4.5	6.2	ns
t_{PLH}	Differential Propagation Delay, Low to High (1)	V_{ID} = 200 mV	3.0	4.5	6.2	ns
t_{SKD1}	Differential Pulse Skew (1) $\lvert T_{PHLD} - T_{PLHD} \rvert$			0.1		ns
t_{SKD2}	Differential Channel-to-Channel Skew (1)	Same device		0.1	2.0	ns
t_{SKD3}	Differential Part-to-Part Skew (1)	Different device		0.1	2.0	ns
t_{TLH}	Rise Time			1.0		ns
t_{THL}	Fall Time			1.0		ns
t_{PHZ}	Disable Time High to Z	R_L = 2 kΩ		6		ns
t_{PLZ}	Disable Time Low to Z	C_L = 10 pF		6		ns
t_{PZH}	Enable Time Z to High			6		ns
t_{PZL}	Enable Time Z to Low			4		ns
f_{MAX}	Maximum Operating Frequency (1)	All channels switching			200	MHz

(1) Spec limit is based on bench characterization and design simulation.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 1 shows the typical application schematic.

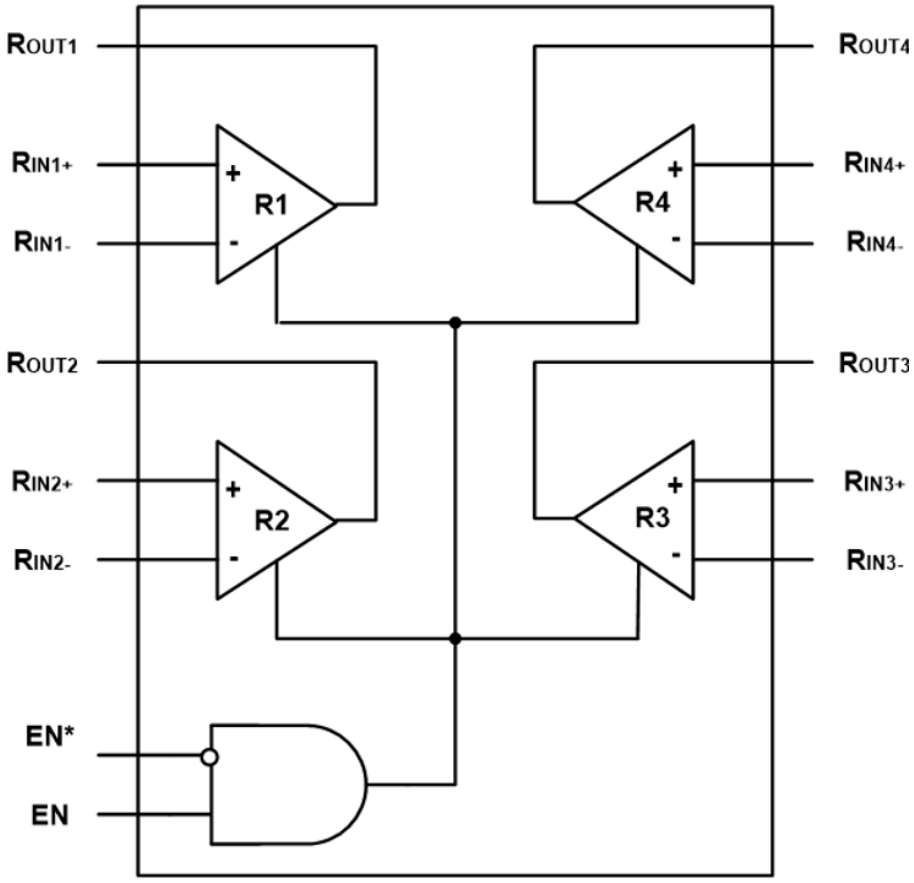
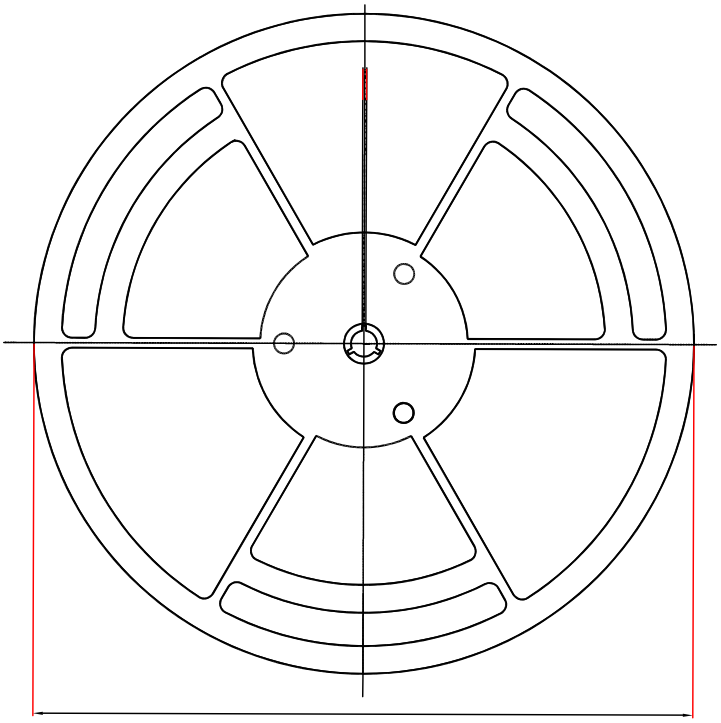
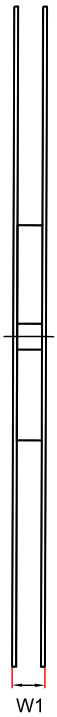
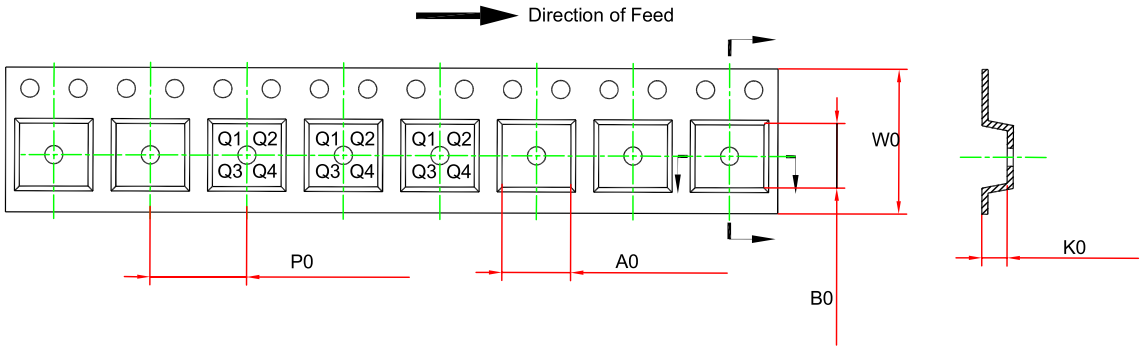


Figure 1. Typical Application Circuit

Tape and Reel Information







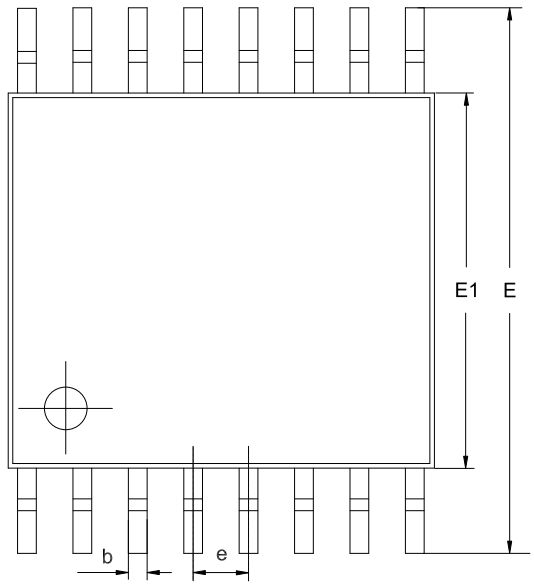
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT9L484L1-TSR-S	TSSOP16	330	17.6	6.8	5.5	1.5	8.0	12.0	Q1

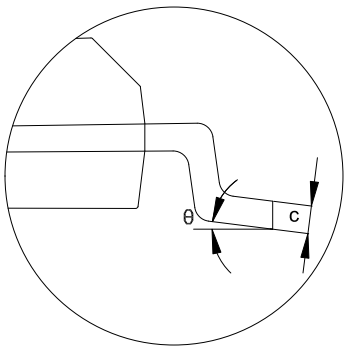
(1) The value is for reference only. Contact the 3PEAK factory for more information.

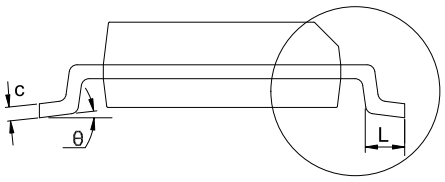
Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT9L484L1-TSR-S	−40 to 85°C	TSSOP16	T9L484	1	Tape and Reel, 3000	Green

(1) Mark Definition: include symbol, part, date code (details about how to read date code), filled by OP.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Copyright© 3PEAK 2012-2025. All rights reserved.

Trademarks. Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.