SPECIFICATION

Customer: _____

Model Name: SAT035TM54D06Y0-30638T058KN-02

ERP NO.: 1010350016

Spec Vision: V.1

Date: 2015-09-20

■ **Preliminary Specification**

☐ **Final Specification**

Approved by	Comment

Prepared by	Reviewed by	Approved by

Preliminary

Record of Revision

Version	Revise Date	Page	Content	Modified by
V.1	2015-09-20	ALL	First Issued.	

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1. General Specifications

3.5” is a color active matrix thin film transistor (TFT) TN liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, Driver IC, FPC and Backlight.

NO.	Item	Specification	Remark
1	Panel Size	3.5 inch(Diagonal)	
2	Driver Method	a-Si TFT active matrix	
3	Display Color	16.7M	
4	Display Mode	Normally White	
5	Viewing Direction	12 O' Clock	
	Gray Scale Inversion Direction	6 O' Clock	
6	Resolution	320 x 3(RGB) x 240	
7	Active Area	70.08(W) x 52.56(H) mm	
8	Dot Pitch	0.219(W) x 0.219 (H) mm	
9	Pixel Arrangement	RGB-stripe	
10	Module Size	76.9(W) x 63.9(H) x 3.0(D) mm	
11	Interface	RGB	
12	Driving IC	NV3035	
13	Backlight	White LED	
14	Weight	TBD	g

Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: LCM weight tolerance: ±5%

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2. Pin Assignment

No.	Symbol	Function	Remarks
1~2	LED_K	Power for LED backlight(Cathode)	
3~4	LED_A	Power for LED backlight(anode)	
5~7	NC	No connection	
8	RESTET	Hardware Reset	
9	SCS	Interface Data Enable Signal	
10	SCL	Interface Data Clock	
11	SDI	Interface Data	
12~19	B0~B7	Blue data	
20~27	G0~G7	Green data	
29~35	R0~R7	Red data（DX0~DX7）	
36	HSYNC	Horizontal Sync input	
37	VSYNC	Vertical Sync input	
38	DOTCLK	Pixel clock	
39~40	NC	No connection	
41~42	VDD	Digital Power	
43~47	NC	No connection	
48	XR	Right electrode-differential analog	When this PIN not used, Please leave it open
49	YD	Bottom electrode-differential analog	
50	XL	Left electrode-differential analog	
51	YU	Top electrode-differential analog	
52	DEN	Data input enable	
53~54	GND	Ground	

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3. Operation Specifications

3.1. Absolute Maximum Ratings

Voltage (AGND=GND=0V, Ta = 25℃)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power Voltage	VDD	-0.5	5.0	V	
Operating Temperature	Top	-20	55	℃	
Storage Temperature	Tst	-20	60	℃	

Note: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings case, the module may be permanently destroyed.

3.1.1. Typical Operation Range

Item	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Voltage	VDD	3.0	3.3	3.6	V
Input logic high voltage	V_{IH}	0.7V_{DD}	-	V_{DD}	V
Input logic low voltage	V_{IL}	0	-	0.3V_{DD}	V

3.1.2. Current Consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Current for Driver	I_{VDD}	-	10	-	mA	VDD=3.3V

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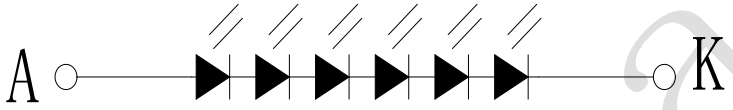
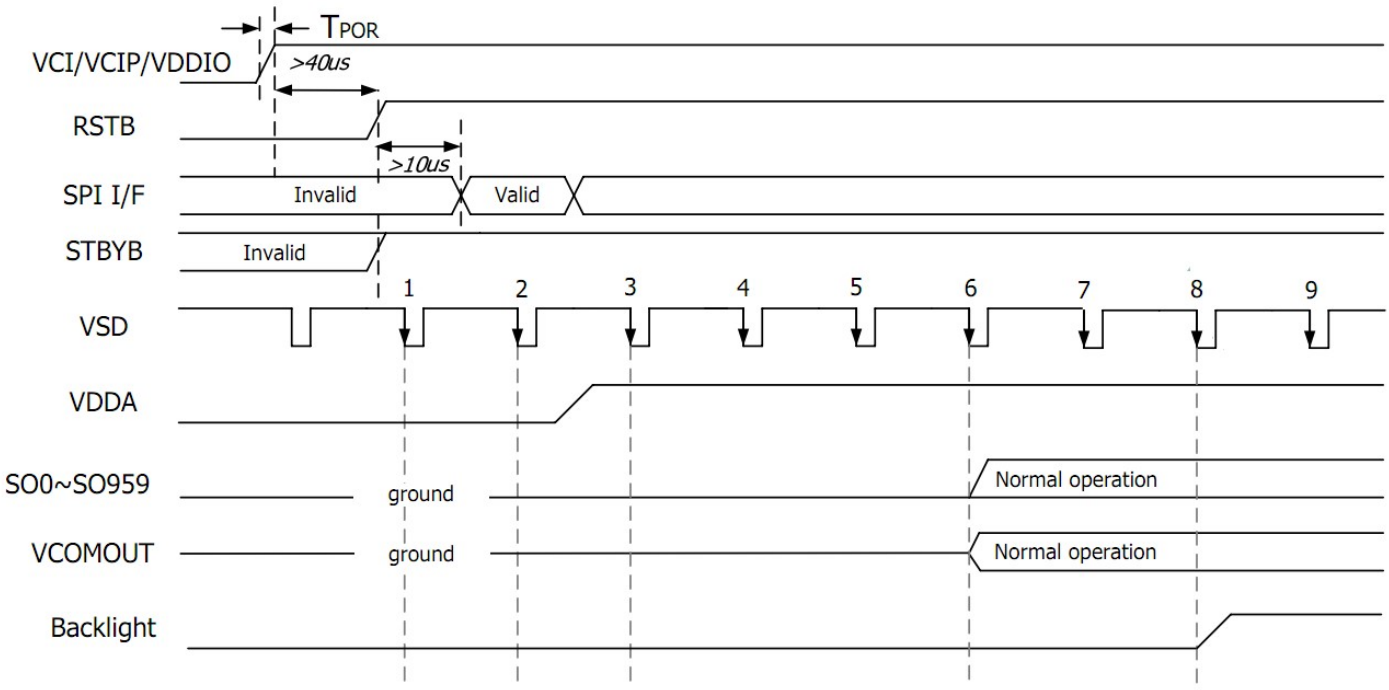
3.1.3. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage of white LED backlight	V_L	17.4	18.6	19.8	V	6S
Current for LED backlight	IL	--	20	-	mA	20mA/LED
Power dissipation	Pd	-	372	-	mW	6LED
Luminance (on the module surface,BM-7)		350	400	-	cd/m^2	
LED life time	-	30000	-	-	Hr	



3.2. Power Sequence

3.2.1. Power-On Timing Sequence



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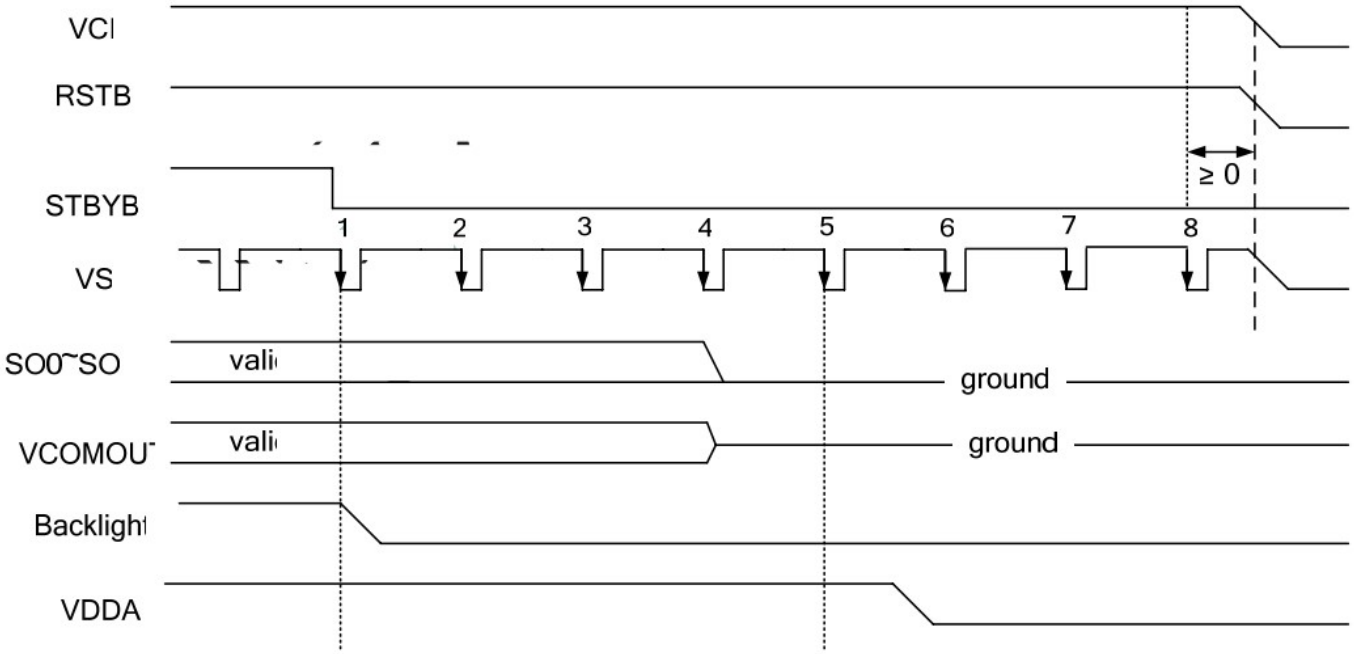
3.2.2 Power-Off Timing Sequence



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3.3. Timing Characteristics

3.3.1 Electrical Characteristics

(Test Condition: VCI=VCIP=3.3V, VDDA=5.0V, VSS=GNDA=VSSP=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply Voltage	VCI	3.0	3.3	3.6	V	
I/O power supply	VDDIO	VDD	3.3	3.6	V	
Pump circuits supply	VCIP	3.0	3.3	3.6	V	
Low power supply	VDD	1.6	1.8	2.0	V	
Low Level Input Voltage	Vil	VSS	-	0.2xVDDIO	V	Digital input pins TA=25℃
High Level Input Voltage	Vih	0.8xVDDIO	-	VDDIO	V	Digital input pins TA=25℃
Input Leakage Current	Ii	-	-	±1	μA	Digital input pins
High Level Output Voltage	Voh	VDDIO-0.4	-	VDDIO	V	Digital output pins; Ioh=400μA
Low Level Output Voltage	Vol	VSS	-	VSS+0.4	V	Digital output pins; Iol= -400 A
2xVCI pump output level	VINT1	5.2	5.5	5.8	V	VCIP=3.3V, w/o panel loading
Analog power voltage	VDDA	4.5	5.0	VINT1-0.3	V	Analog circuit power from Power Block
VCOMAC output level	VCOMAC	4.6	-	VINT1-0.3	V	By VCSL[2:0] setting VCOMAC=$V_{(VCSL[3:0])}$±100mV
VCOMDC output level	VCOMDC	1.0	-	2.26	V	By VCDCSL[5:0] setting VCOMDC= $V_{(VCDCSL[5:0])}$±50mV
Positive power supply	VGH	14.5	15	15.5	V	Gate driver load + procard load
Negative power supply	VGL	-10	-8	-6	V	Gate driver load + procard load
Base drive current	IDRV	-	-	10	mA	VCIP=3.3V, DRV=0.7V
DRV output voltage	VDRV	VSS+0.1	-	VCI-0.1	V	
Feed back voltage	VFB	0.55	0.6	0.65	V	DC/DC operating, VBL current=20mA
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	Vo=0.1V~0.5V & VDDA-0.5V~VDDA-0.1V
			±15	±25	mV	Vo=0.5V~VDDA-0.5V
Low-Level Output Current of VCOMOUT	IOLF	-	-10	-	mA	Force VCOMAC=6.0V VCOMOUT output=0V V.S 0.9V
High-Level Output Current of VCOMOUT	IOHF	-	10	-	mA	Force VCOMAC=6.0V VCOMOUT output=6.0V V.S 5.1V
Source Low-Level Output Current	I_{OLS}	-	-30	-	μA	Son=Vo V.S. (Vo+0.9)
Source High-Level Output Current	I_{OHS}	-	30	-	μA	Son=Vo V.S. (Vo-0.9)
Gate Low-Level Output Current	IOLG	-	-250	-	μA	GOn; Vo=VGL V.S. (VGL+0.5)
Gate High-Level Output Current	IOHG	-	250	-	μA	GOn; Vo=VGL V.S. (VGH-0.5)
Chip Stand-by Current	Idds	-	15	50	μA	STBYB="0", all function are shutdown, CLKIN/VSD/HSD halted
Chip Operating Current	Idda	-	10	-	mA	No load, CLKIN=27MHz, Fld=15KHz

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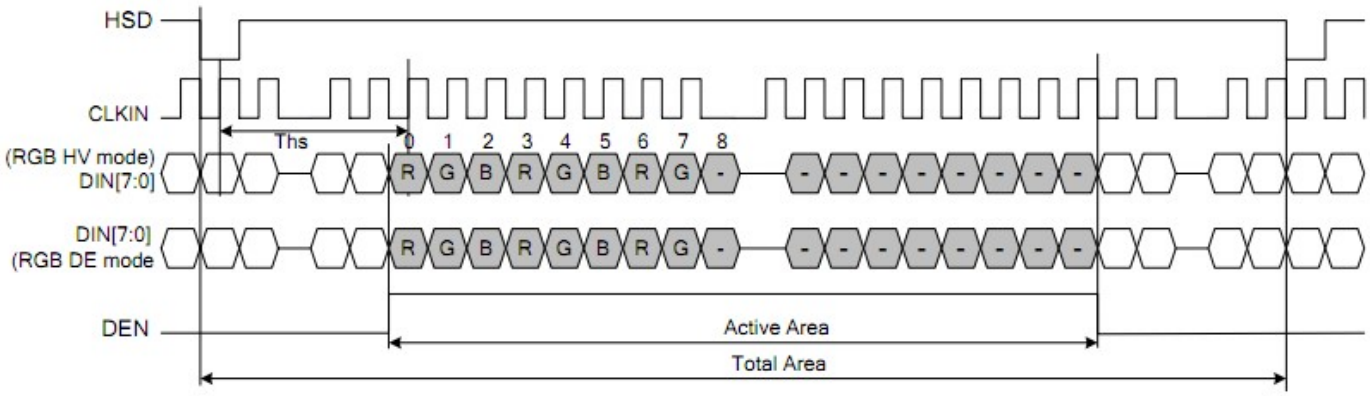
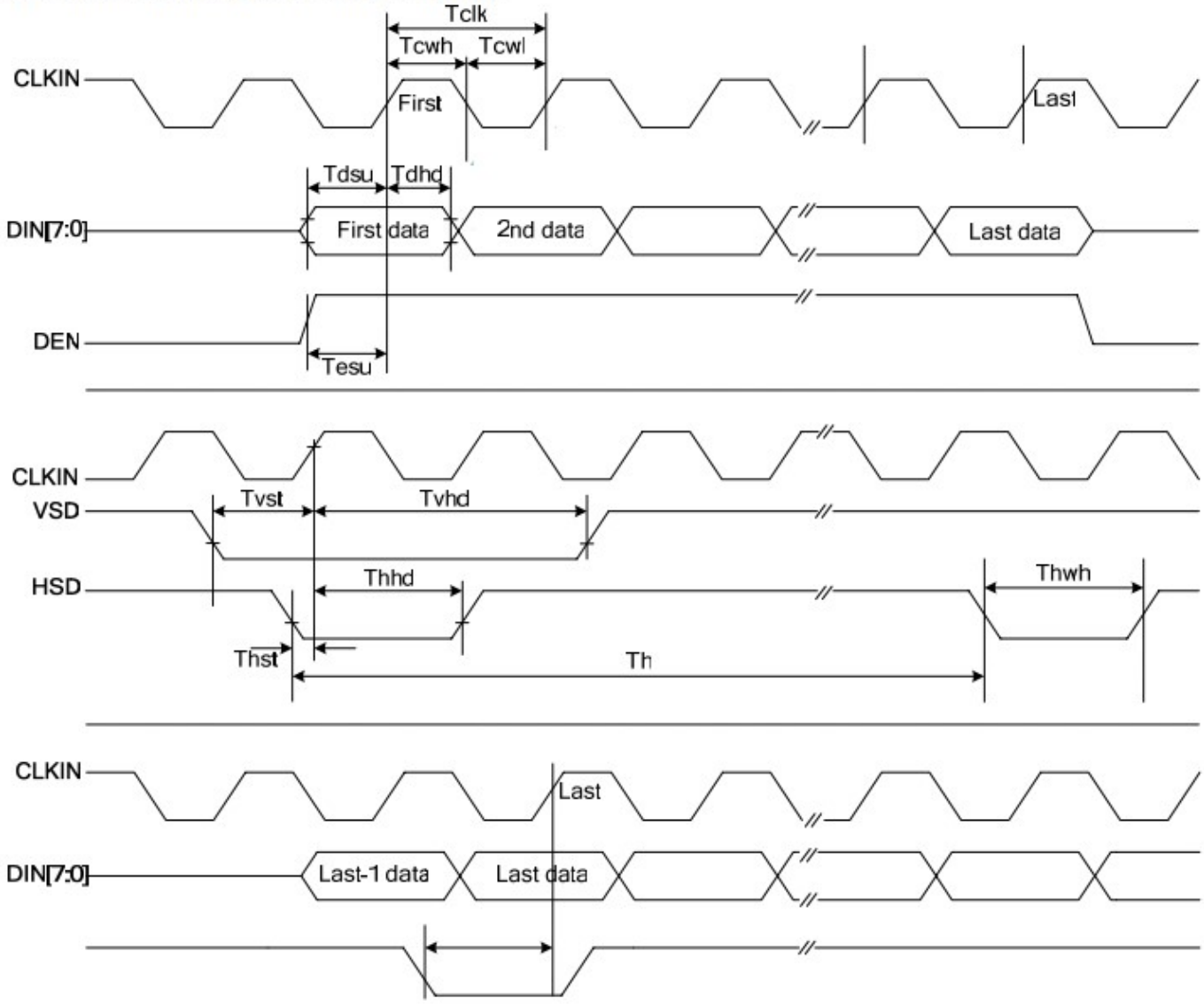
3.3.2 Input Data Format



Input Format	Format Standard	CLKIN(MHz)	HSD(CLKIN)	Total Area (CLKIN)	Active Area (CLKIN)	Note
8bit RGB	8bit RGB	27	1	1716	960	960×240
24bit RGB	24bit RGB	6.4	1	408	320	

3.3. Time Diagram

Clock and Data Input Timing Diagram



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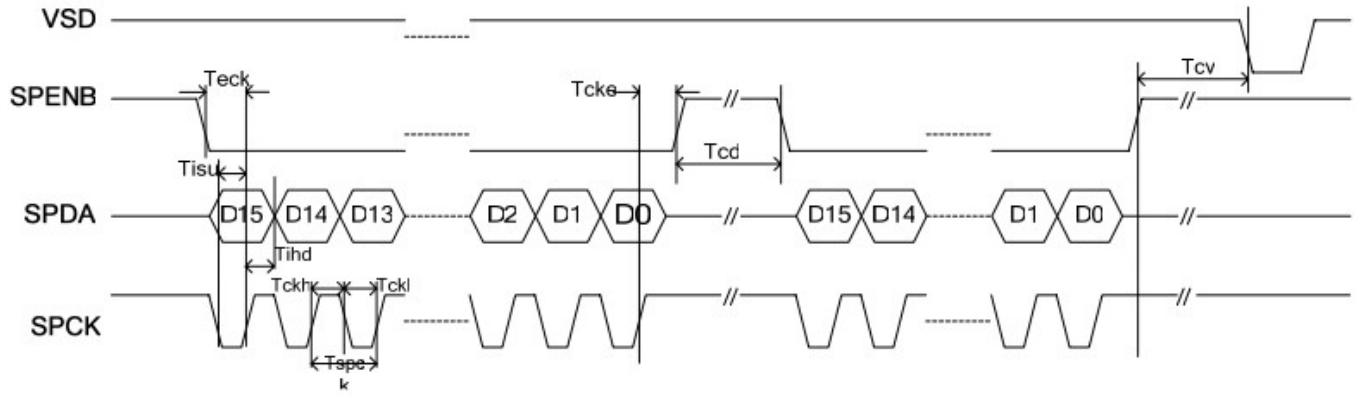
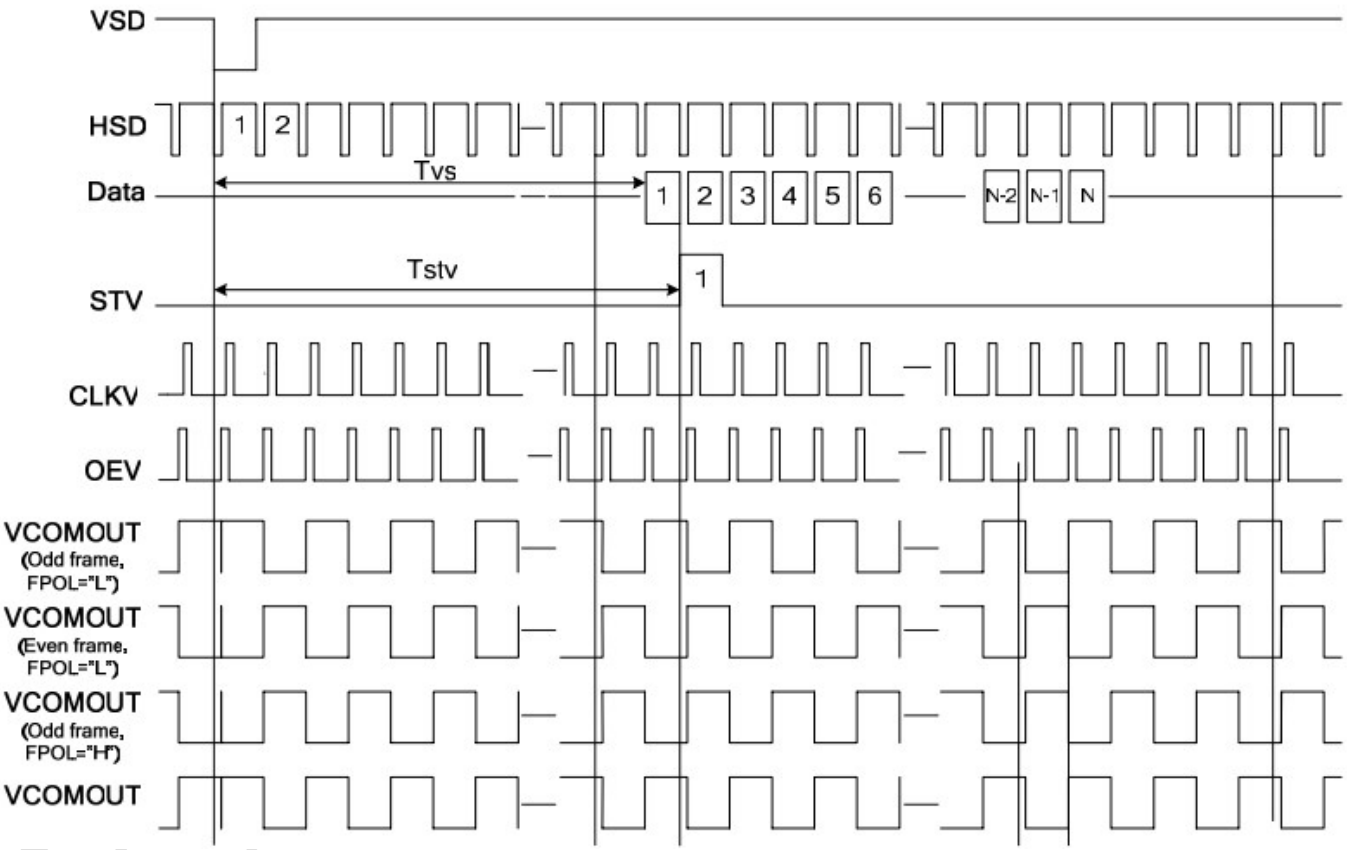
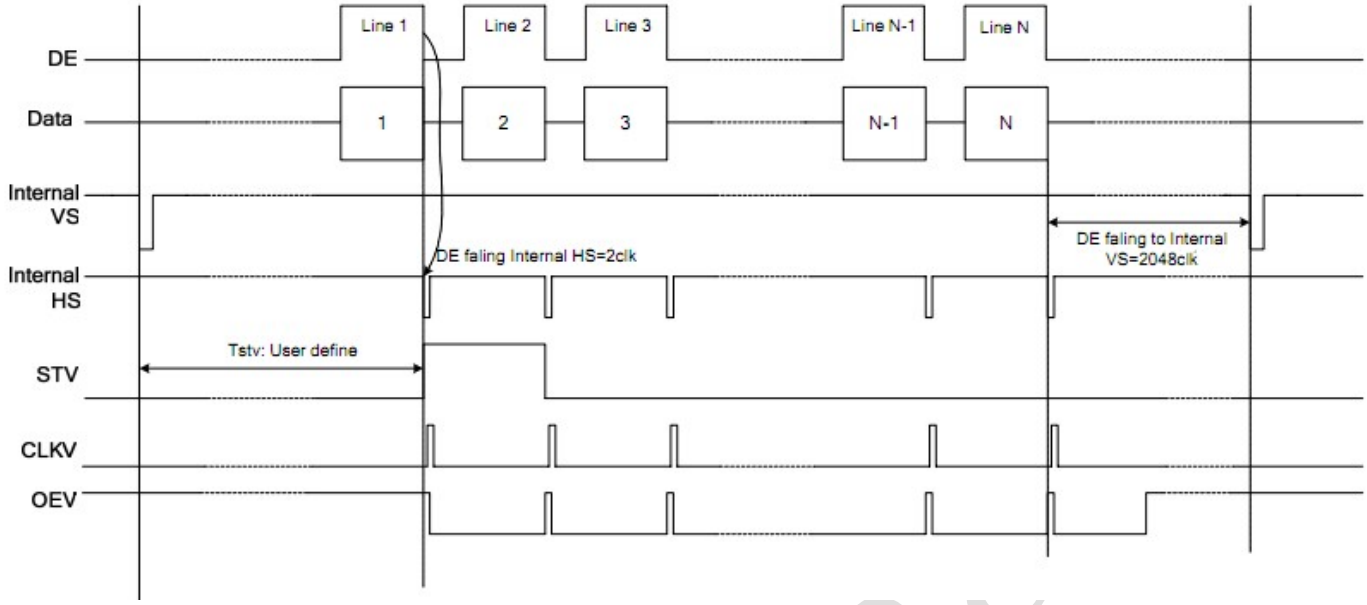
3-Wire Timing Diagram



Vertical Timing Diagram (HV Mode)



Vertical Timing Diagram (DE Mode)



3.3.4 Timing

8 Bit RGB 960 CH Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	27	30	MHz	VDD=3.0~3.6V
CLKIN cycle time	Tclk	-	37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1st data input(NTSC)	Ths	35	70	255	CLKIN	DDLY=70,Offset=0(fixed)

24 Bit RGB Mode (@ SEL[3:0]=1100 or 1101)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	6.1	6.4	8.0	MHz	VDD=3.0~3.6V
CLKIN cycle time	Tclk	125	156	164	ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1st data input(NTSC)	Ths	40	70	255	CLKIN	DDLY=70,Offset=0(fixed)

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
System Operation Timing						
VDD power source slew time	T_{POR}			1000	us	From 0V to 90% VDD
RSTB active pulse width	T_{RSTB}	40			us	VDD=3.3V
Input Output Timing						
CLKIN clock time	Tclk	-		35.7	ns	Please refer to timing table(P25)
HSD to CLKIN	Thc	-	-	1	CLKIN	
HSD width	Thwh	1	-	-	CLKIN	
VSD width	Tvwh	1	-	-	Th	
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
Data set-up time	Tdsu	12	-	-	ns	DIN[23:0] to CLKIN
Data hold time	Tdhd	12	-	-	ns	DIN[23:0] to CLKIN
DEN setup time	Tesd	12	-		ns	DEN to CLKIN
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@CIR601/8bit RGB HV mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	12	20	28	Th	@CCIR656 NTSC mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	17	25	33	Th	@CCIR656 PAL mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@24bit RGB HV mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Source output stable time 1	Tst	-	25	30	us	96% final, CL=30pF, RL=2K
Gate output stable time	Tgst	-	500	1000	ns	96% final, CL=40pF
VCOMOUT output stable time	Tcst	-	4	8	us	96% final, CL=33nF, RL=100ohm
3-wire serial communication AC timing						
Serial clock	Tspck	320	-	-	ns	
SPCK pulse duty	Tscdut	40	50	60	%	Tckh/Tspck
Serial data setup time	Tisu	120	-	-	ns	
Serial data hold time	Tihd	120	-	-	ns	
Serial clock high/low	Tssw	120	-	-	ns	
Chip select distinguish	Tcd	1	-	-	us	
SPENA to VSD	Tcv	1	-	-	us	
SPENB input setup time	Teck	150	-	-	Ns	
SPENB input hold time	Tcke	150	-	-	ns	

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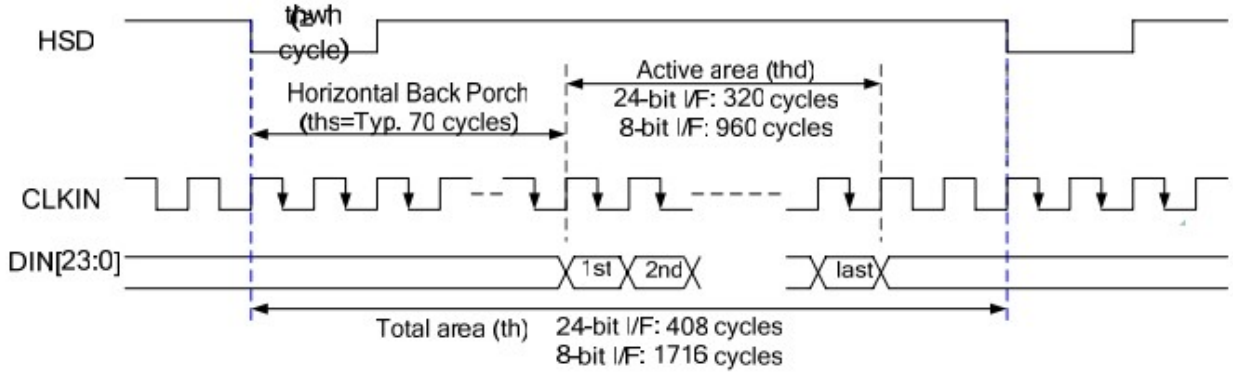
RGB (NTSC) input timing

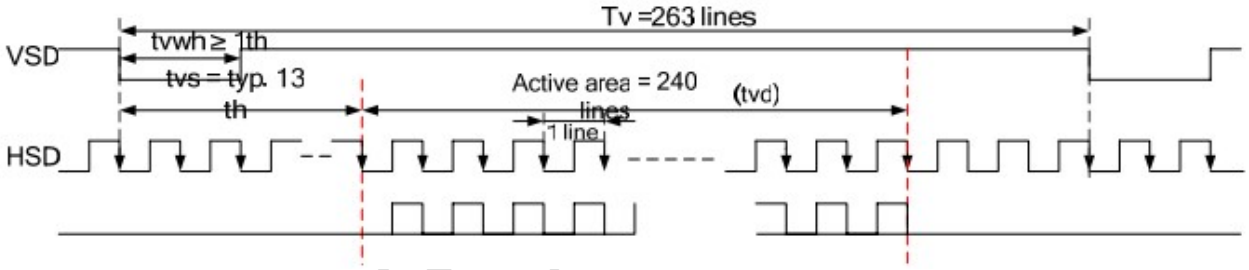
(1) HV mode timing: DE signal is not necessary, host float this pin.

Horizontal:

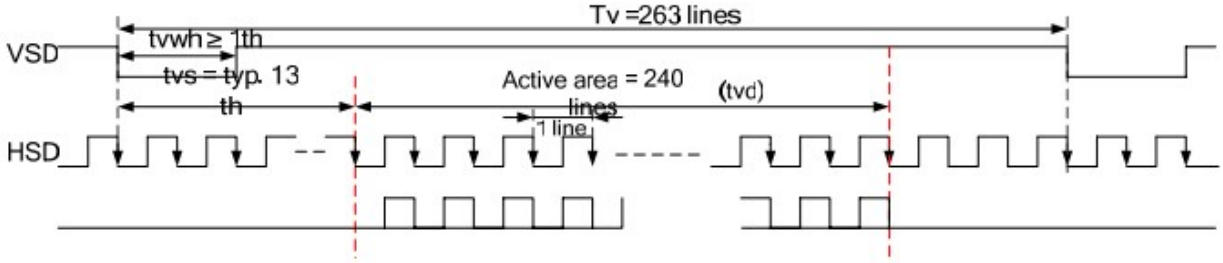
CLKIN frequency:
6.4MHz for 24bit mode
27MHz for 8bit mode



Vertical:

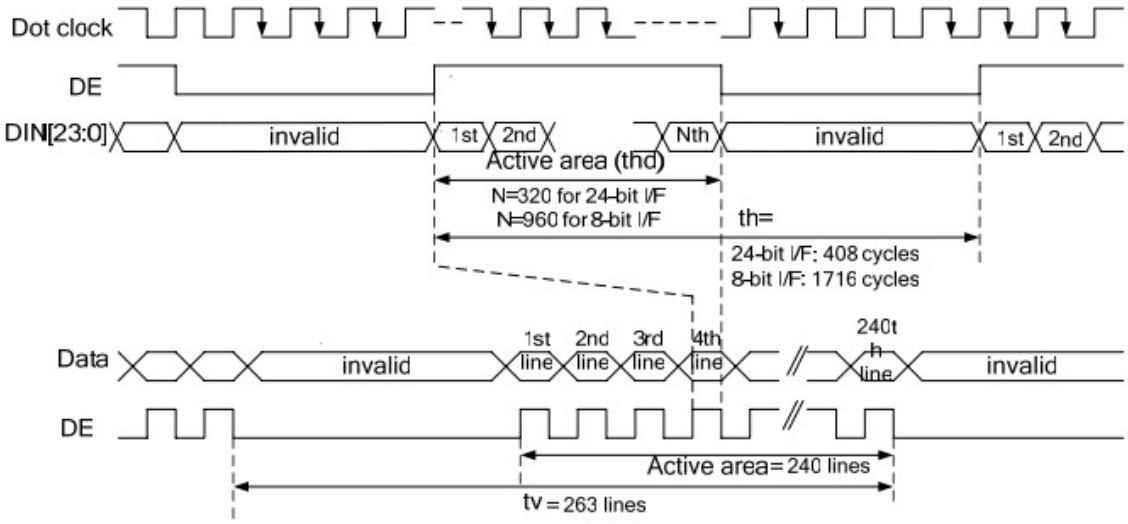


Vertical:



(2) DE mode: Hsync and Vsync are not needed in DE mode, host float these pins.

CLKIN frequency:
6.4MHz for 24bit mode
27MHz for 8bit mode



Notes:
(1) both CLKIN, HSD, VSD and DE supports active polarity selection. In the diagrams above, the VSD and HSD is low active, CLKIN samples data at negedge, DE is high active, and however, other kinds of polarity of these signals are also supported.
(2) signal relationship timing specification please refers the reference datasheet.

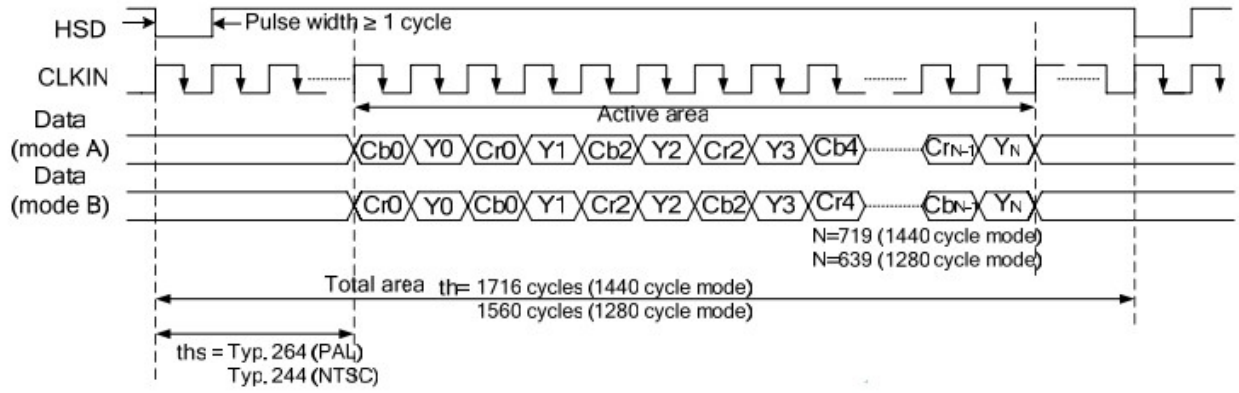
CCIR601 input timing

Features of the CCIR601 supported by this chip:

(1) only 8-bit I/F supported
(2) Both PAL and NTSC support. For PAL, both 280 and 288 lines supported
(3) Both 1440 and 1280 horizontal cycles are supported
(4) For all supported CCIR601 input format, the data sequence can be two types: mode A is Cb/Y/Cr/Y, mode B is Cr/Y/Cb/Y

Horizontal signal:

CLKIN frequency:
24.54MHz for 1280-cycle mode
27MHz for 1440-cycle mode



For CCIR601, 1 image frame = 1 odd field + 1 even field.
The odd/even filed is recognized by the inter relationship of Hsync and Vsync signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition

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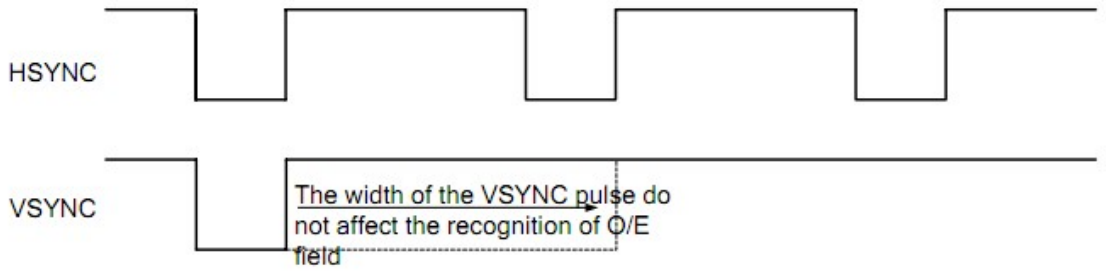
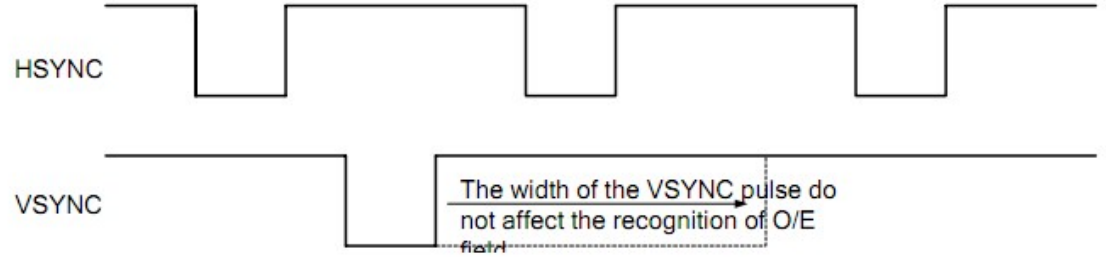
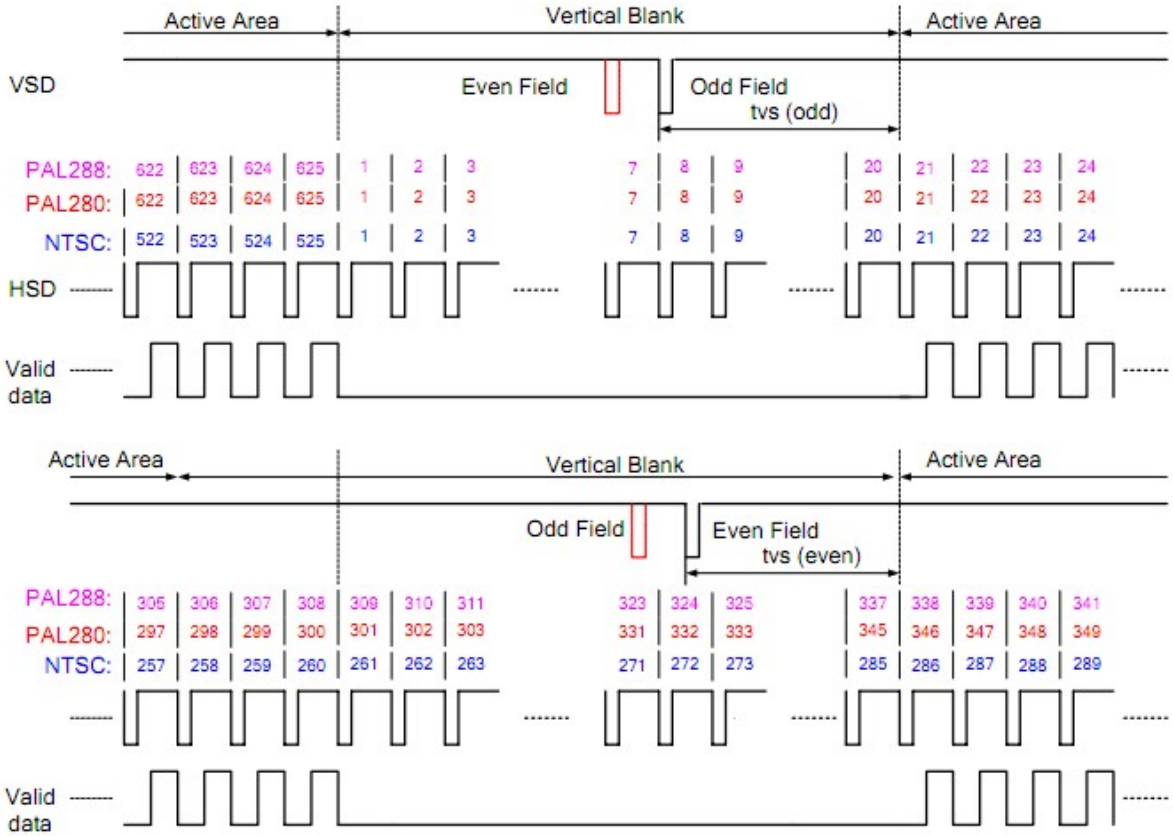
Odd Field



Even Fie



Vertical signal:

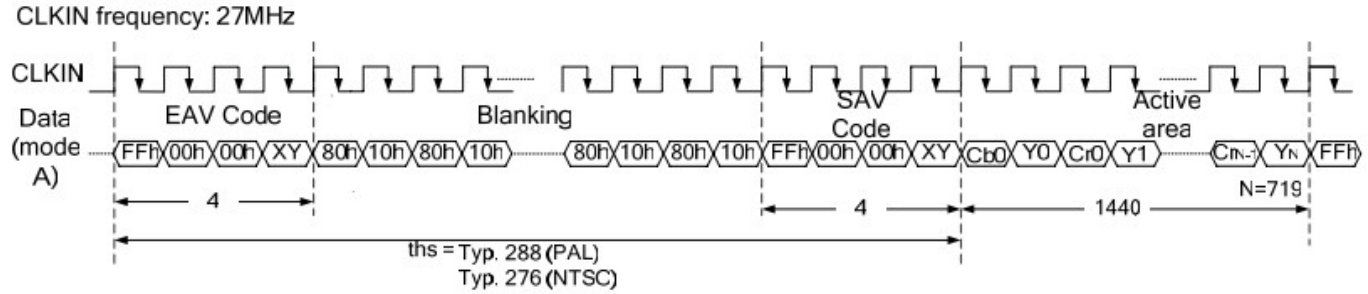


NTSC mode: active area=240 lines; PAL 280 mode: active area=280 lines; PAL 288 mode: active area=288 lines.

CCIR656 input timing

The CCIR656 use the YUV color encoding too. The difference of CCIR656 is that sync signals are embedded into the code stream. By this mode, VSD, HSD, DEN signals are not needed.

Horizontal:



EAV/SAV Format:

the "XY" byte in EAV/SAV plays a critical role for synchronization:

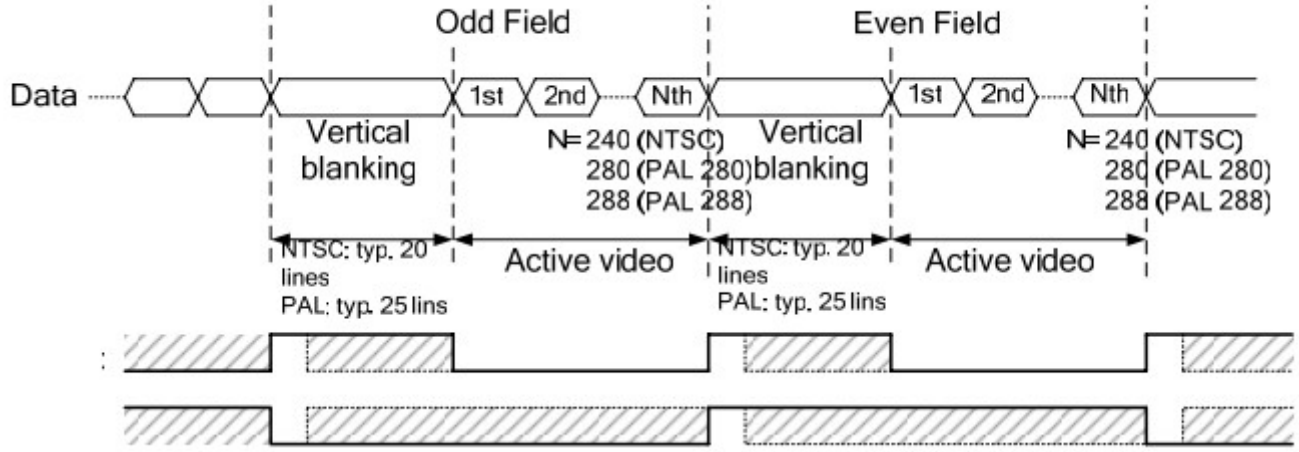
XY	B7	B6	B5	B4	B3	B2	B1	B0
EAV	1	F	V	H	Protection bits by ITU 656			
SAV	1	F	V	H	Protection bits by ITU 656			

F: Field bit. This is for vertical timing. F=0 indicates this is the line of the 1st field (odd field). F=1 indicates this is the line of the 2nd field (even field).

V: Vertical blanking bit. This is for vertical timing. V=1 indicates vertical blanking lines, V=0 indicates an active video line.

H: Horizontal recognizing bit. H=0: SAV, H=1: EAV.

Vertical:



3.4. Registers Table

Following table list the default 3-Wire control registers and bit name definition for NV3035C. Refer to the next section for detail register function description, please.

NV3035C 3-Wire Control Register List (Default)

3-Wire Registers		Register Description		
D[15:10]	Name	Init.	R/W	Function Description
000000b	R00	03h	R/W	System control register
000001b	R01	00h	R/W	Timing Controller function register
000010b	R02	03h	R/W	Operation control register
000011b	R03	8Ch	R/W	Input data Format control register
000100b	R04	46h	R/W	Source Timing delay control register
000101b	R05	0Dh	R/W	Gate Timing delay control register
000111b	R07	00h	R/W	Internal function control register
001000b	R08	08h	R/W	RGB Contrast control register
001001b	R09	40h	R/W	RGB Brightness control register
001011b	R0B	88h	R/W	R/B Sub-Contrast control register
001100b	R0C	20h	R/W	R Sub-Brightness control register
001101b	R0D	20h	R/W	B Sub-Brightness control register
001110b	R0E	2bh	R/W	VCOMDC Level Control Register
001111b	R0F	A5h	R/W	VCOMAC Level Control Register
010000b	R10	04h	R/W	VGAM2 level Control Register
010001b	R11	24h	R/W	VGAM3/4 level control register
010010b	R12	24h	R/W	VGAM5/6 level control register
011101b	R1D	00h	R/W	OTP operation control register
011110b	R1E	00h	R/W	OTP operation control register
011111b	R1F	00h	R/W	OTP operation control register

Pre

NV3035C 3-Wire Register Bit Definition (Default)

3-Wire Control Register Bit Map								
Reg.	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
R00	PAT3	PAT2	PAT1	PAT0	PWMPDB	X	STBYB	RESETB
R01	X	X	X	SWD2	SWD1	SWD0	DITHB	CFTYP
R02	SKIPMOD	HDNC1	HDNC0	X	FPOL	VSET	UPDN	SHLR
R03	DENPOL	CLKPOL	HSDPOL	VSDPOL	SEL3	SEL2	SEL1	SEL0
R04	DDLY7	DDLY6	DDLY5	DDLY4	DDLY3	DDLY2	DDLY1	DDLY0
R05	X	HDLY6	HDLY5	HDLY4	HDLY3	HDLY2	HDLY1	HDLY0
R07	FRAD1	FRAD[0]	INVSL[1]	INVSL[0]	PAL	PALM		AVGY
R08	X	X	X	CON4	CON3	CON2	CON1	CON0
R09	X	BRI6	BRI5	BRI4	BRI3	BRI2	BRI1	BRI0
R0A	HUE[3]	HUE[2]	HUE[1]	HUE[0]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
R0B	SCONB1	SCONB0			SCONR1	SCONR0		
R0C	X	X	SBRIR5	SBRIR4	SBRIR3	SBRIR2	SBRIR1	SBRIR0
R0D	X	X	SBRIB5	SBRIB4	SBRIB3	SBRIB2	SBRIB1	SBRIB0
R0E	X	OTP_BYPS	VCDCSL5	VCDCSL4	VCDCSL3	VCDCSL2	VCDCSL1	VCDCSL0
R0F	VGLSL1	VGLSL0	VGHSL1	VGHSL0	VCACSL3	VCACSL2	VCACSL1	VCACSL0
R10	X	X	X	GAMEN	X	V2GAM2	V2GAM1	V2GAM0
R11	X	X	V4GAM2	V4GAM1	V4GAM0	V3GAM2	V3GAM1	V3GAM0
R12	X	X	V6GAM2	V6GAM1	V6GAM0	V5GAM2	V5GAM1	V5GAM0
R1D	PDIN[7]	PDIN[6]	PDIN[5]	PDIN[4]	PDIN[3]	PDIN[2]	PDIN[1]	PDIN[0]
R1E	PPROG	PSWSL	PWE	POR	PTM[1]	PTM[0]	PA[1]	PA[0]
R1F								OTPSEL
R20							WNSEL[1]	WNSEL[0]

Note: Register function active at the falling edge of VSD except STBYB, RESETB register bits.

Registers list below require Vsync trigger:

DITHB, CFTYP, FPOL, VSET, UPDN, SHLR, DDLY, HDLY, INVSL, CON, BRI, HUE, SAT, SCONB, SCONR, SBRIR, SBRIB

Pr

R03: Input Data Format Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	DENPOL	1b	R/W	DEN input pin polarity control. DENPOL="0", DEN negative polarity. DENPOL="1", DEN positive polarity. (Default mode)
Bit[6]	CLKPOL	0b	R/W	CLKIN pin polarity control. CLKPOL="0", CLKIN negative edge latch data. CLKPOL="1", CLKIN positive edge latch data. (Default mode)
Bit[5]	HSDPOL	0b	R/W	HSD pin polarity control. HSDPOL="0", HSD negative polarity. (Default mode) HSDPOL="1", HSD positive polarity.
Bit[4]	VSDPOL	0b	R/W	VSD pin polarity control. VSDPOL="0", VSD negative polarity. (Default mode) VSDPOL="1", VSD positive polarity
Bit[3:0]	SEL[3:0]	1100b	(R) R/W	Input data format selection. Note: Different SEL[3:0] setting resolution in different AC timing.

SEL [3:0]: Data input mode

SEL3	SEL2	SEL1	SEL0	Data input format	Operating frequency
0	0	0	0	CCIR601 YUV 1280 input format（YUV mode A）	24.54MHz
0	0	0	1	CCIR601 YUV 1280 input format（YUV mode B）	24.54MHz
0	0	1	0	CCIR601 YUV 1440 input format（YUV mode A）	27MHz
0	0	1	1	CCIR601 YUV 1440 input format（YUV modeB）	27MHz
0	1	0	0	CCIR656 YCbCr input format（YCbCr mode A）	27MHz
0	1	0	1	CCIR656 YCbCr input format（YCbCr modeB）	27MHz
0	1	1	0	-	-
0	1	1	1	-	-
1	0	0	0	8-bit digital RGB input format HV Mode (NTSC only)	27MHz
1	0	0	1	8-bit digital RGB input format DE Mode (NTSC only)	27MHz
1	0	1	0	8-bit digital RGB through mode input format HV Mode (NTSC only)	27MHz
1	0	1	1	8-bit digital RGB through mode input format DE Mode (NTSC only)	27MHz
1	1	0	0	24-bit digital RGB input format HV Mode(NTSC only)	6.4MHz
1	1	0	1	24-bit digital RGB input format DE Mode(NTSC only)	6.4MHz
1	1	1	*	-	-

Note: Hsync and Vsync will be ignored in DE mode

Remark:RGB through mode will bypass 3-wire SWD[2:0] function; TCON will not arrange data color mapping.

Pr

4. Optical Specifications

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle		θT	CR≥10	40	50	-	degree	3
		θB		45	55	-		
		θL		50	60	-		
		θR		50	60	-		
Contrast Ratio		CR	Θ=0°	200	300	-	-	4
Color saturation		NTSC	CIE 1931	40	50	-	%	
Response Time		T_{on}+ T_{off}	25℃	-	25	50	ms	5
Chromaticity	White	X	LCM	-0.03	0.27	+0.03	-	1
		Y			0.30			
	Red	X		-0.03	0.624	+0.03		
		Y			0.368			
	Green	X			0.350			
		Y			0.550			
	Blue	X			0.143			
		Y			0.119			
Luminance (center)		L		350	400	-	cd/m^2	1
Luminance Uniformity		ΔL		75	80	-	%	1.2

Note：The parameter is slightly changed by temperature, driving voltage and materiel

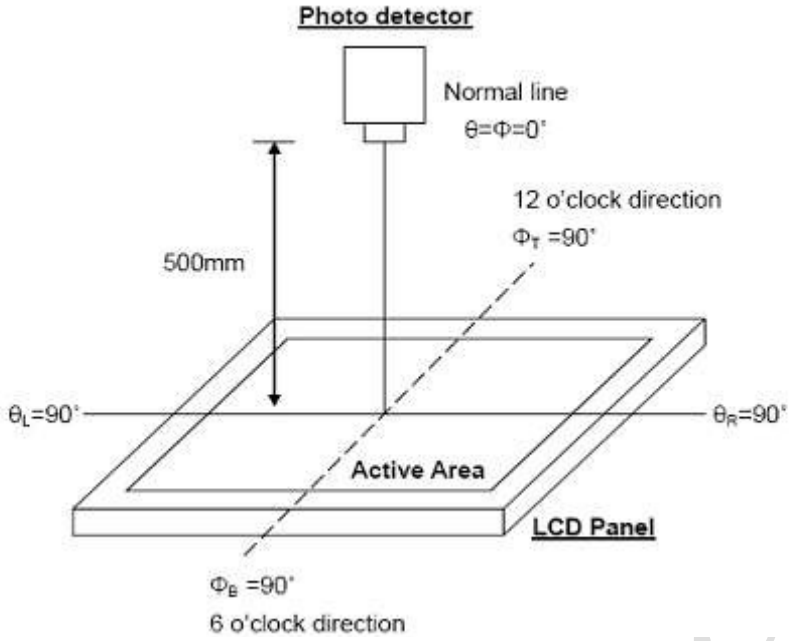
Note 1: The data are measured after LEDs are turned on for 3 minutes. LCM displays full white. The brightness is the average value of 5 measured spots. Measurement equipment BM-7 (Φ8mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

The measured value is more than 3 minutes at the center point of the LCD panel, and the backlight is turned on at the same time.

Preliminary

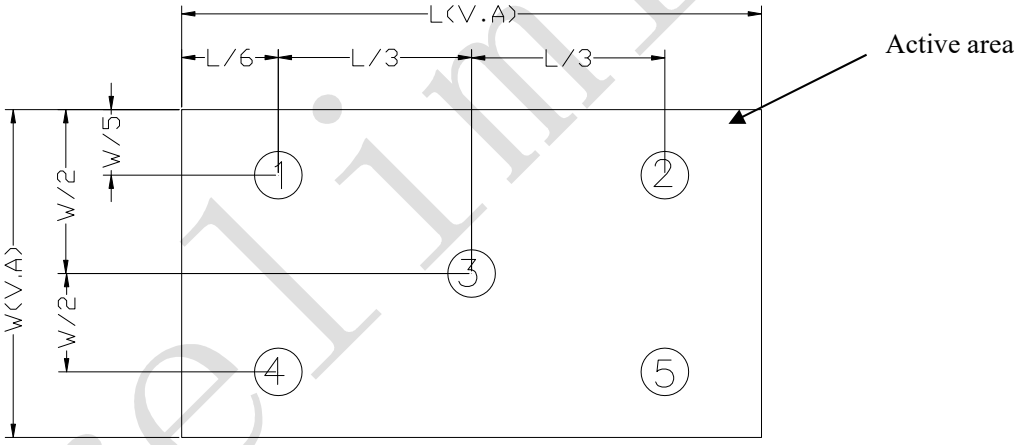


Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

Bp (Max.) = Maximum brightness in 5 measured spots

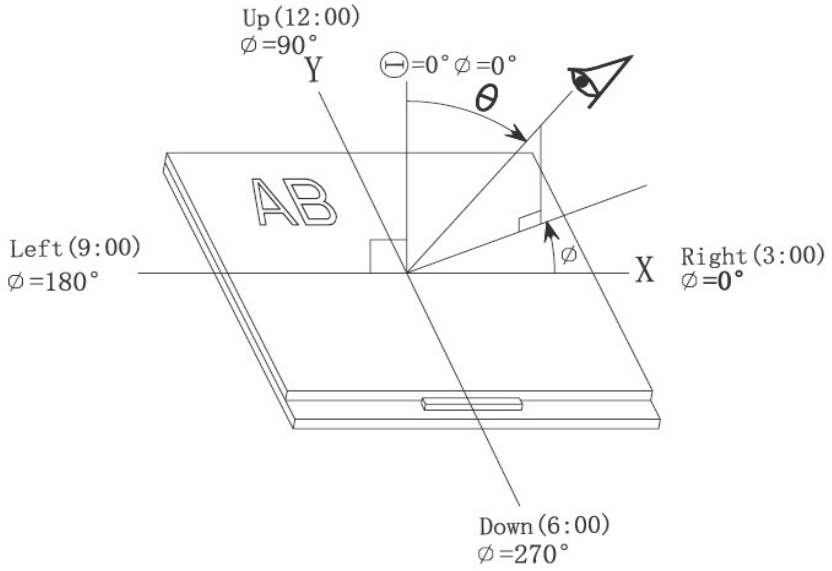
Bp (Min.) = Minimum brightness in 5 measured spots.



Note 3: The definition of viewing angle:

Refer to the graph below marked by θ and Φ

Preliminary



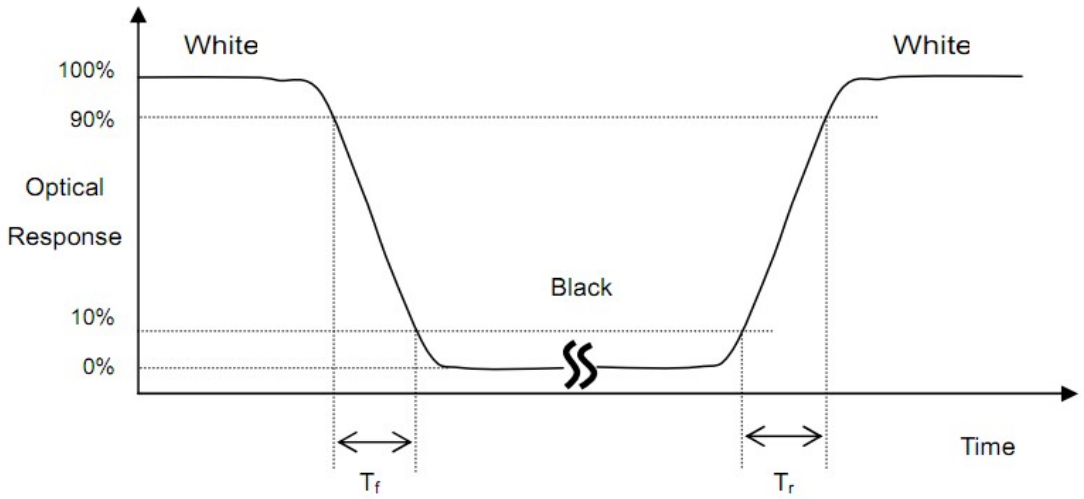
Note 4: Definition of contrast ratio

Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 5: Definition of Response time

The output signals of photo detector are measured when the input signals are changed from “white” to “black”(Tf) and from “black” to “white”(Tr), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



5. Reliability Test Items

Item	Test Conditions	Remark
High Temperature Storage	Ta=60℃; 120Hrs	Note1 ,Note4
Low Temperature Storage	Ta=-20℃; 120Hrs	Note1, Note4
High Temperature Operation	Ts=55℃; 120Hrs	Note2 ,Note4
Low Temperature Operation	Ts=-20℃; 120Hrs	Note4
Operation at High Temperature and Humidity	+50℃,90%RH; 120Hrs (no condensation)	Note4
Thermal Shock	-20℃/30min~+55℃/30min for a total 48 cycles	Start with cold temperature and end with high temperature
Package Drop Test	Height 40cm 1corner ， 3edges ， 6surfaces	
Elector Static Discharge	150pF/330Ω, Contact:±2KV,Air:±4KV	Human Body Mode
Image Sticking	25℃ ; 30min's	Note5

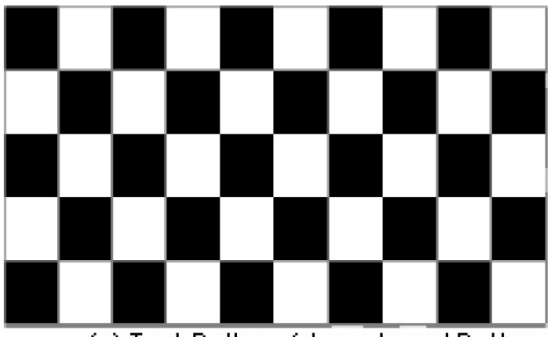
Note1: Ta is the ambient temperature of samples.

Note2: Ts is the temperature of panel's surfaces.

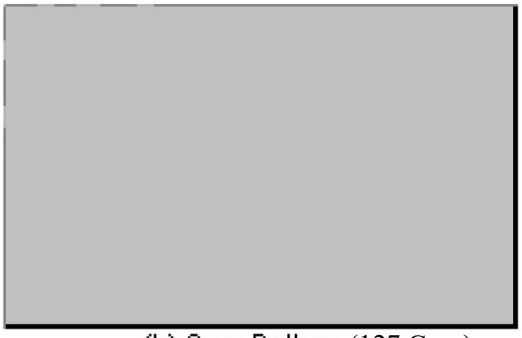
Note3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

Note4: before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note5: Condition of image sticking test :25℃±2℃, Operation with test pattern sustained for 30min's,then change to gray pattern immediately. After 5 min's, the Mura must be disappeared completely.



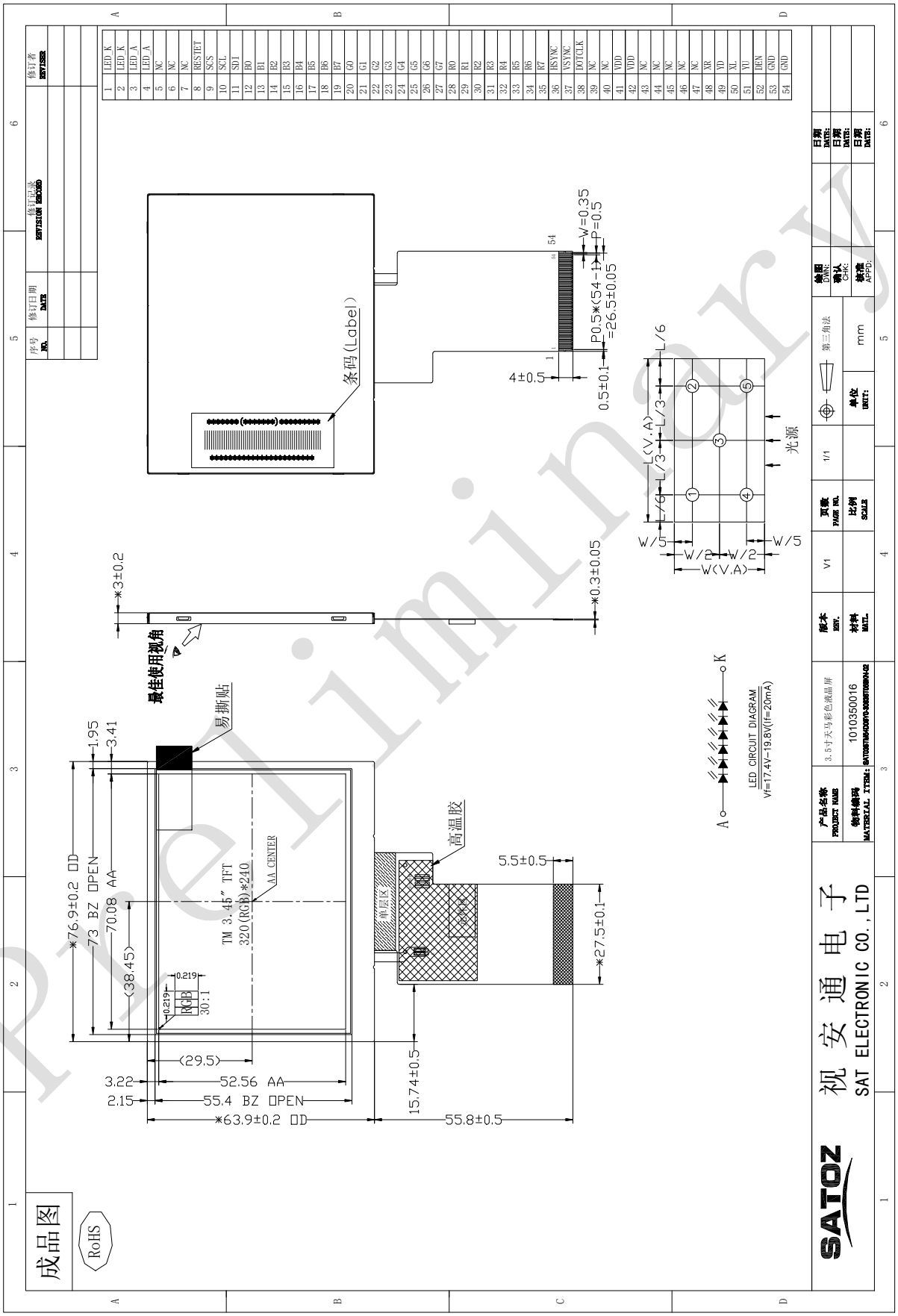
(a) Test Pattern (chess board Pattern)



(b) Gray Pattern (127 Gray)

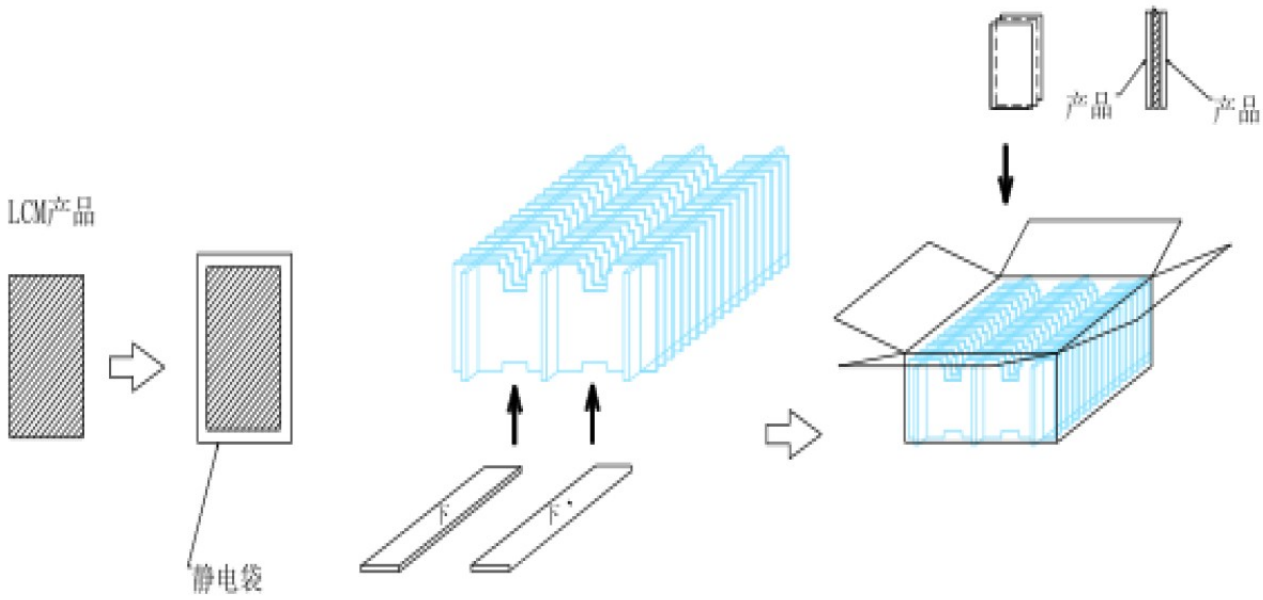
Preliminary

6. Mechanical Drawing



Preliminary

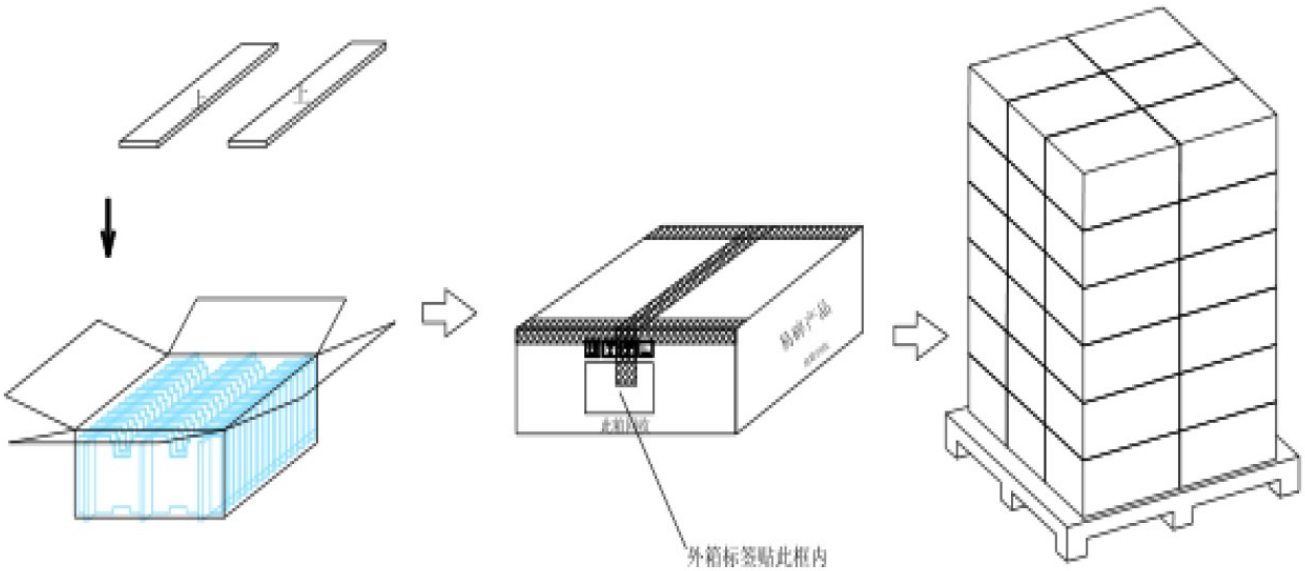
7. Package Drawing



第一步：
LCM产品装入静电袋

第二步：
把长卡，短卡组成卡阵（短卡朝向一致）
形状和数量按照 BOM 实际物料
卡阵底部放对应的　线刀卡后装箱

第三步：
放产品，每个卡槽内放两片产品；
2PCS 产品显示面相对，



第四步：
装箱后，按照BOM实际物料在纸箱内

第五步：
最后胶带封箱，贴外箱标签

第六步：
将每箱整齐摆放在栈板上并包裹
最高可堆叠6层

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