PE42723

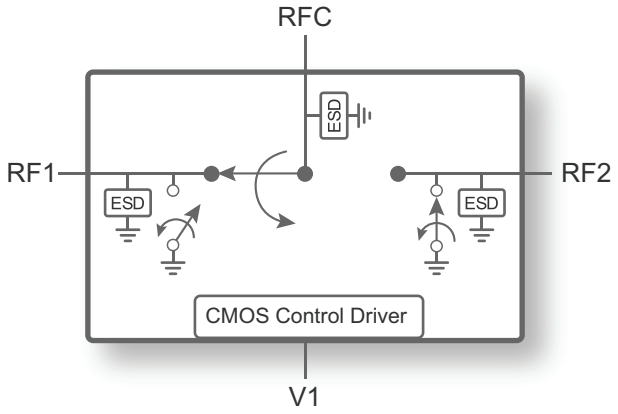
Document Category: Product Specification

UltraCMOS® SPDT RF Switch, 5–1794 MHz

Features

- Supports DOCSIS 3.0/1 requirements
- Exceptional harmonics:
  - 2fo of –121 dBc at 17 MHz
  - 3fo of –140 dBc at 17 MHz
- Best-in-class linearity across the frequency band
- Low insertion loss and high isolation performance:
  - Insertion loss: 0.3 dB at 1218 MHz
  - Isolation: 54 dB at 204 MHz
- High ESD performance: 3 kV HBM
- Packaging: 12-lead 3 × 3 × 0.75 mm QFN

Figure 1 • PE42723 functional diagram



Applications

- Broadband market (DOCSIS 3.0/1):
  - Cable modems
  - Set-top boxes
  - Residential gateways
- Filter bank switching
- Relay replacement between DOCSIS 3.0 and DOCSIS 3.1 configurations

Product description

The PE42723 is a HaRP™ technology-enhanced reflective SPDT RF switch designed for use in cable applications, including DOCSIS 3.0/1 cable modems, set-top boxes, and residential gateways. It delivers high linearity and excellent harmonics performance in the 5–1794 MHz band. It also features low insertion loss and high isolation performance, making the PE42723 ideal for DOCSIS 3.1 applications.

The PE42723 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

©2015–2026, pSemi Corporation. All rights reserved. • Headquarters: 9369 Carroll Park Drive, San Diego, CA, 92121

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in **Table 1** could cause permanent damage. Restrict operation to the limits in **Table 2**. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in **Table 1**.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • PE42723 absolute maximum ratings

Parameter or condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Digital input voltage, V1	–0.3	3.6	V
RF input power, 75Ω	–	86	dBmV
Storage temperature range	–65	+150	°C
ESD voltage HBM(1), all pins	–	3000	V
ESD voltage CDM(2), all pins	–	500	V

Notes:
1) Human body model (MIL-STD 883 Method 3015).
2) Charged device model (JEDEC JESD22-C101).

Recommended operating conditions

Table 2 lists the PE42723 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2 • PE42723 recommended operating conditions

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	2.3	3.3	5.5	V
Supply current, I_{DD}	–	130	200	µA
Digital input high, V1	1.17	–	3.6(1)	V
Digital input low, V1	–0.3	–	0.6	V
RF input power, CW(2)	–	–	80	dBmV
RF input power, peak(3)	–	–	85	dBmV
Operating temperature range	–40	+25	+85	°C

Notes:
1) The maximum digital input voltage is limited to V_{DD} and cannot exceed 3.6V.
2) 100% duty cycle, 75Ω.
3) OFDMA DOCSIS 3.1, single channel, 75Ω.

Electrical specifications

Table 3 lists the PE42723 key electrical specifications at +25 °C, V_{DD} = 3.3V, and $Z_S = Z_L$ = 75Ω, unless otherwise specified.

Table 3 • PE42723 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	5	–	1794	MHz
Insertion loss[1]	RFC–RFx	5–204 MHz 204–1218 MHz 1218–1794 MHz	–	0.10 0.30 0.40	0.20 0.45	dB dB dB
Isolation	All paths	5–204 MHz 204–612 MHz 612–1218 MHz 1218–1794 MHz	50 40 36	54 44 38 34	–	dB dB dB dB
Return loss[1]	RFC–RFx	5–204 MHz 204–612 MHz 612–1218 MHz 1218–1794 MHz	25 18	30 22 14 13	–	dB dB dB dB
Second harmonic, 2fo	RFx	fo = 17 MHz, average P_{CW} = 65 dBmV fo = 170 MHz, average P_{CW} = 65 dBmV fo = 900 MHz, average P_{CW} = 65 dBmV	–	–121 –121 –121	–	dBc dBc dBc
Third harmonic, 3fo	RFx	fo = 17 MHz, average P_{CW} = 65 dBmV fo = 170 MHz, average P_{CW} = 65 dBmV fo = 900 MHz, average P_{CW} = 65 dBmV	–	–140 –132 –135	–	dBc dBc dBc
Input 0.1-dB compression point[2]	RFC–RFx	5–1218 MHz	–	87	–	dBmV
Switching time	–	50% CTRL to 90% or 10% RF	–	35	–	µs

Notes:
1) High-frequency performance can be improved by external matching. For details, see **Figure 12–Figure 15**.
2) The input 0.1-dB compression point is a linearity figure of merit. For the operating RF input power (75Ω), see **Table 2**.

Switching frequency

The PE42723 has a maximum 10-kHz switching frequency. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spurious performance

The PE42723 spur fundamental occurs around 10 MHz. Its typical performance is –154 dBm/Hz (V1 = H) and –165 dBm/Hz (V1 = L), with 100-kHz bandwidth.

Thermal data

Psi-JT (Ψ_{JT}), the junction top-of-package, is a thermal metric to estimate the junction temperature of a device on an application PCB (JEDEC JESD51-2).

$\Psi_{JT} = (T_J - T_T)/P$

where:

- **Ψ_{JT} = Junction-to-top of package characterization parameter in °C/W**
- **T_J = Die junction temperature in °C**
- **T_T = Package temperature (top surface, in the center) in °C**
- **P = Power dissipated by the device in Watts**

Table 4 • PE42723 thermal data

Parameter	Typ	Unit
Maximum junction temperature, T_{JMAX} (RF input power, CW = 80 dBmV, +85°C ambient)	90	°C
Ψ_{JT}	21	°C/W

Control logic

Table 5 lists the PE42723 control logic truth table.

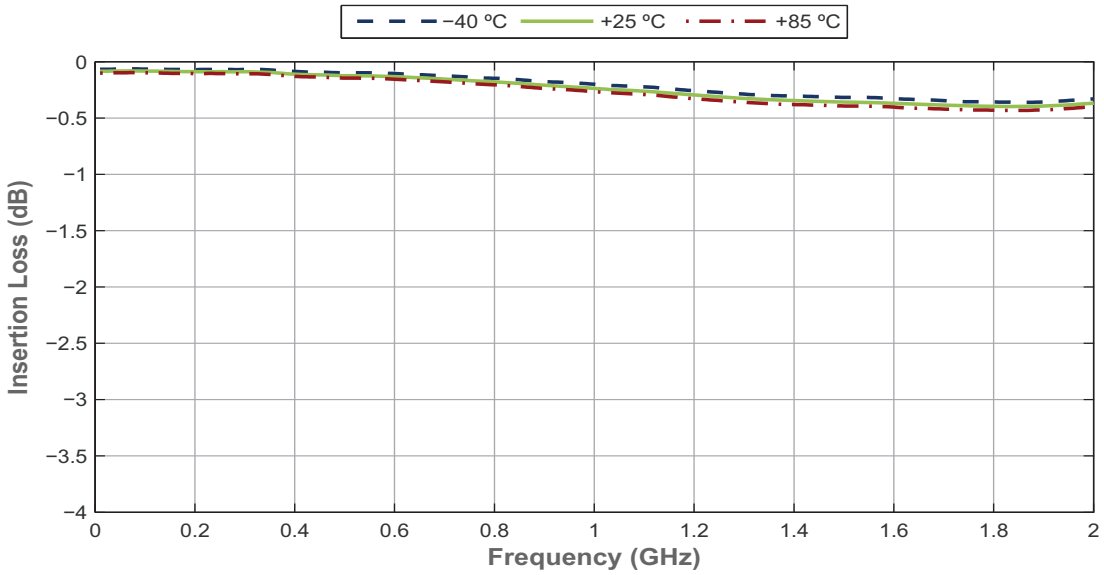
Table 5 • PE42723 truth table

State	V1
RFC–RF1	H
RFC–RF2	L

Typical performance data

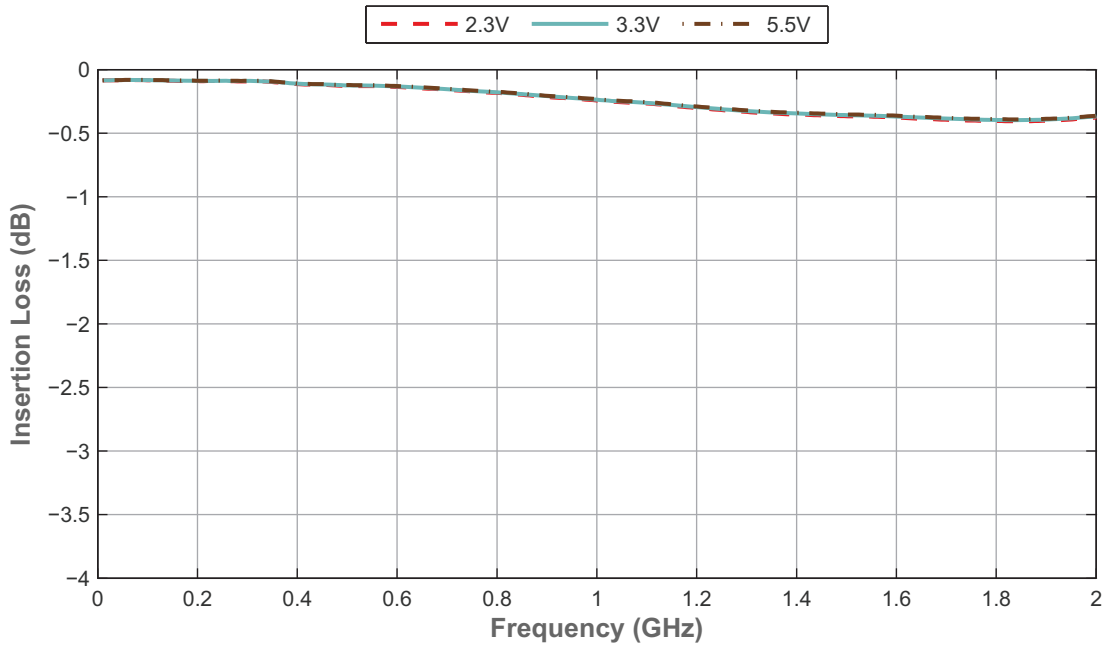
Figure 2–Figure 11 show the typical performance data at +25 °C, V_{DD} = 3.3V, and Z_S = Z_L = 75Ω, unless otherwise specified.

Figure 2 • Insertion loss vs. temperature (RFC–RFx)(*)



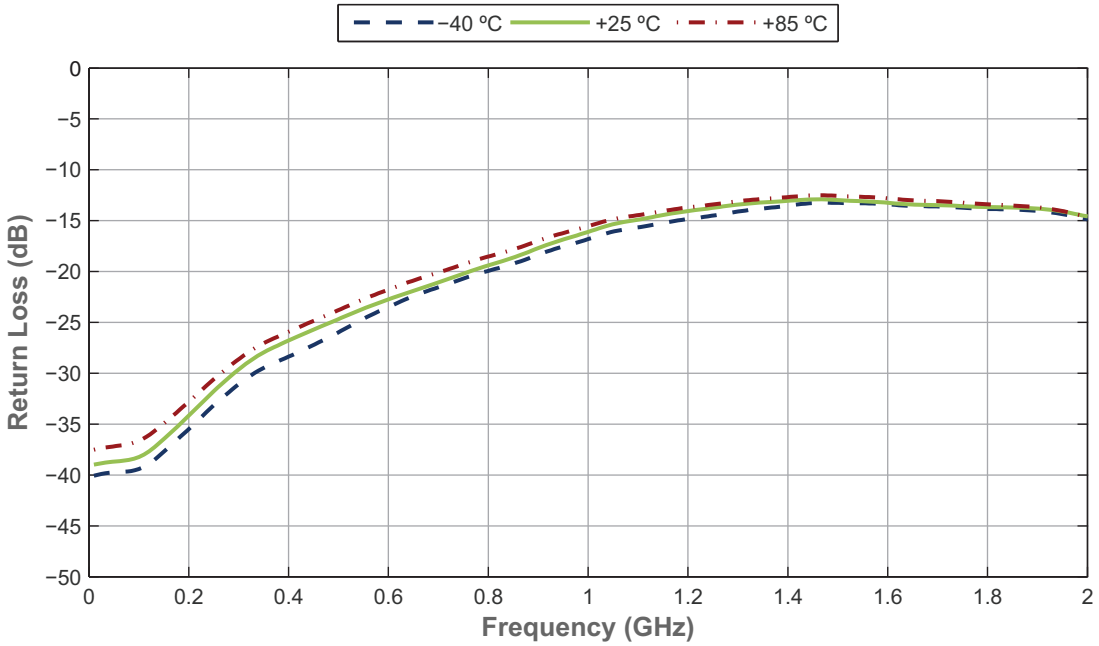
Note: * High frequency performance can be improved by external matching (see **Figure 12–Figure 15**).

Figure 3 • Insertion loss vs. V_{DD} (RFC–RFx)(*)



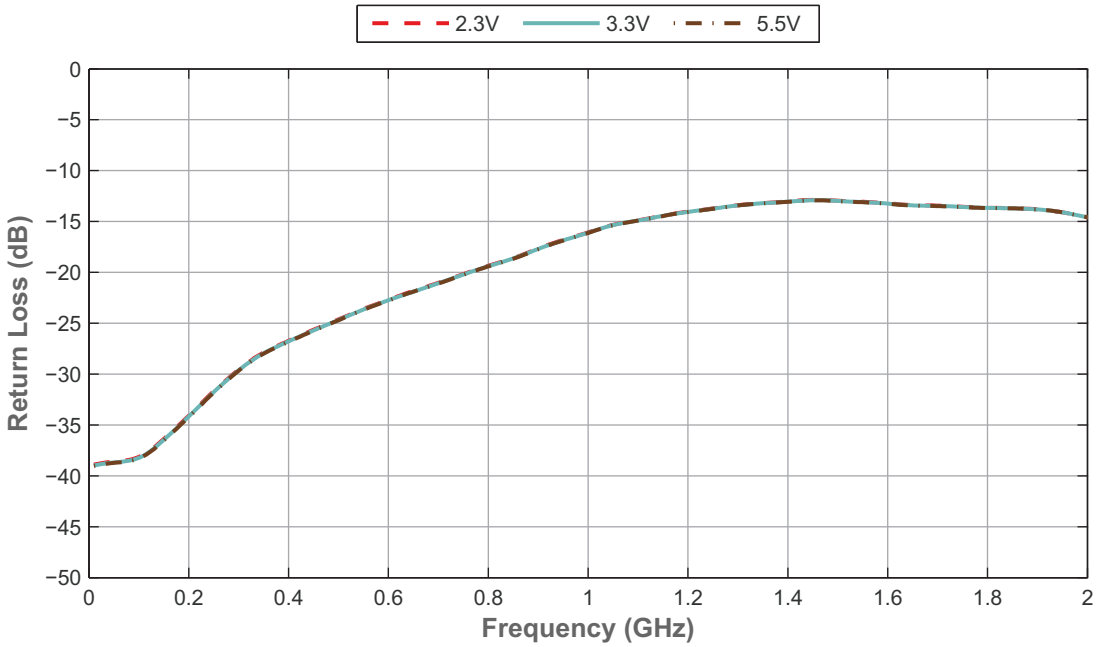
Note: * High frequency performance can be improved by external matching (see **Figure 12–Figure 15**).

Figure 4 • RFC port return loss vs. temperature(*)



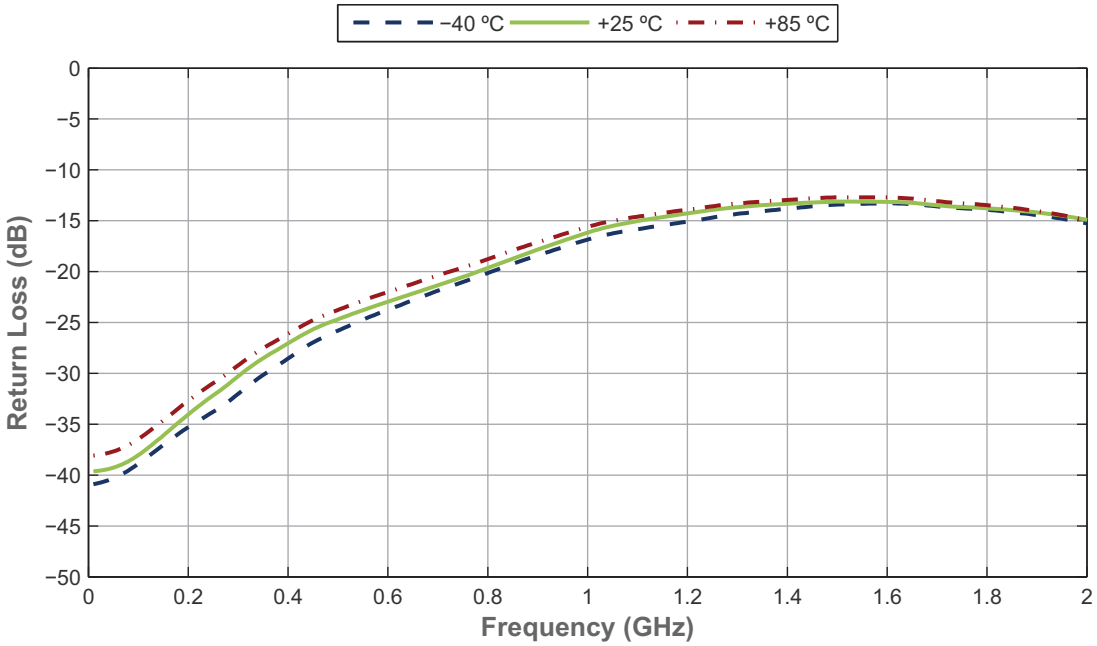
Note: * High frequency performance can be improved by external matching (see **Figure 12–Figure 15**).

Figure 5 • RFC port return loss vs. V_{DD}(*)



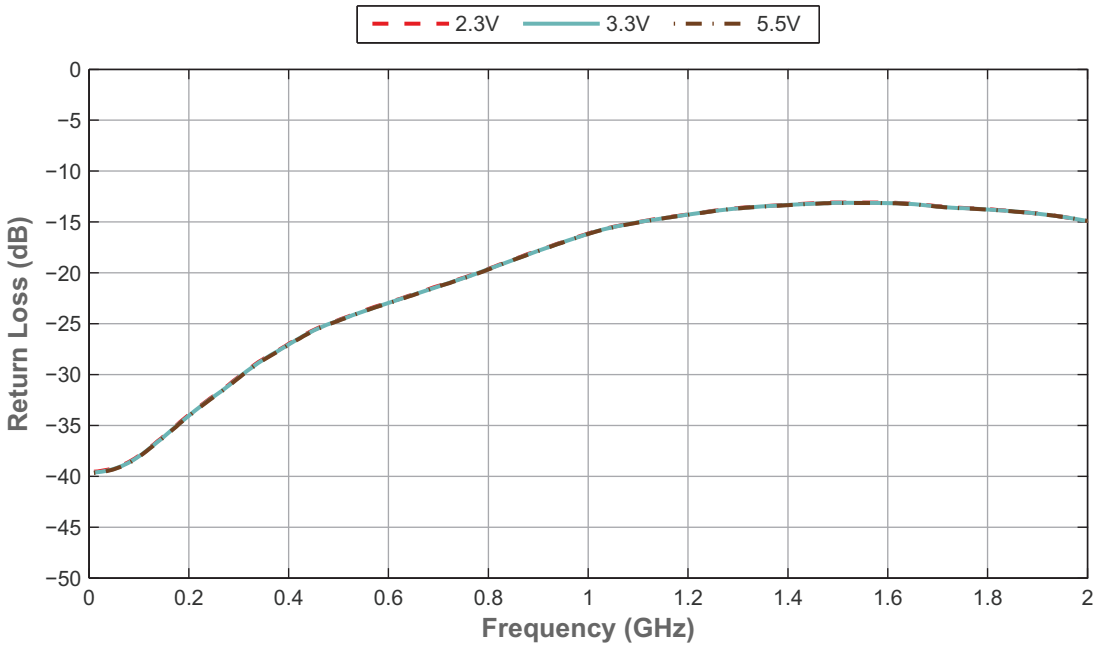
Note: * High frequency performance can be improved by external matching (see **Figure 12–Figure 15**).

Figure 6 • Active port return loss vs. temperature(*)



Note: * High frequency performance can be improved by external matching (see **Figure 12–Figure 15**).

Figure 7 • Active port return loss vs. V_{DD}(*)



Note: * High frequency performance can be improved by external matching (see **Figure 12–Figure 15**).

Figure 8 • Isolation vs. temperature (RFx–RFx)

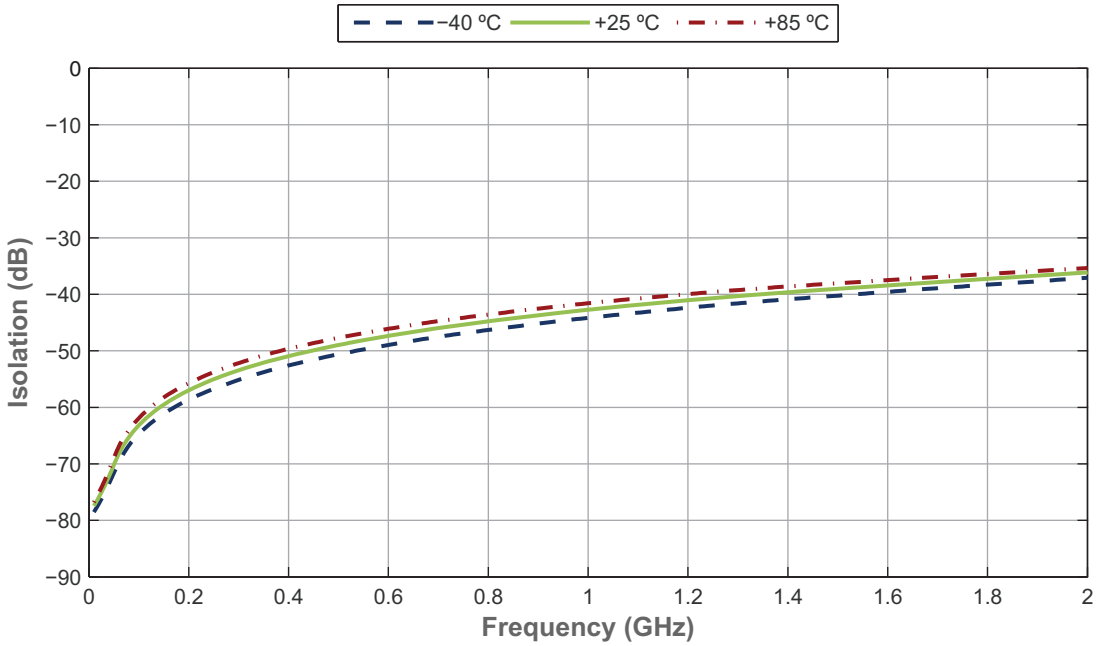


Figure 9 • Isolation vs. V_{DD} (RFx–RFx)

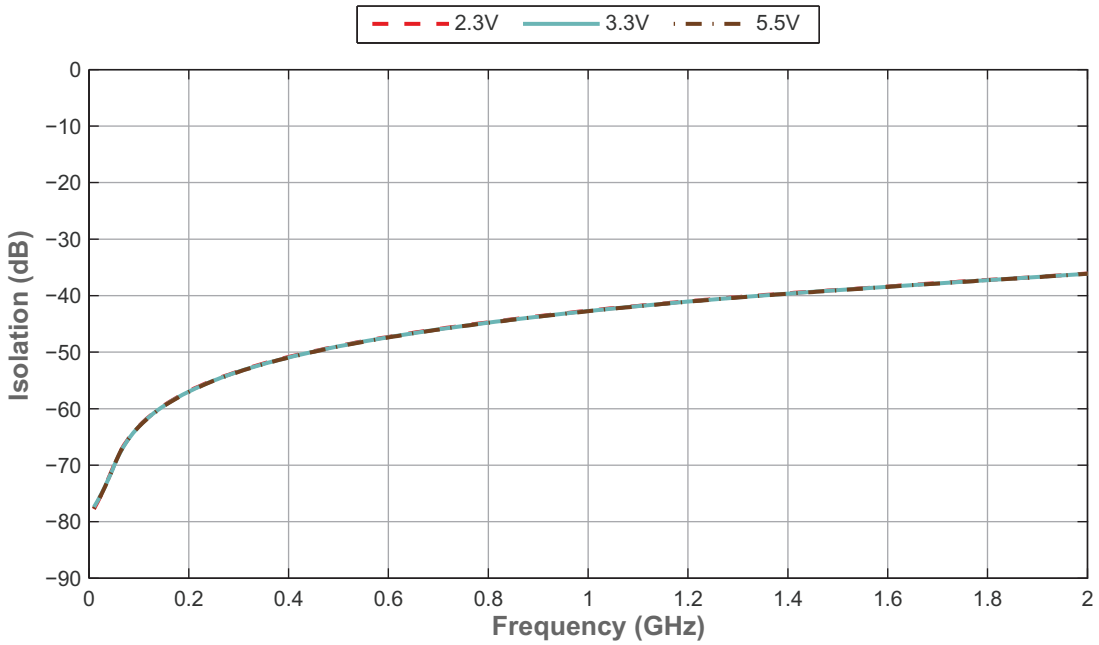


Figure 10 • Isolation vs. temperature (RFC–RFx)

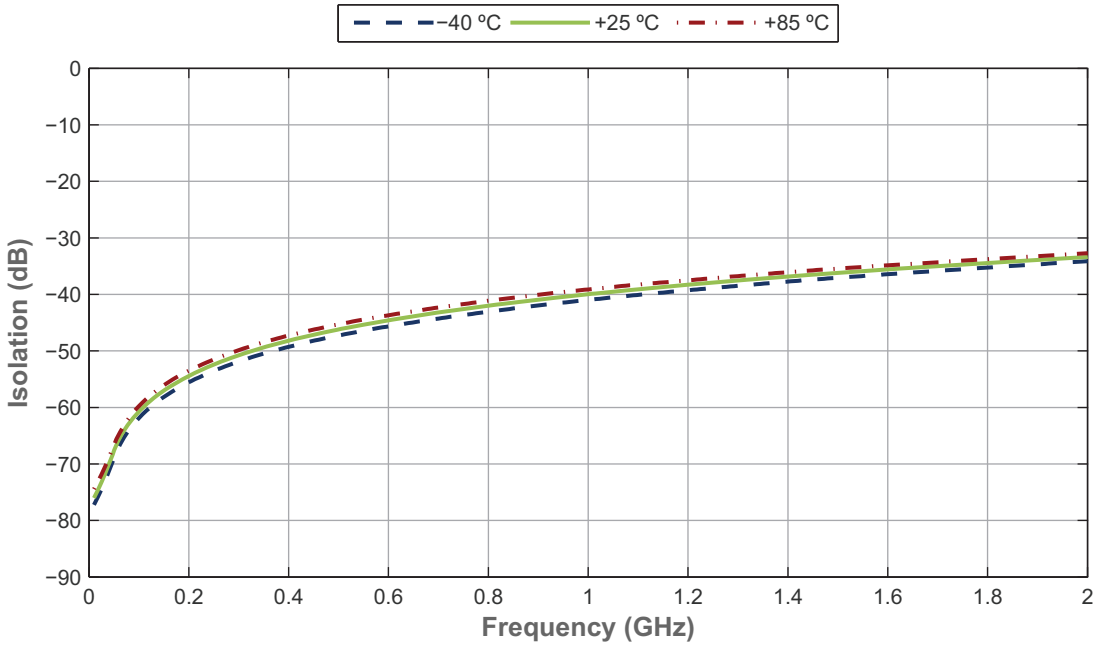
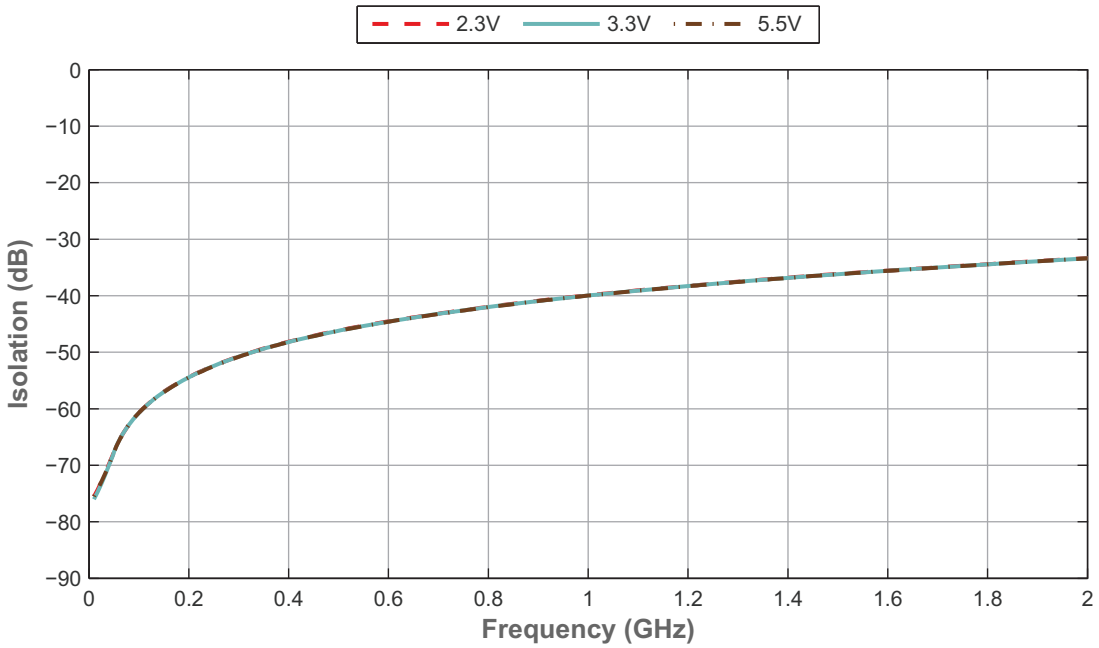


Figure 11 • Isolation vs. V_{DD} (RFC–RFx)



High-frequency performance with external matching

To improve high-frequency insertion loss and return loss, use inductive matching on the RF ports in your application board layout. **Figure 12** shows a matching network using a 2.2 nH inductor on each RF port. The inductor must be placed as close to the device under test (DUT) as possible. **Figure 13–Figure 15** show the insertion loss and return loss improvement using a 2.2 nH inductor on the RF1, RF2, and RFC ports, respectively.

Figure 12 • PE42723 matching network

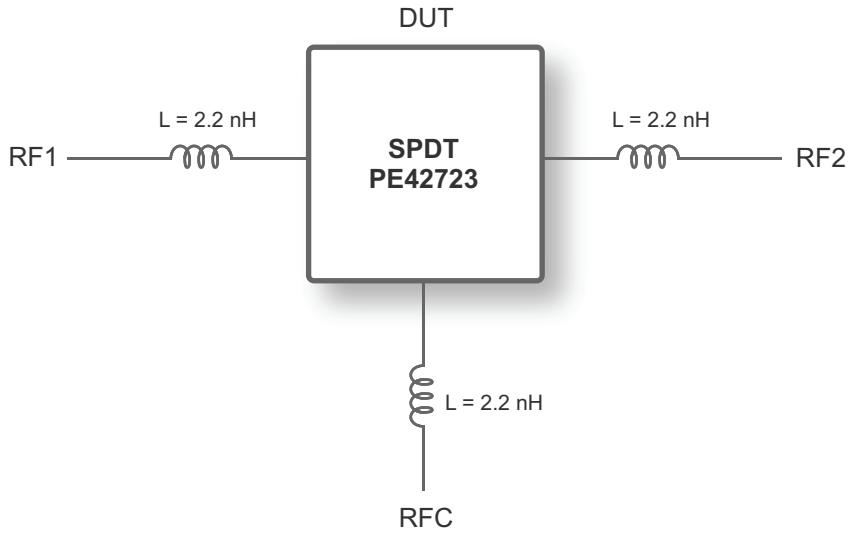
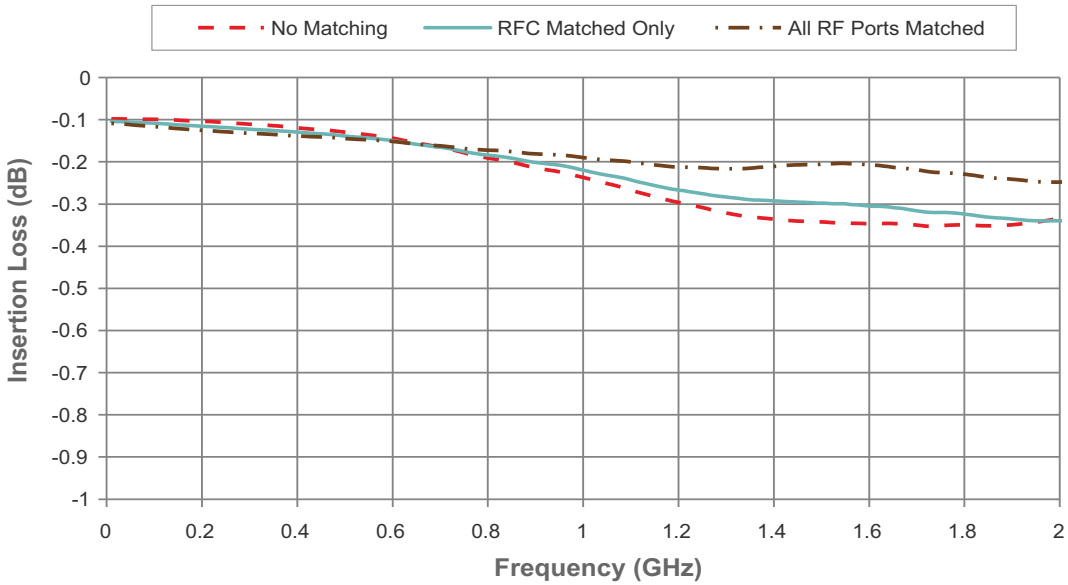
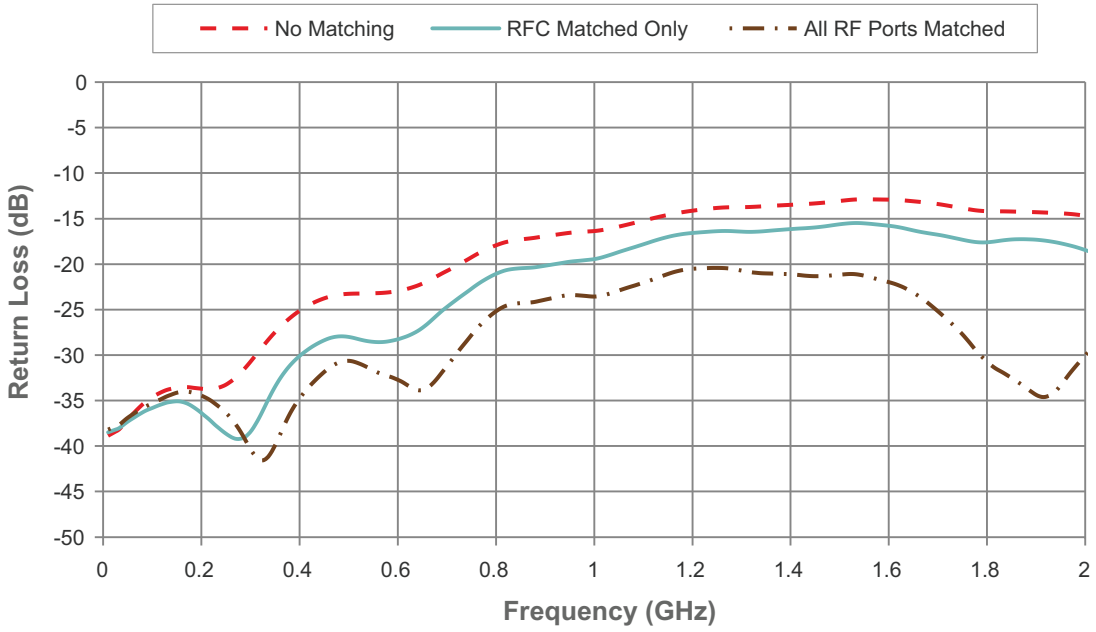


Figure 13 • Insertion loss (RFC–RFx) with and without matching(*)



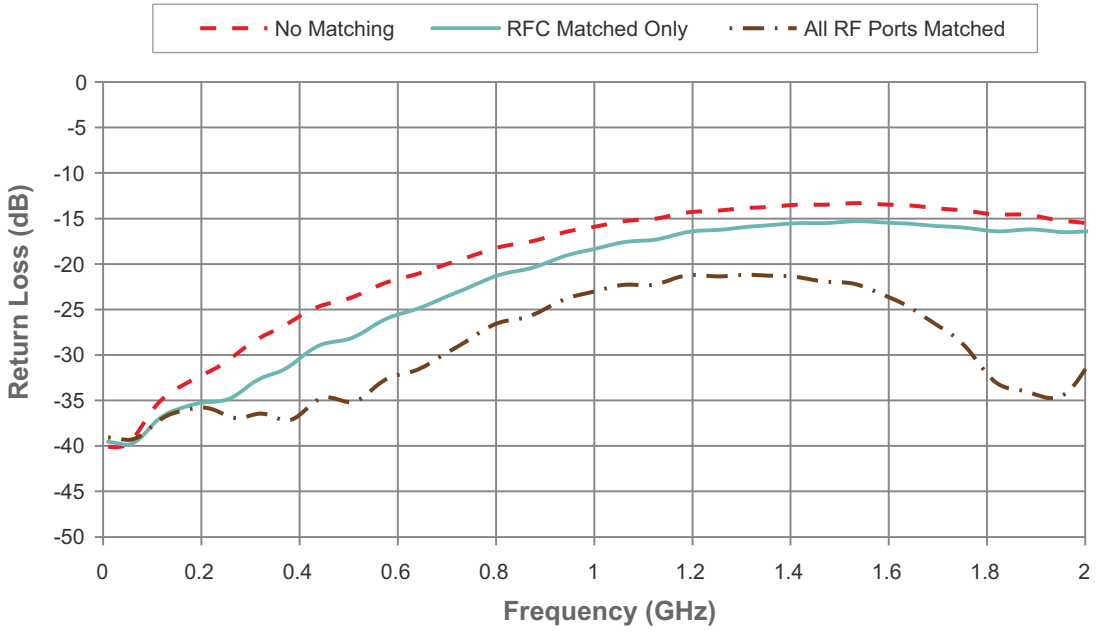
Note: * For reference only.

Figure 14 • RFC port return loss with and without matching(*)



Note: * For reference only.

Figure 15 • Active port return loss with and without matching(*)

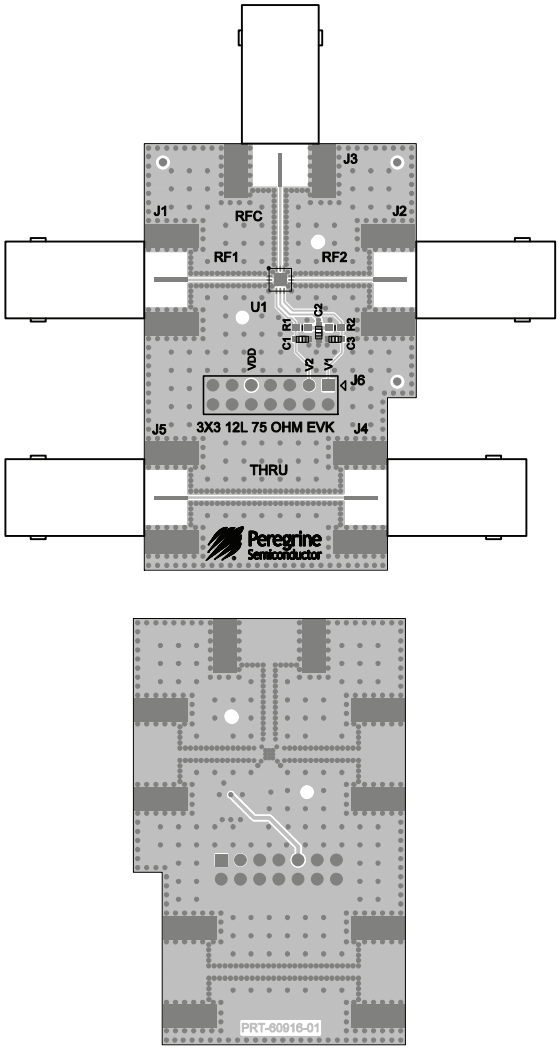


Note: * For reference only.

Evaluation kit

pSemi designed the PE42723 evaluation board to ease your evaluation of the PE42723 RF switch. The RF common port (RFC) connects through a 75Ω transmission line via the F-Type connector, J3. The RF1 and RF2 ports connect through 75Ω transmission lines via F-type connectors J1 and J2, respectively. A 75Ω through transmission line is available via F-type connectors J4 (THRU left) and J5 (THRU right), which you can use to de-embed the loss of the PCB. J6 provides DC and digital inputs to the device.

Figure 16 • PE42723 evaluation board layout



Pin configuration

Figure 17 shows the PE42723 pin map for the 12-lead 3 × 3 × 0.75 mm QFN package, and **Table 6** lists the description for each pin.

Figure 17 • Pin configuration, top view

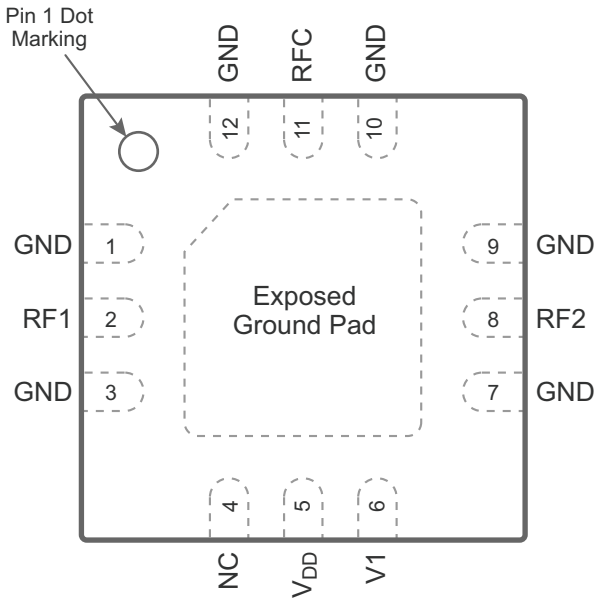


Table 6 • PE42723 pin descriptions

Pin no.	Pin name	Description
1, 3, 7, 9, 10, 12	GND	Ground
2	RF1(*)	RF port 1
4	NC	Do not connect
5	V_{DD}	Supply voltage (nominal 3.3V)
6	V1	Digital control logic input 1
8	RF2(*)	RF port 2
11	RFC(*)	RF common port
Pad	GND	Exposed pad. Ground for proper operation.

Note: * RF pins 2, 8, and 11 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Packaging information

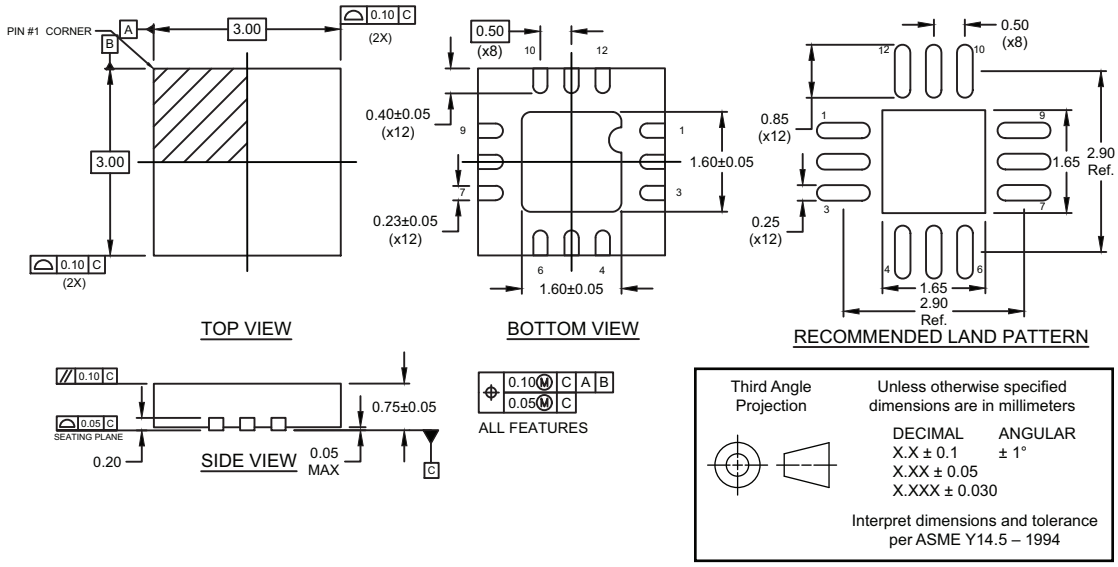
This section provides the PE42723 packaging data, including the moisture sensitivity level, package drawing, package marking, and tape-and-reel information.

Moisture sensitivity level

The PE42723 moisture sensitivity level rating for the 12-lead 3 × 3 × 0.75 mm QFN package is MSL1.

Package drawing

Figure 18 • Package mechanical drawing for the 12-lead 3 × 3 × 0.75 mm QFN package



Top-marking specification

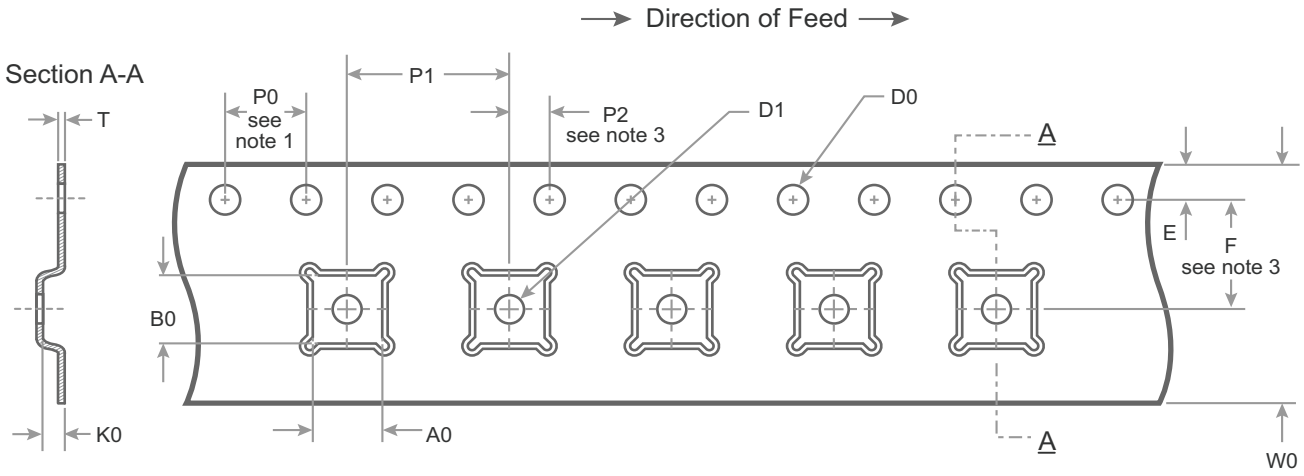
Figure 19 • PE42723 package marking specifications



● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Tape and reel specification

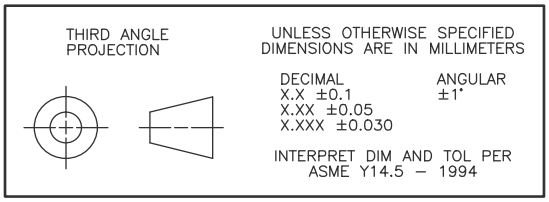
Figure 20 • Tape and reel specification for the 12-lead 3 × 3 × 0.75 mm QFN package

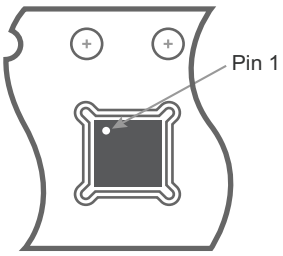


A0	3.30
B0	3.30
K0	1.10
D0	1.50 + 0.1/ -0.0
D1	1.5 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.3

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole





Device Orientation in Tape

Ordering information

Table 7 lists the PE42723 ordering codes and shipping methods.

Table 7 • PE42723 order codes and shipping methods

Order code	Description	Packaging	Shipping method
PE42723A-Z	PE42723 SPDT RF switch	12-lead 3 × 3 × 0.75 mm QFN	3000 units/T&R
EK42723-01	PE42723 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent statement

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and trademark

©2015–2026, pSemi Corporation. All rights reserved. The Peregrine Semiconductor name, Peregrine Semiconductor logo and UltraCMOS are registered trademarks and the pSemi name, pSemi logo, HaRP and DuNE are trademarks of pSemi Corporation in the U.S. and other countries.