PE42521

Document category: Product Specification

UltraCMOS® SPDT RF Switch, 9 kHz–13 GHz

Features

- HaRP™ technology enhanced:
  - Fast settling time: 2 ms
  - No gate or phase lag
  - No drift in insertion loss and phase
- Fast switching time: 500 ns
- High power handling @ 4 GHz in 50Ω:
  - 36 dBm CW
  - 38.5 dBm instantaneous power
  - 26 dBm terminated port
- High linearity: 65 dBm IIP3
- Low insertion loss:
  - 0.75 dB @ 3 GHz
  - 1.15 dB @ 10 GHz
  - 1.85 dB @ 13 GHz
- High isolation:
  - 44 dB @ 3 GHz
  - 30 dB @ 10 GHz
  - 17 dB @ 13 GHz
- ESD performance:
  - 3 kV HBM on RF pins to GND
  - 1.5 kV HBM on all pins
  - 1 kV CDM on all pins
- Packaging: 16-lead 3 × 3 mm QFN

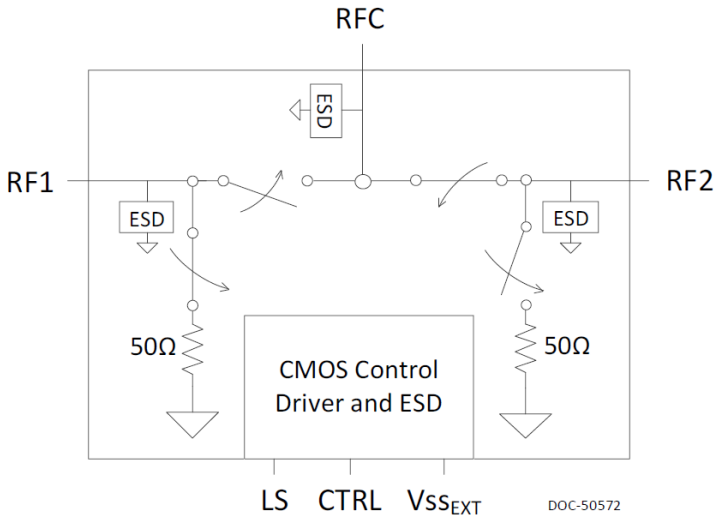


Figure 1. PE42521 functional diagram

Product description

pSemi designed the PE42521 SPDT absorptive RF switch for use in test/automated test equipment (ATE) and other high-performance wireless applications. This broadband general-purpose switch maintains excellent RF performance and linearity from 9 kHz–13 GHz. This switch is a pin-compatible and upgraded version of the pSemi PE42552 with fast switching time and higher power handling of 36 dBm continuous wave (CW) and 38.5 dBm instantaneous power in 50Ω @ 4 GHz. The PE42521 exhibits high isolation, fast settling time, and is offered in a 16-lead 3 × 3 mm QFN package.

The PE42521 is manufactured using the pSemi UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42521 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (CTRL)	V_{CTRL}	-0.3	3.6	V
LS input voltage	V_{LS}	-0.3	3.6	V
RF input power, CW (RFC–RFx):(1) - 9 kHz ≤ 600 MHz - 600 MHz ≤ 4 GHz - 4 GHz ≤ 13 GHz	P_{IN-CW}	–	Figure 2 36 Figure 3	dBm
RF input power, pulsed (RFC-RFX):(2) - 9 kHz ≤ 600 MHz - 600 MHz ≤ 13 GHz	$P_{IN-PULSED}$	–	Figure 2 Figure 3	dBm
RF input power into terminated ports, CW (RFX):(1) - 9 kHz ≤ 30 MHz - 30 MHz ≤ 13 GHz	$P_{IN,TERM}$	–	Figure 2 26	dBm
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM:(3) - RF pins to GND - All pins	$V_{ESD,HBM}$	–	3000 1500	V
ESD voltage MM, all pins(4)	$V_{ESD,MM}$	–	200	V
ESD voltage CDM, all pins(5)	$V_{ESD,CDM}$	–	1000	V

Parameter or condition	Symbol	Min	Max	Unit

1. 100% duty cycle, all bands, 50Ω.
2. Pulsed, 5% duty cycle of 4620-µs period, 50Ω.
3. Human Body Model (MIL-STD 883 Method 3015).
4. Machine Model (JEDEC JESD22-A115).
5. Charged Device Model (JEDEC JESD22-C101).

Recommended operating conditions

Table 2 lists the PE42521 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42521 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage (normal mode, Vss_{EXT} = 0V)(1)	V_{DD}	2.3	–	5.5	V
Supply voltage (bypass mode, Vss_{EXT} = -3.4V, VDD ≥ 3.4V for full specification compliance)(2)	V_{DD}	2.7	3.4	5.5	V
Negative supply voltage (bypass mode)(2)	Vss_{EXT}	-3.6	–	-3.2	V
Supply current (normal mode, Vss_{EXT} = 0V)(1)	I_{DD}	–	120	200	µA
Supply current (bypass mode, Vss_{EXT} = -3.4V)(2)	I_{DD}	–	50	80	µA
Negative supply current (bypass mode, Vss_{EXT} = -3.4V)(2)	I_{SS}	-40	-16	–	µA
Digital input high (CTRL)	V_{IH}	1.07	–	3.6	V
Digital input low (CTRL)	V_{IL}	-0.3	–	0.68	V
Digital input current	I_{CTRL}	–	–	10	µA
RF input power, CW (RFC–RFx):(3) - 9 kHz ≤ 600 MHz - 600 MHz ≤ 4 GHz - 4 GHz ≤ 13 GHz	P_{IN-CW}	–	–	Figure 2 36 Figure 3	dBm
RF input power, pulsed (RFC-RFX):(4) - 9 kHz ≤ 600 MHz - 600 MHz ≤ 13 GHz	$P_{IN-PULSED}$	–	–	Figure 2 Figure 3	dBm
RF input power, hot switch, CW:(3) - 9 kHz ≤ 10 MHz - 10 MHz ≤ 13 GHz	P_{IN-HOT}	–	–	Figure 2 20	dBm
RF input power into terminated ports, CW (RFX):(3) - 9 kHz ≤ 30 MHz - 30 MHz ≤ 13 GHz	$P_{IN,TERM}$	–	–	Figure 2 26	dBm
Operating temperature range	T_{OP}	-40	+25	+85	°C

1. Normal mode: Connect Vss_{EXT} (pin 13) to GND (Vss_{EXT} = 0V) to enable the internal negative voltage generator.
2. Bypass mode: Use Vss_{EXT} (pin 13) to bypass and disable the internal negative voltage generator.
3. 100% duty cycle, all bands, 50Ω.
4. Pulsed, 5% duty cycle of 4620-µs period, 50Ω.

Electrical specifications

Table 3 lists the PE42521 key electrical specifications at +25 °C, V_{DD} = 3.3V, Vss_{EXT} = 0V or V_{DD} = 3.4V, Vss_{EXT} = -3.4V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. PE42521 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	9 kHz	–	13 GHz	As shown
Insertion loss	RFC–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	–	0.60 0.75 0.95 1.15 1.75 1.85	0.80 1.00 1.20 1.40 2.20 2.60	dB
Isolation	RFx–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	70 46 35 23 16 14	90 49 37 26 19 17	–	dB
Isolation	RFC–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	80 42 39 26 18 14	90 44 41 30 21 17	–	dB
Return loss (active port)	RFC–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	–	23 19 16 21 10 15	–	dB
Return loss (common port)	RFC–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	–	23 19 16 21 10 16	–	dB
Return loss (terminated port)	RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	–	32 23 18 11 6 5	–	dB
Input 0.1-dB compression point[1]	RFC–RFx	600 MHz–13 GHz	–	–	–	dBm
Input IP2	RFC–RFx	834 MHz, 1950 MHz	–	Figure 3	–	dBm
Input IP3	RFC–RFx	834 MHz, 1950 MHz, 2700 MHz	–	120	–	dBm
Setting time	–	50% CTRL to 0.05 dB final value	–	2	4	µs

Parameter	Path	Condition	Min	Typ	Max	Unit
Switching time[2]	–	50% CTRL to 90% or 10% of final value	–	500	700	ns

1. The input 0.1-dB compression point is a linearity figure of merit. For the RF input power P_{IN} (50Ω), see Table 2.
2. The PE42521 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 13 = GND). The rate at which the PE42521 can switch is only limited to the switching time above if an external negative supply is provided (pin 13 = VssEXT). The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal
reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Spurious performance

The PE42521 typical spurious performance is –135 dBm when Vss_{EXT} = 0V (pin 13 = GND). To further improve performance, disable the internal negative voltage generator by setting Vss_{EXT} = -3.4V.

Optional external Vss control (Vss_{EXT})

For proper operation, ground the Vss_{EXT} control pin (pin 13) or tie it to the Vss voltage specified in Table 2. When the Vss_{EXT} control pin is grounded, the field-effect transistors (FETs) in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spurious performance, apply Vss_{EXT} externally to bypass the internal negative voltage generator.

Logic Select (LS)

The Logic Select feature determines the definition for the CTRL pin, as shown in Table 4.

SPDT control logic

Table 4. PE42521 truth table

LS (pin 15)	CTRL (pin 14)	RFC–RF1	RFC–RF2
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	ON
1	1	OFF	OFF

Power de-rating curves

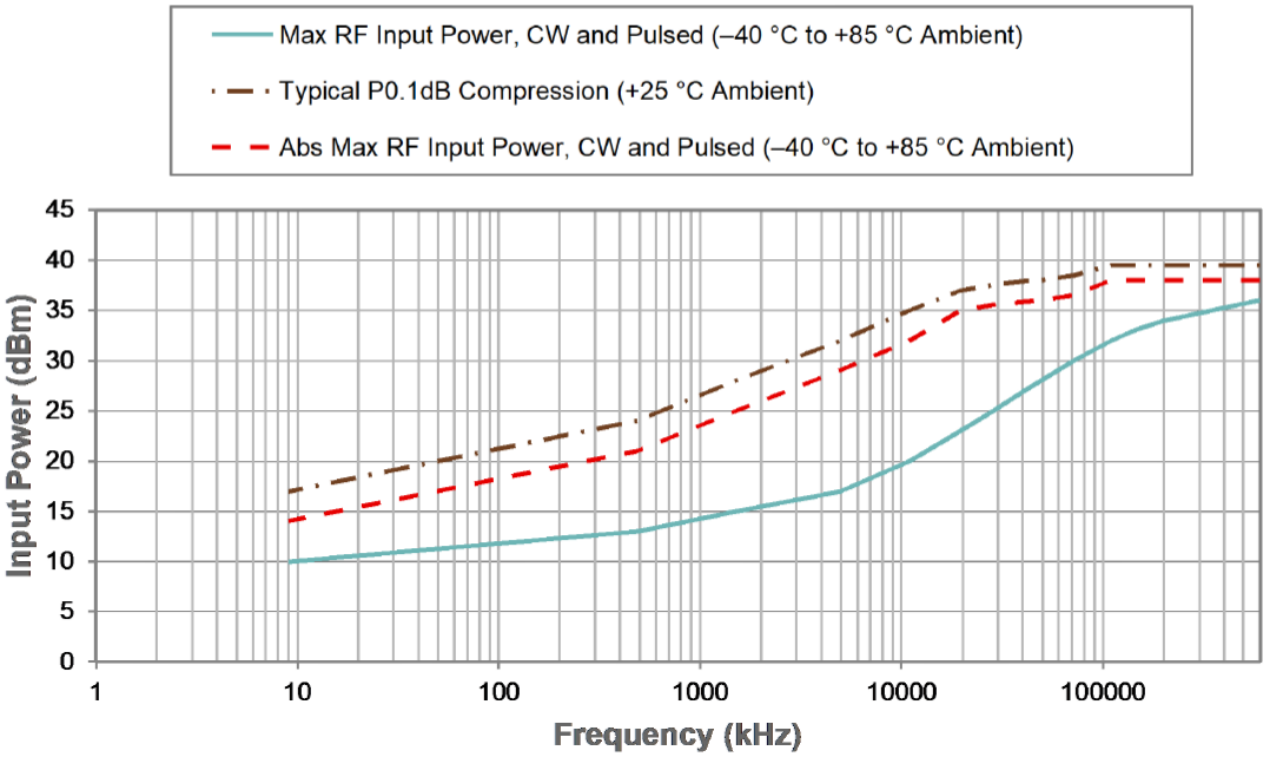


Figure 2. Power de-rating curve 9 kHz–600 MHz (50Ω)

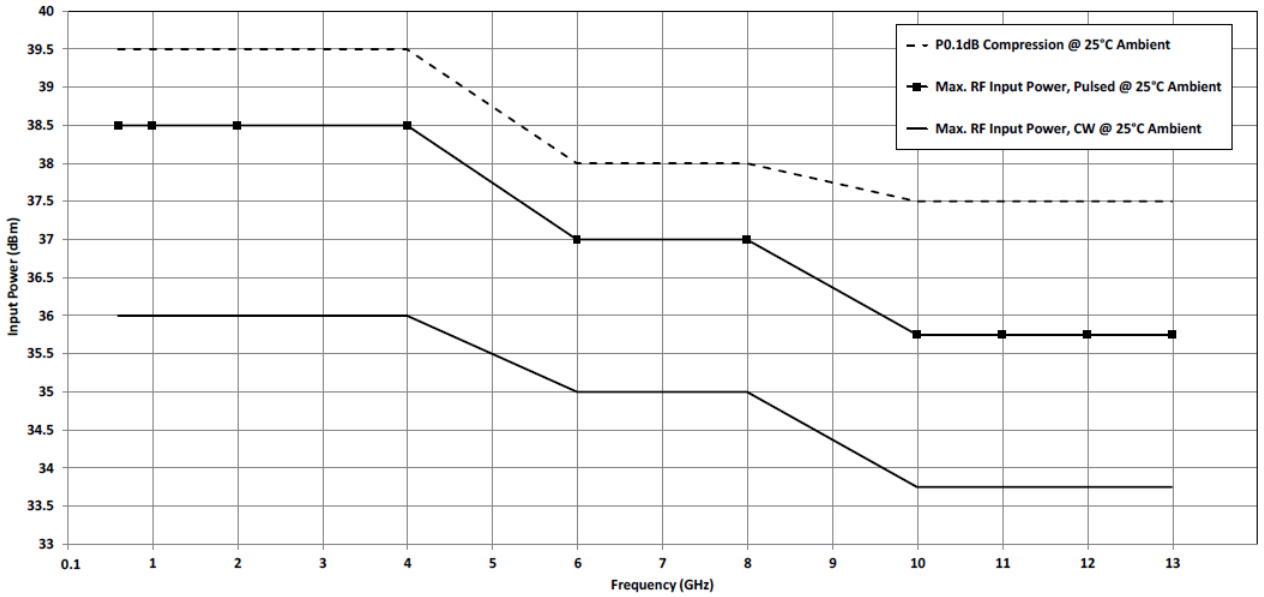


Figure 3. Power de-rating curve for 600 MHz–13 GHz @ 25 °C ambient (50Ω)

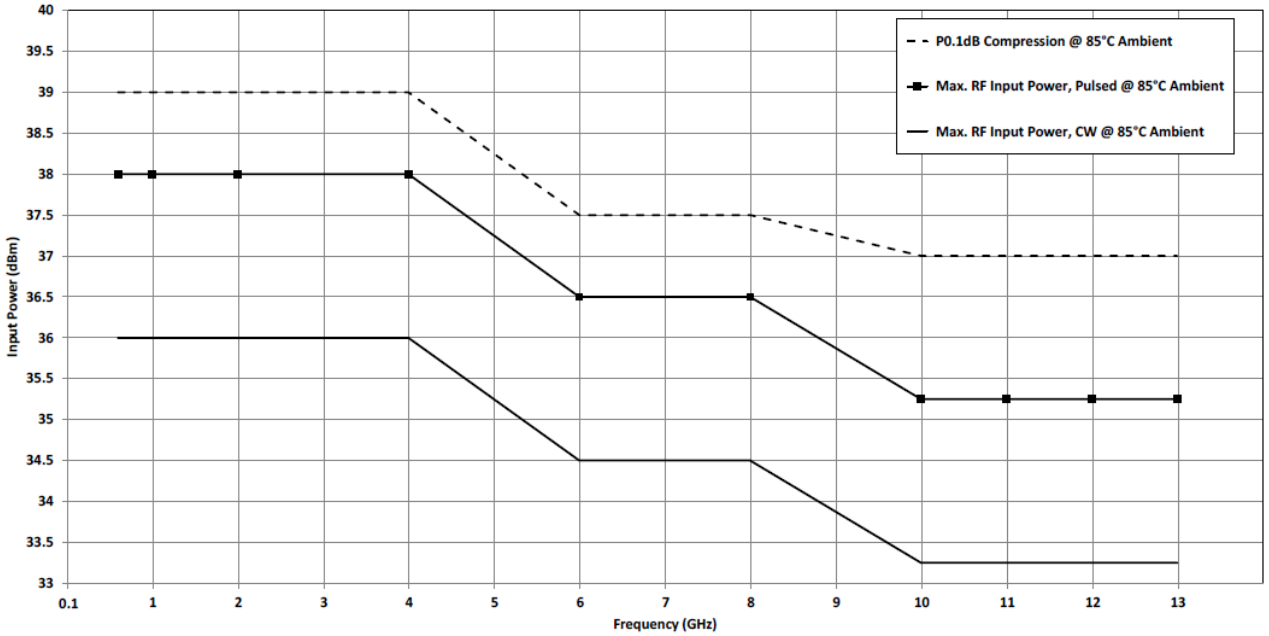


Figure 4. Power de-rating curve for 600 MHz–13 GHz @ 85 °C ambient (50Ω)

Typical performance data

Figure 5–Figure 28 show the typical performance data at +25 °C and V_{DD} = 3.4V, unless otherwise specified.

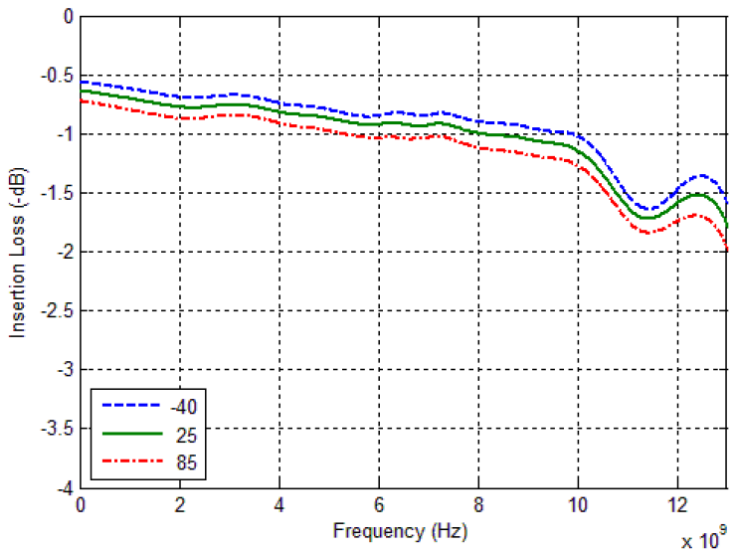


Figure 5. Insertion loss vs. temperature (RFC–RF1)

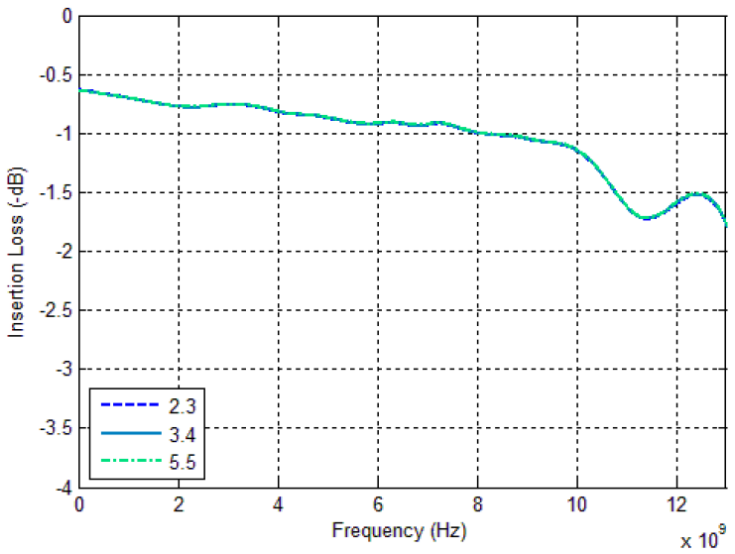


Figure 6. Insertion loss vs. V_{DD} (RFC–RF1)

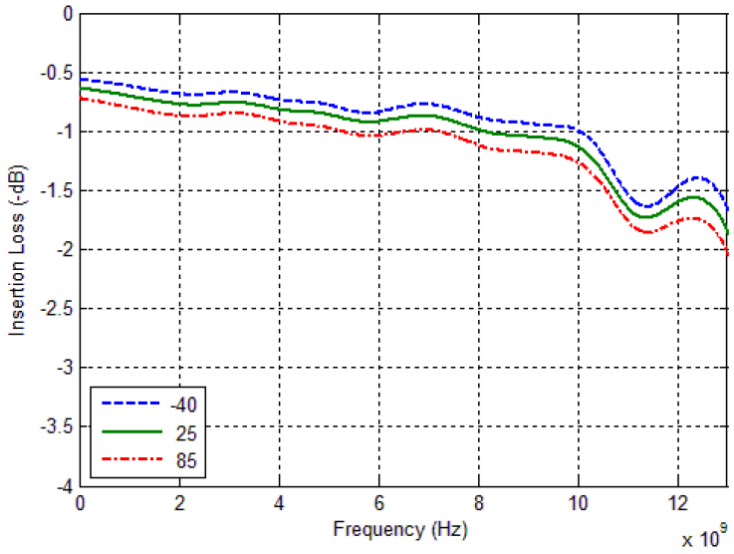


Figure 7. Insertion loss vs. temperature (RFC–RF2)

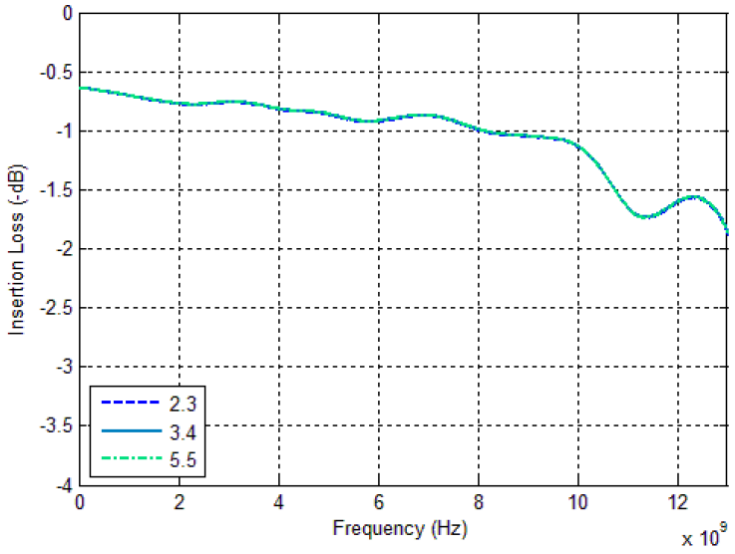


Figure 8. Insertion loss vs. V_{DD} (RFC–RF2)

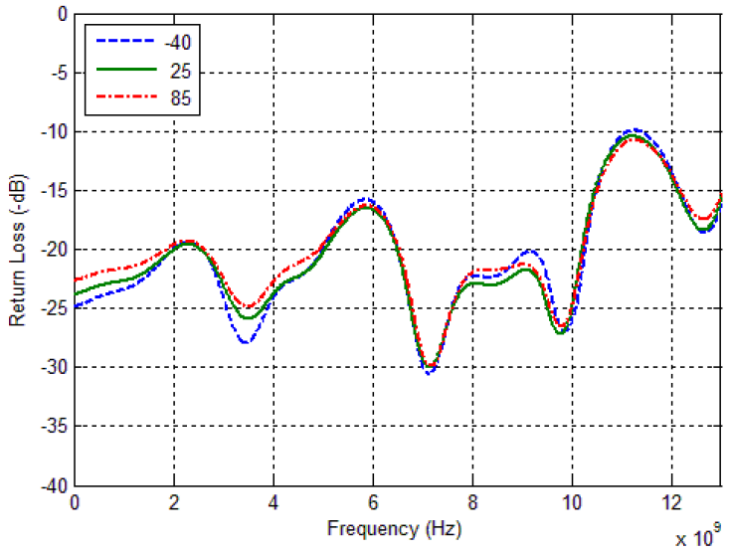


Figure 9. RFC port return loss vs. temperature (RF1 active)

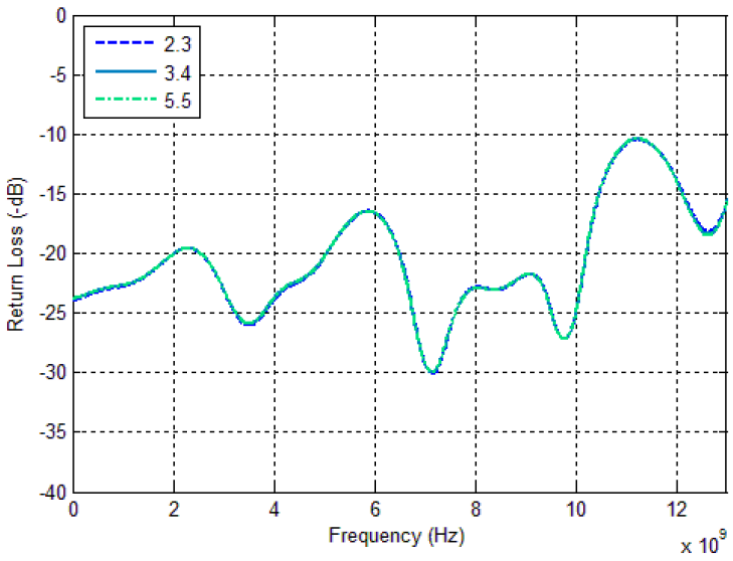


Figure 10. RFC port return loss vs. V_{DD} (RF1 active)

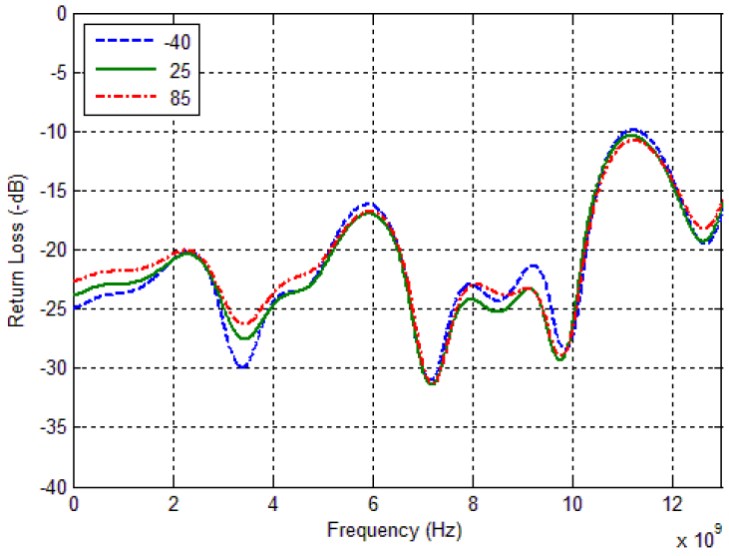


Figure 11. RFC port return loss vs. temperature (RF2 active)

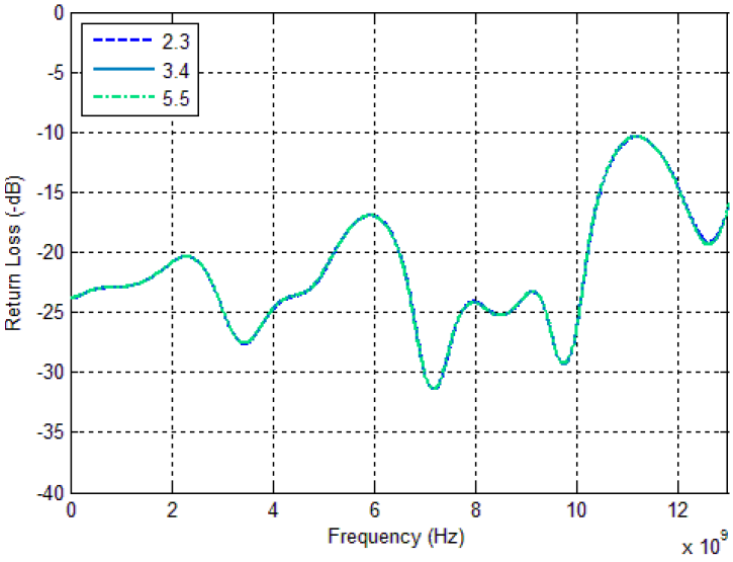


Figure 12. RFC port return loss vs. V_{DD} (RF2 active)

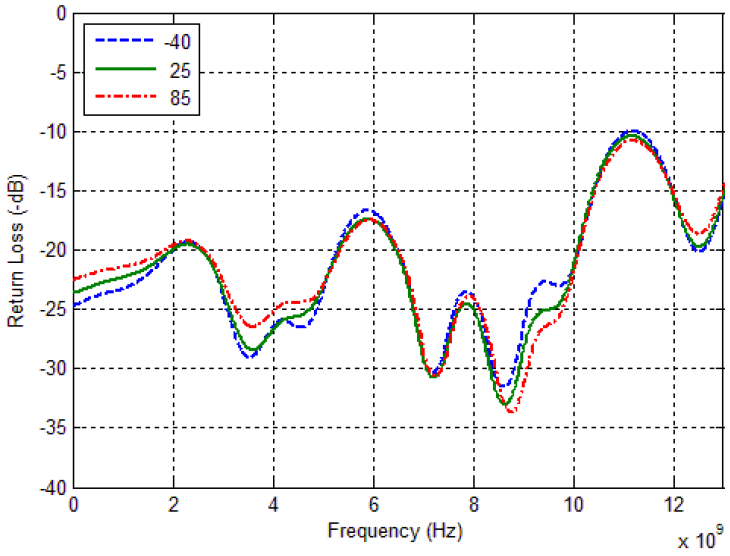


Figure 13. Active port return loss vs. temperature (RF1 active)

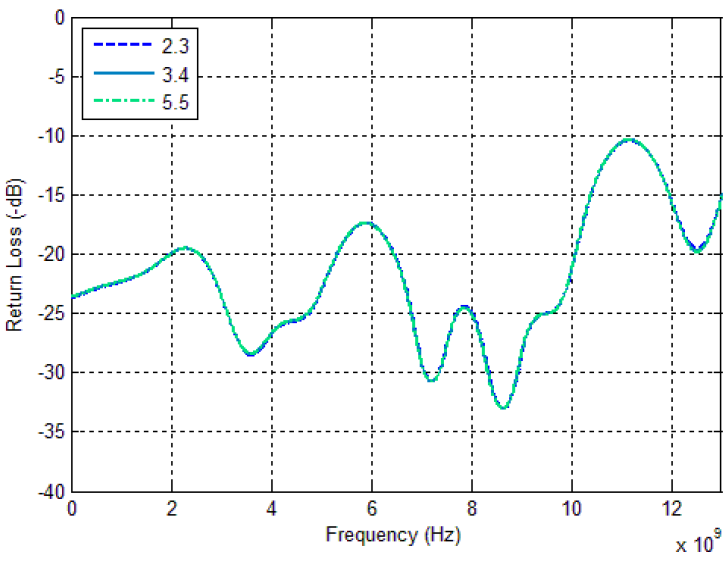


Figure 14. Active port return loss vs. V_{DD} (RF1 active)

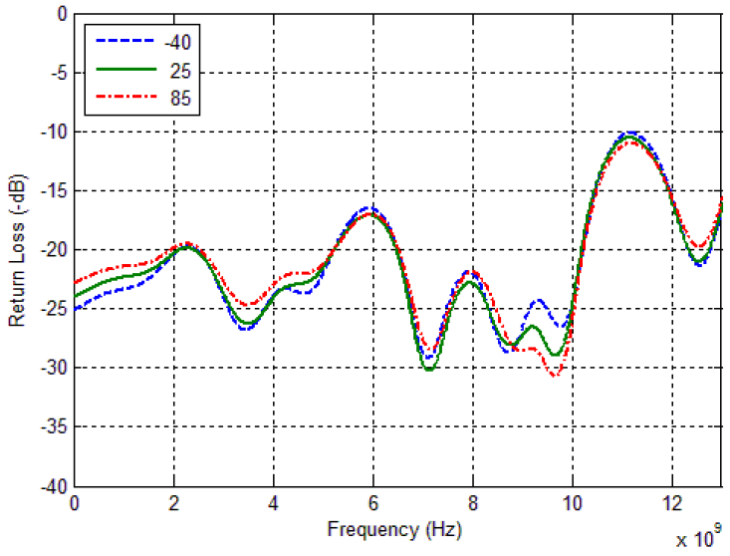


Figure 15. Active port return loss vs. temperature (RF2 active)

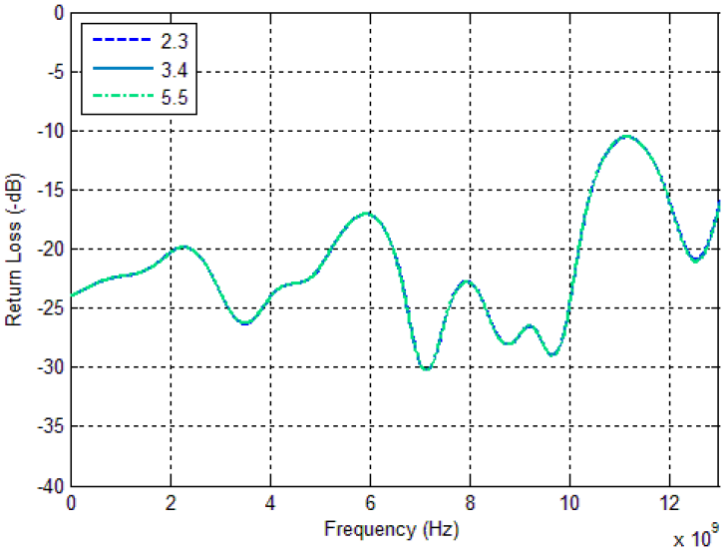


Figure 16. Active port return loss vs. V_{DD} (RF2 active)

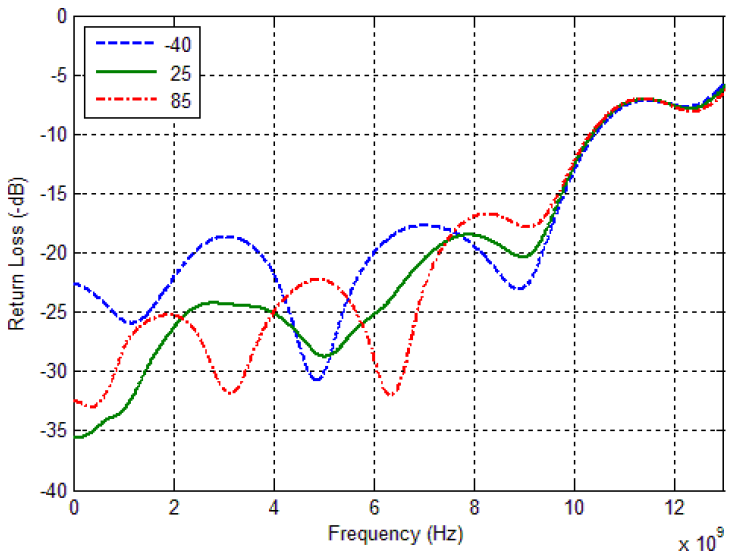


Figure 17. Terminated port return loss vs. temperature (RF1 active)

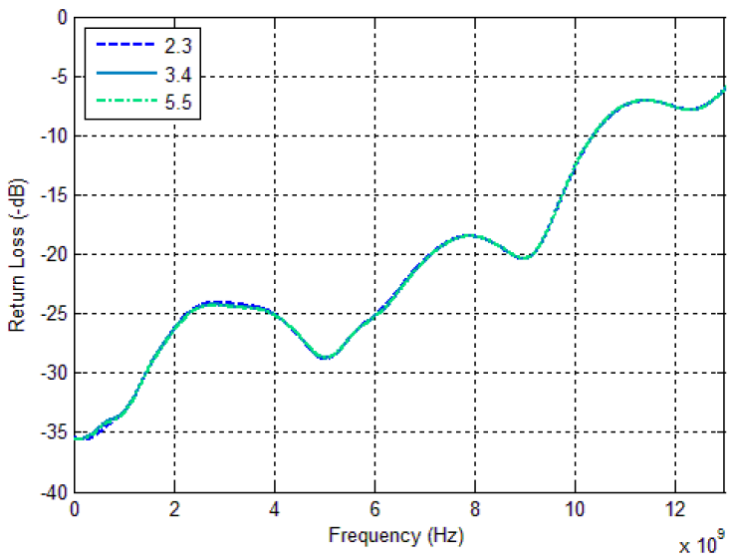


Figure 18. Terminated port return loss vs. V_{DD} (RF1 active)

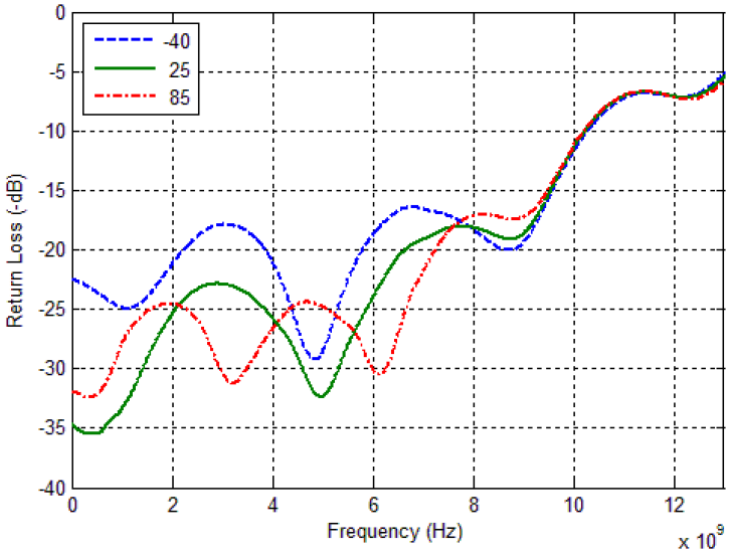


Figure 19. Terminated port return loss vs. temperature (RF2 active)

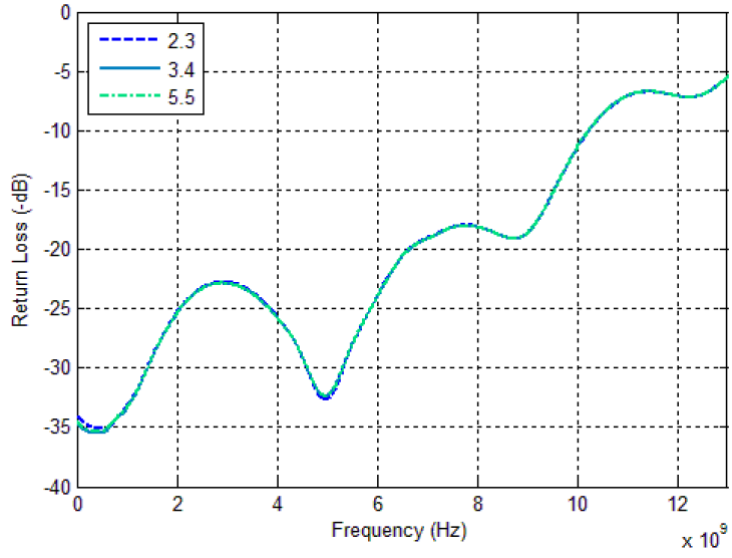


Figure 20. Terminated port return loss vs. V_{DD} (RF2 active)

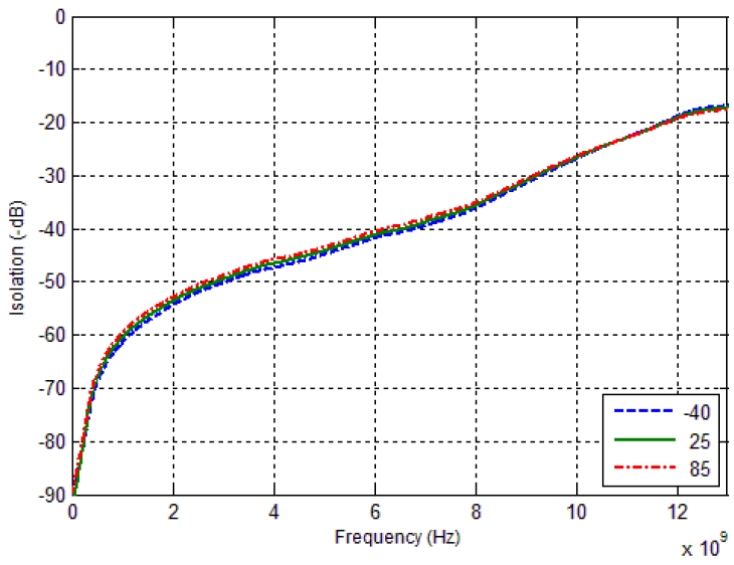


Figure 21. Isolation vs. temperature (RF1–RF2, RF1 active)

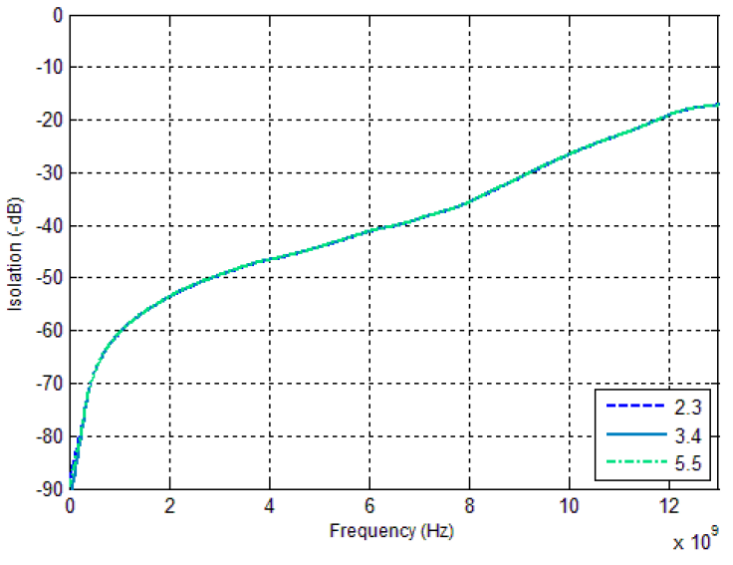


Figure 22. Isolation vs. V_{DD} (RF1–RF2, RF1 active)

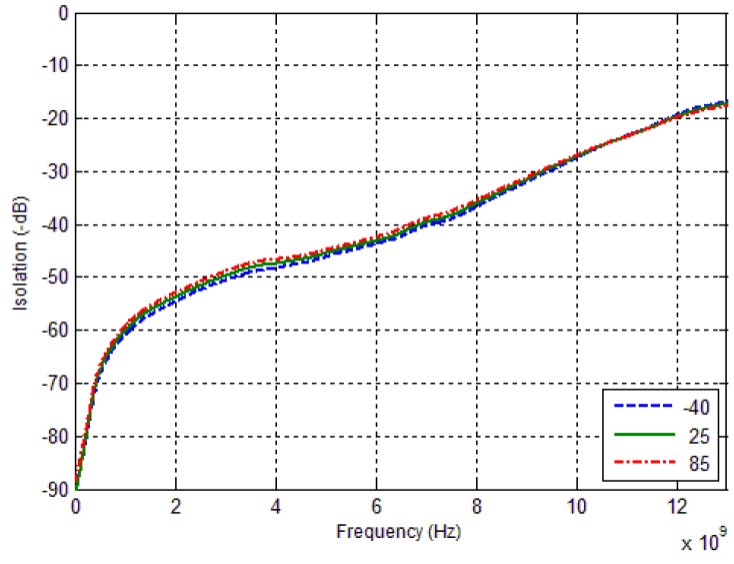


Figure 23. Isolation vs. temperature (RF2–RF1, RF2 active)

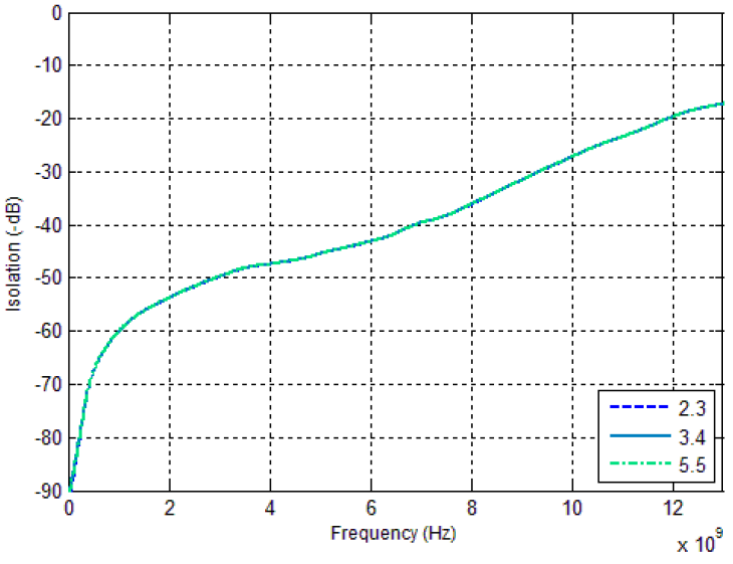


Figure 24. Isolation vs. V_{DD} (RF2–RF1, RF2 active)

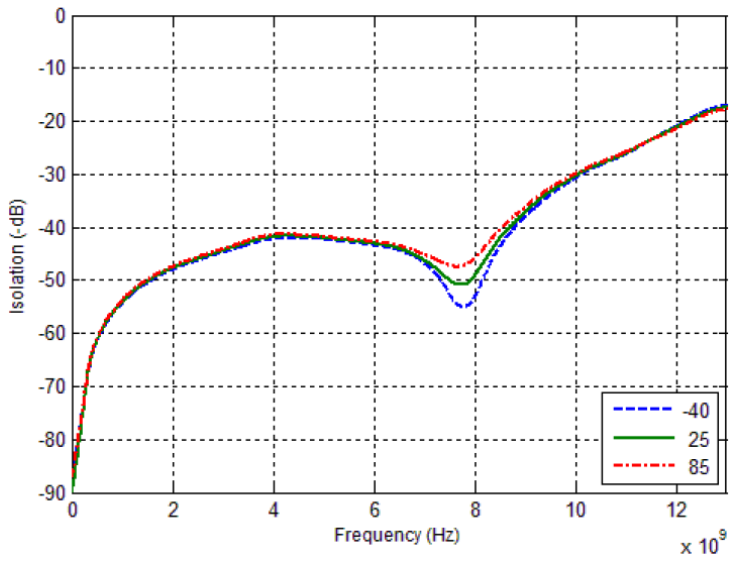


Figure 25. Isolation vs. temperature (RFC–RF2, RF1 active)

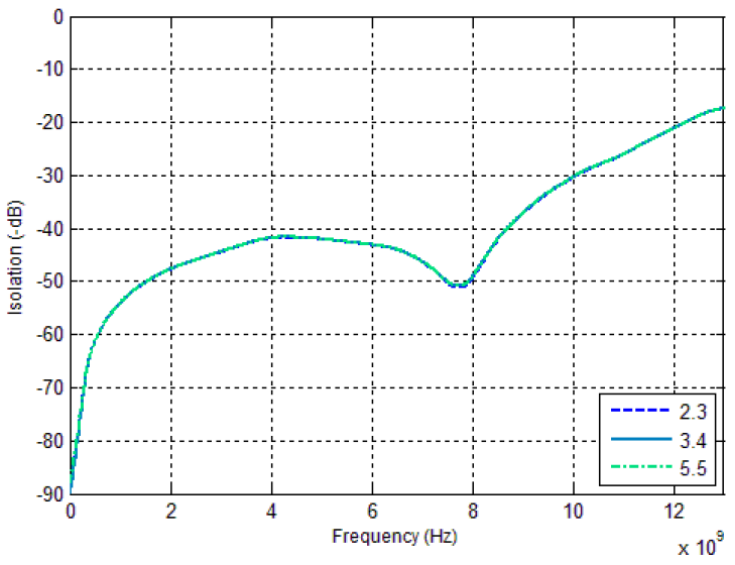


Figure 26. Isolation vs. V_{DD} (RFC–RF2, RF1 active)

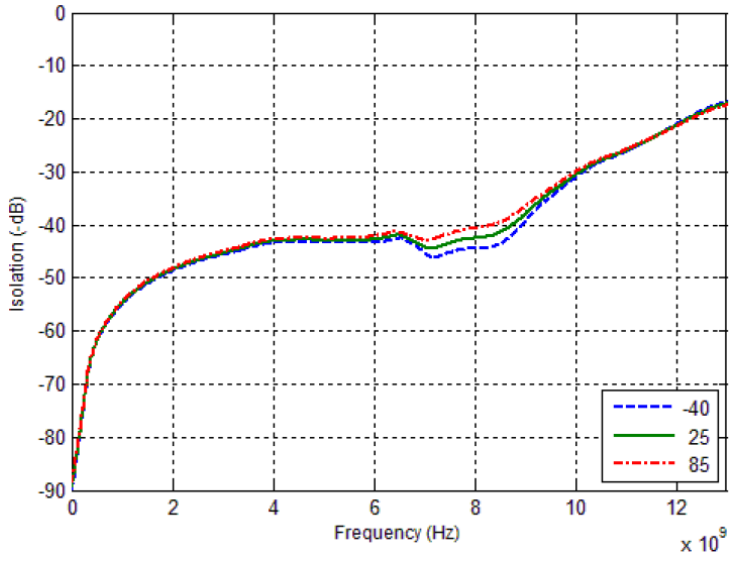


Figure 27. Isolation vs. temperature (RFC–RF1, RF2 active)

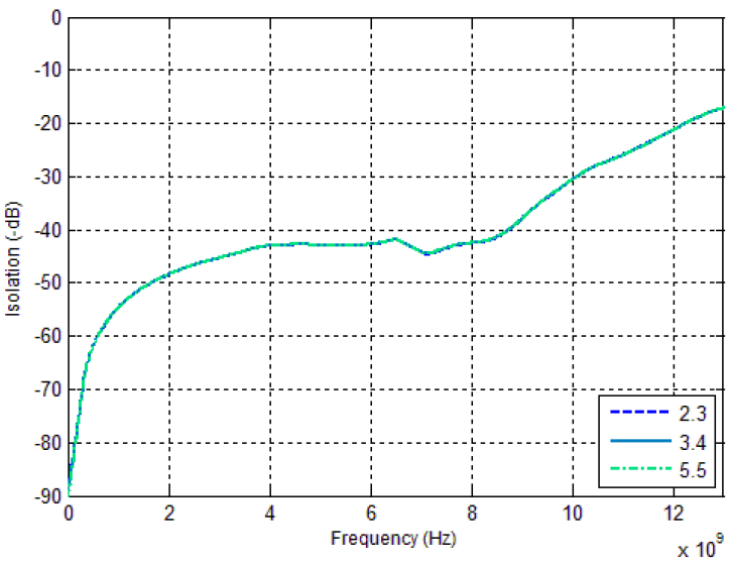


Figure 28. Isolation vs. V_{DD} (RFC–RF1, RF2 active)

Evaluation kit

pSemi designed the SPDT switch evaluation board to ease your evaluation of the pSemi PE42521. The RF common port connects through a 50Ω transmission line via the SMA connector, J1. The RF1 and RF2 ports connect through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which you can use to de-embed the loss of the PCB. J4 provides DC and digital inputs to the device.

To realize the true performance of the PE42521, design the PCB so that the RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

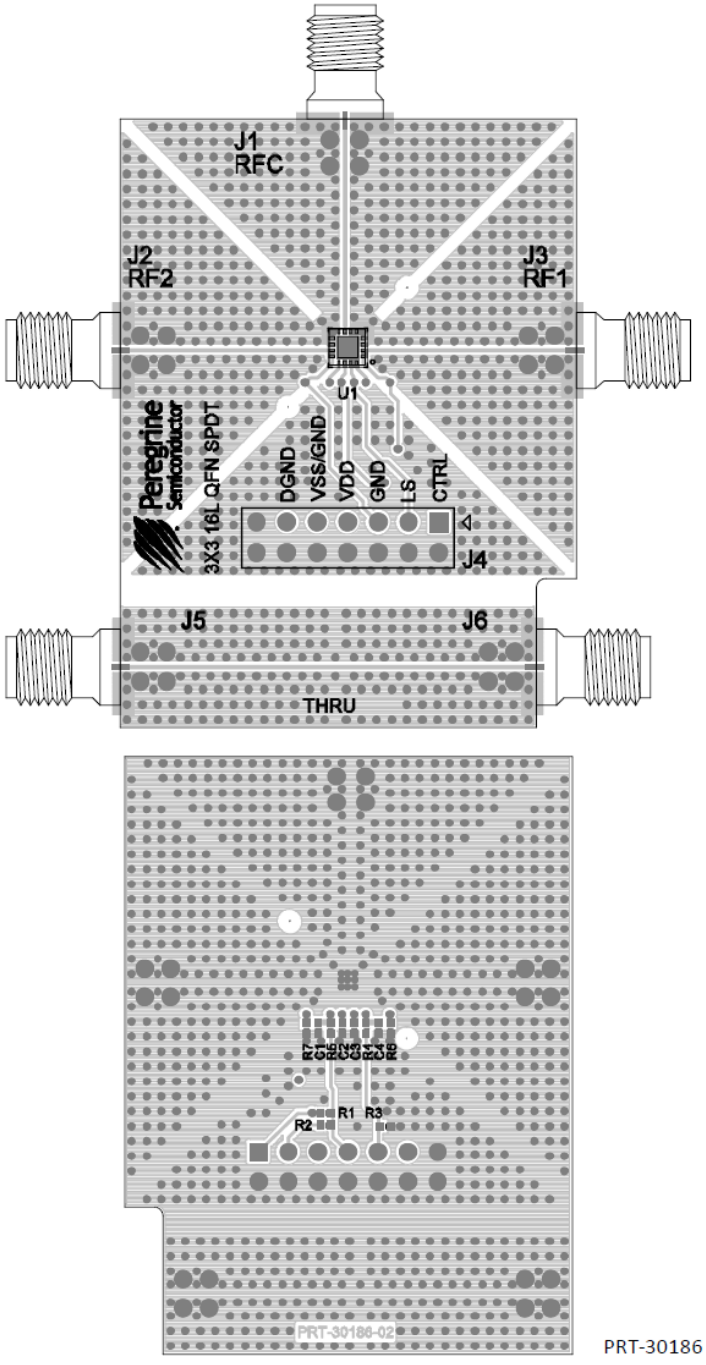
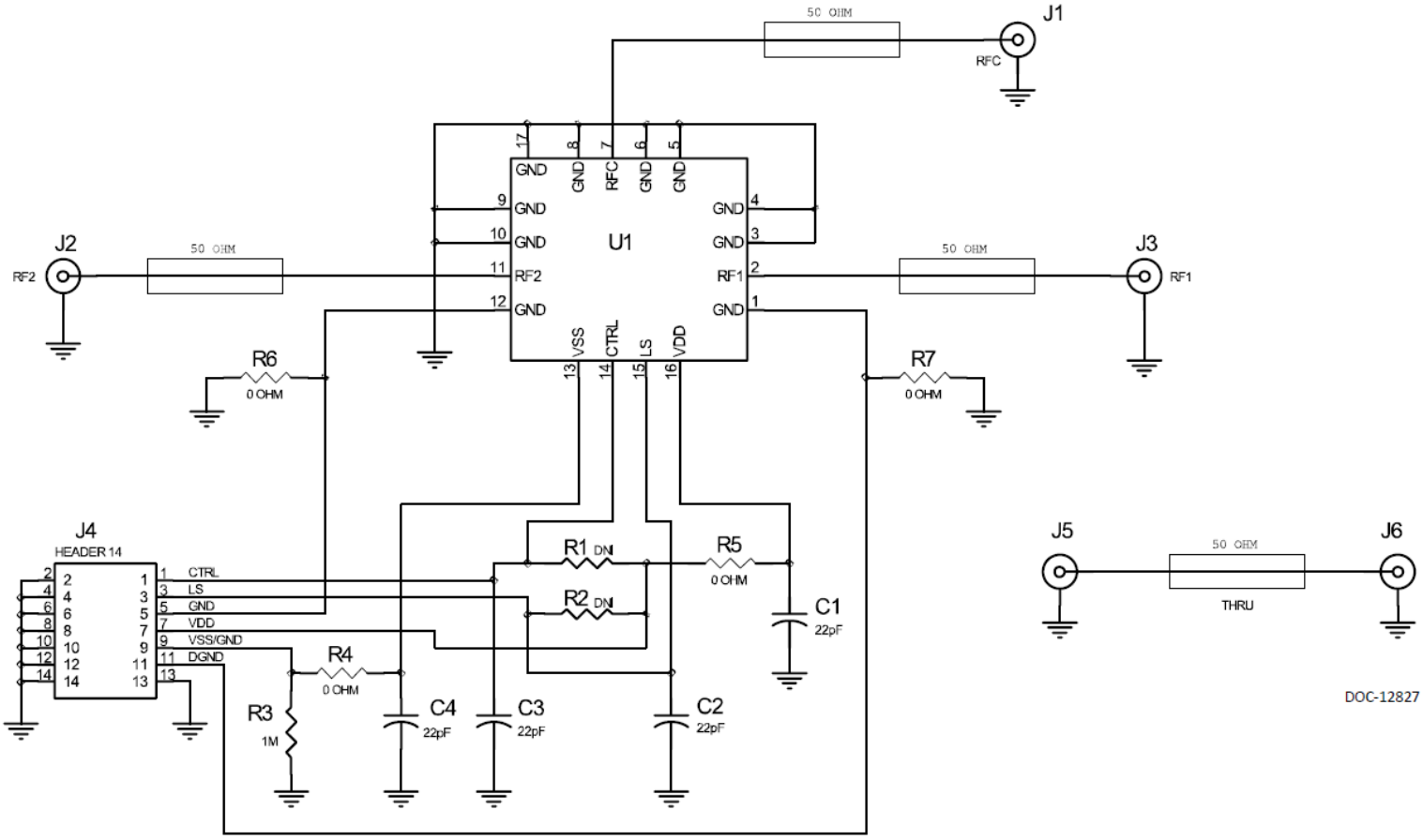


Figure 29. Evaluation board layout

Evaluation board schematic



Notes: 1. Use PRT-30186-02 PCB
2. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD)

Figure 30. Evaluation board schematic

Pin information

Figure 31 shows the PE42521 pin map for the 16-lead 3 × 3 mm QFN package, and Table 5 lists the description for each pin.

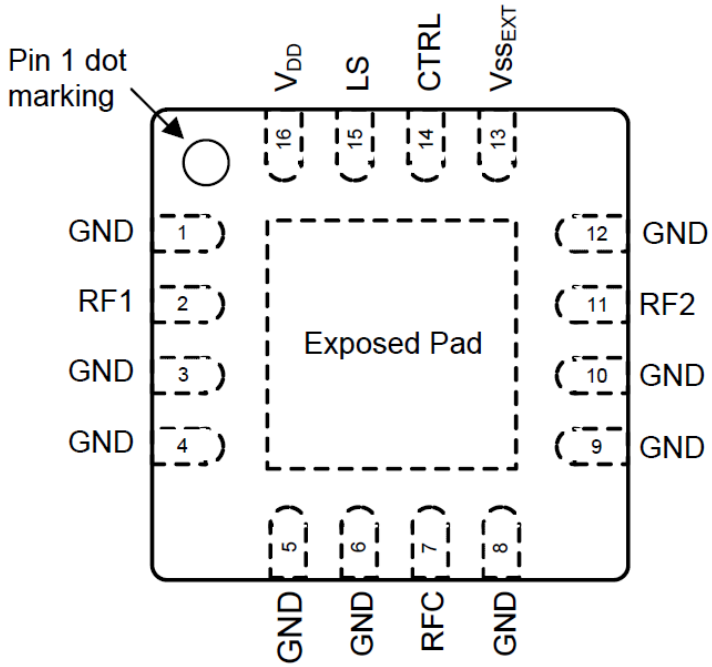


Figure 31. Pin configuration (top view)

Table 5. PE42521 pin descriptions

Pin no.	Pin name	Description
1, 3, 4, 5, 6, 8, 9, 10, 12	GND	Ground
2[1]	RF1	RF port 1
7[1]	RFC	RF common
11[1]	RF2	RF port 2
13[2]	Vss_{EXT}	External Vss negative voltage control
14	CTRL	Digital control logic input
15	LS	Logic Select: Determines the CTRL pin definition. See Table 4.
16	V_{DD}	Supply voltage
Pad	GND	Exposed pad. Ground for proper operation.

1. RF pins 2, 7, and 11 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Use Vss_{EXT} (pin 13) to bypass and disable the internal negative voltage generator. Connect Vss_{EXT} (pin 13) to GND (Vss_{EXT} = 0V) to enable the internal negative voltage generator.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42521 moisture sensitivity level rating for the 16-lead 3 × 3 mm QFN package is MSL3.

Package drawing

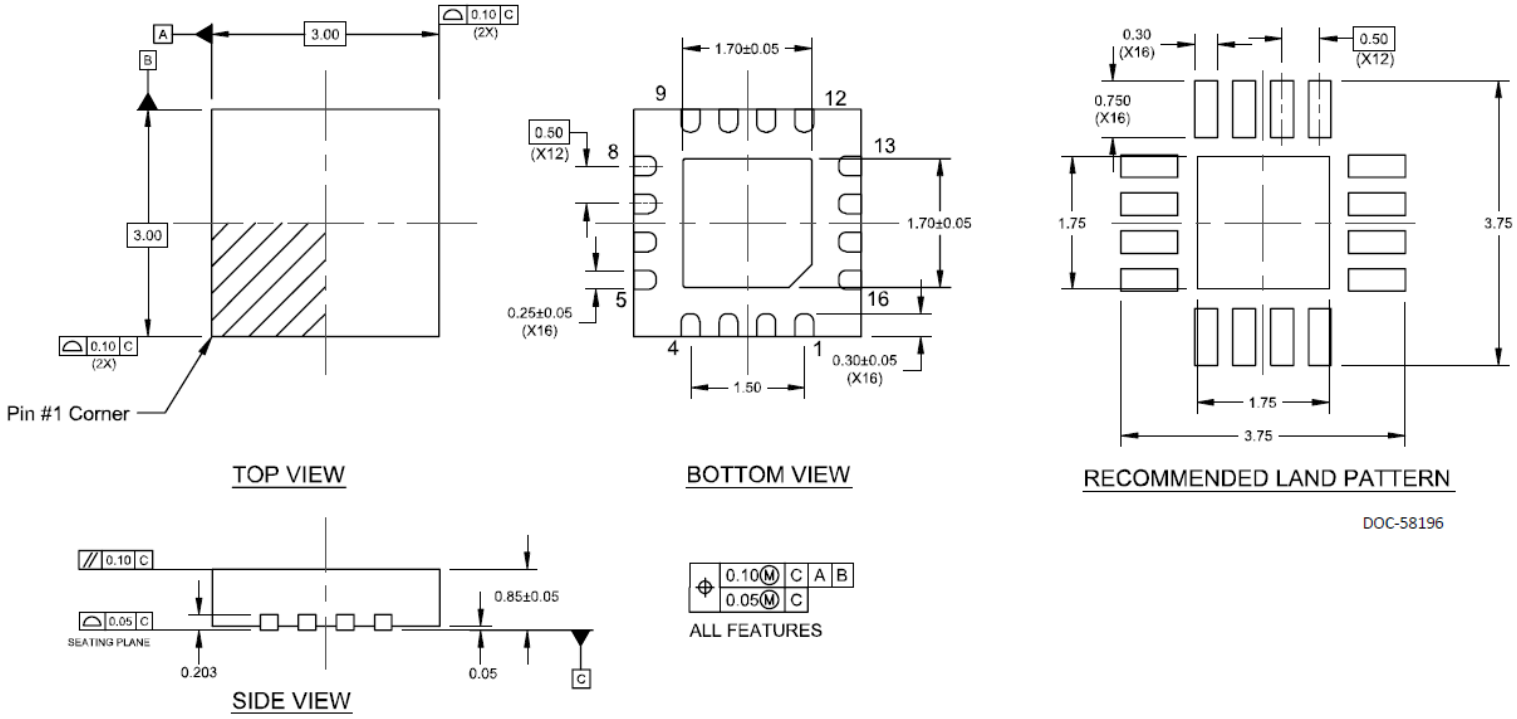


Figure 32. Package mechanical drawing for the 16-lead 3 × 3 mm QFN package

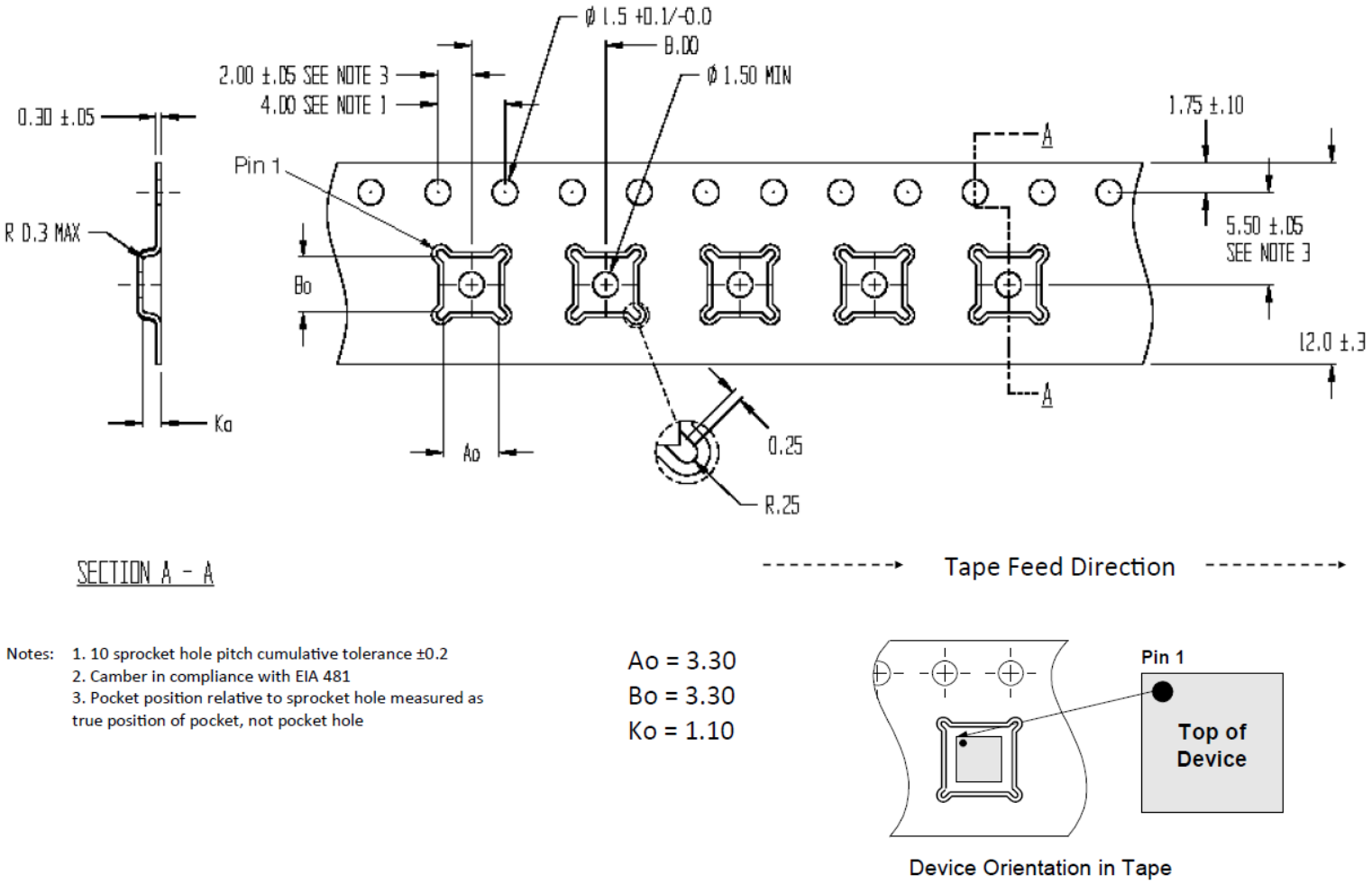
Top-marking specification



● = Pin 1 designator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Figure 33. PE42521 package marking specification

Tape and reel specification



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Ao = 3.30
Bo = 3.30
Ko = 1.10

Device Orientation in Tape

Figure 34. Tape and reel specification for the 16-lead 3 × 3 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE42521C-Z	PE42521 SPDT RF switch	Green 16-lead 3 × 3 mm QFN	3000 units/T&R
EK42521-03	PE42521 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
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