PE42520

Document category: Product Specification

UltraCMOS® SPDT RF Switch, 9 kHz–13 GHz

Features

- HaRP™ technology enhanced:
  - Fast settling time
  - No gate or phase lag
  - No drift in insertion loss or phase
- High power handling @ 8 GHz in 50Ω:
  - 36 dBm CW
  - 38 dBm instantaneous power
  - 26 dBm terminated port
- High linearity: 66 dBm IIP3
- Low insertion loss:
  - 0.8 dB @ 3 GHz
  - 0.9 dB @ 10 GHz
  - 2.0 dB @ 13 GHz
- High isolation:
  - 45 dB @ 3 GHz
  - 31 dB @ 10 GHz
  - 18 dB @ 13 GHz
- ESD performance:
  - 4 kV HBM on RF pins to GND
  - 2.5 kV HBM on all pins
  - 1 kV CDM on all pins
- Packaging: 16-lead 3 × 3 mm QFN

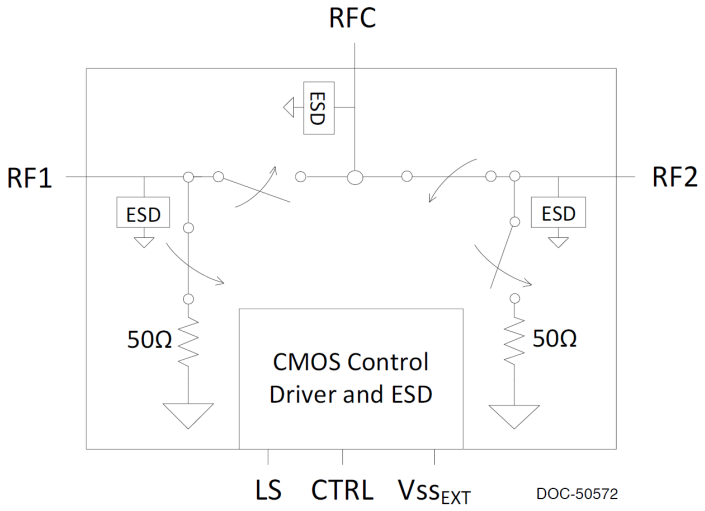


Figure 1. PE42520 functional block diagram

Applications

- Test and measurement
- Automated test equipment (ATE)
- High-performance wireless

Product description

The PE42520 SPDT absorptive RF switch is designed for use in test and measurement, ATE, and other high-performance wireless applications. This broadband general-purpose switch maintains excellent RF performance and linearity from 9 kHz through 13 GHz. This switch is a pin-compatible upgraded version of the pSemi PE42552 with higher power handling of 36 dBm continuous wave (CW) and 38 dBm instantaneous power in 50Ω @ 8 GHz. The PE42520 exhibits high isolation, fast settling time, and is offered in a 16-lead 3 × 3 mm QFN package.

pSemi manufactured the PE42520 using the pSemi UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42520 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (CTRL)	V_{CTRL}	-0.3	3.6	V
Logic Select (LS) input voltage	V_{LS}	-0.3	3.6	V
RF input power, CW (RFC–RFx)[1]: 9 kHz ≤ 10 MHz 10 MHz ≤ 8 GHz 8 GHz ≤ 13 GHz	P_{IN_CW}	–	See Figure 2 36 See Figure 3	dBm
RF input power, pulsed (RFC–RFx)[2]: 9 kHz ≤ 10 MHz 10 MHz ≤ 13 GHz	P_{IN_PULSED}	–	See Figure 2 See Figure 3	dBm
RF input power into terminated ports, CW (RFX)[1]: 9 kHz ≤ 10 MHz 10 MHz ≤ 13 GHz	P_{IN_TERM}	–	See Figure 2 29	dBm
Maximum junction temperature	T_{J_MAX}	–	+150	°C
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM[3]: RF pins to GND All pins	V_{ESD_HBM}	–	4000 2500	V
ESD voltage MM[4], all pins	V_{ESD_MM}	–	200	V
ESD voltage CDM[5], all pins	V_{ESD_CDM}	–	1000	V

Parameter or condition	Symbol	Min	Max	Unit

1. 100% duty cycle, all bands, 50Ω.
2. Pulsed, 5% duty cycle of 4620 µs period, 50Ω.
3. Human Body Model (MIL-STD 883 Method 3015).
4. Machine Model (JEDEC JESD22-A115).
5. Charged Device Model (JEDEC JESD22-C101).

Recommended operating conditions

Table 2 lists the PE42520 recommending operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42520 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage (normal mode, V_{SS_EXT} = 0V)[1]	V_{DD}	2.3	–	5.5	V
Supply voltage (bypass mode, V_{SS_EXT} = –3.4V, V_{DD} ≥ 3.4V for full specification compliance)[2]	V_{DD}	2.7	3.4	5.5	V
Negative supply voltage (bypass mode)[2]	V_{SS_EXT}	-3.6	–	-3.2	V
Supply current (normal mode, V_{SS_EXT} = 0V)[1]	I_{DD}	–	120	200	µA
Supply current (bypass mode, V_{SS_EXT} = –3.4V)[2]	I_{DD}	–	50	80	µA
Negative supply current (bypass mode, V_{SS_EXT} = –3.4V)[2]	I_{SS}	-40	-16	–	µA
Digital input high (CTRL)	V_{IH}	1.17	–	3.6	V
Digital input low (CTRL)	V_{IL}	-0.3	–	0.6	V
Digital input current	I_{CTRL}	–	–	10	µA
RF input power, CW (RFC–RFx)[3]: 9 kHz ≤ 10 MHz 10 MHz ≤ 8 GHz 8 GHz ≤ 13 GHz	P_{IN_CW}	–	–	See Figure 2 36 See Figure 3	dBm
RF input power, pulsed (RFC–RFx)[4]: 9 kHz ≤ 10 MHz 10 MHz ≤ 13 GHz	P_{IN_PULSED}	–	–	See Figure 2 See Figure 3	dBm
RF input power, hot switch, CW[3]: 9 kHz ≤ 300 kHz 300 kHz ≤ 13 GHz	P_{IN_HOT}	–	–	See Figure 2 20	dBm
RF input power into terminated ports, CW (RFx)[3]: 9 kHz ≤ 600 kHz 600 kHz ≤ 13 GHz	P_{IN_TERM}	–	–	See Figure 2 26	dBm
Operating temperature range	T_{OP}	-40	+25	+85	°C

1. Normal mode: Connect V_{SS_EXT} (pin 13) to GND (V_{SS_EXT} = 0V) to enable the internal negative voltage generator.
2. Bypass mode: Use V_{SS_EXT} (pin 13) to bypass and disable the internal negative voltage generator.
3. 100% duty cycle, all bands, 50Ω.
4. Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Electrical specifications

Table 3 lists the PE42520 key electrical specifications at +25 °C, V_{DD} = 3.3V, V_{SS_EXT} = 0V or V_{DD} = 3.4V, V_{SS_EXT} = -3.4V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. PE42520 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	9 kHz	–	13 GHz	As shown
Insertion loss	RFC–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	–	0.60 0.80 0.85 0.90 1.20 2.00	0.80 1.00 1.05 1.10 1.65 2.70	dB
Isolation	RFx–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	70 46 35 24 16 13	90 54 38 27 19 17	–	dB
Isolation	RFC–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	80 42 41 26 16 13	90 45 44 31 20 18	–	dB
Return loss (active port)	RFC–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	–	23 17 15 18 20 10	–	dB
Return loss (common port)	RFC–RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	–	23 17 15 18 18 10	–	dB
Return loss (terminated port)	RFx	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	–	32 24 21 13 8 5	–	dB
Input 0.1dB compression point[1]	RFC–RFx	10 MHz–13 GHz	–	See Figure 3	–	dBm
Input IP2	RFC–RFx	834 MHz and 1950 MHz	–	120	–	dBm
Input IP3	RFC–RFx	834 MHz, 1950 MHz, and 2700 MHz	–	66	–	dBm

Parameter	Path	Condition	Min	Typ	Max	Unit
Setting time	–	50% CTRL to 0.05 dB final value	–	15	20	µs
Switching time[2]	–	50% CTRL to 90% or 10% of final value	–	5.5	9.5	µs

1. The input 0.1dB compression point is a linearity figure of merit. For the RF input power PIN (50Ω), see Table 1.
2. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value. The PE42520 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 13 = GND). The rate at which the PE42520 can switch is only limited by the switching time if an external negative supply is provided (pin 13 = V_{SS_EXT}).

Optional external V_{SS} control (V_{SS_EXT})

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the VSS voltage specified in Table 1. When the V_{SS_EXT} control pin is grounded, the FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spurious performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Spurious performance

The typical spurious performance of the PE42520 is –152 dBm when V_{SS_EXT} = 0V (pin 13 = GND). For improved performance, disable the internal negative voltage generator by setting V_{SS_EXT} = –3.4V.

SPDT control logic

Table 4. PE42520 truth table

LS	CTRL	RFC–RF1	RFC–RF2
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

Power de-rating curve for 9 kHz–10 MHz

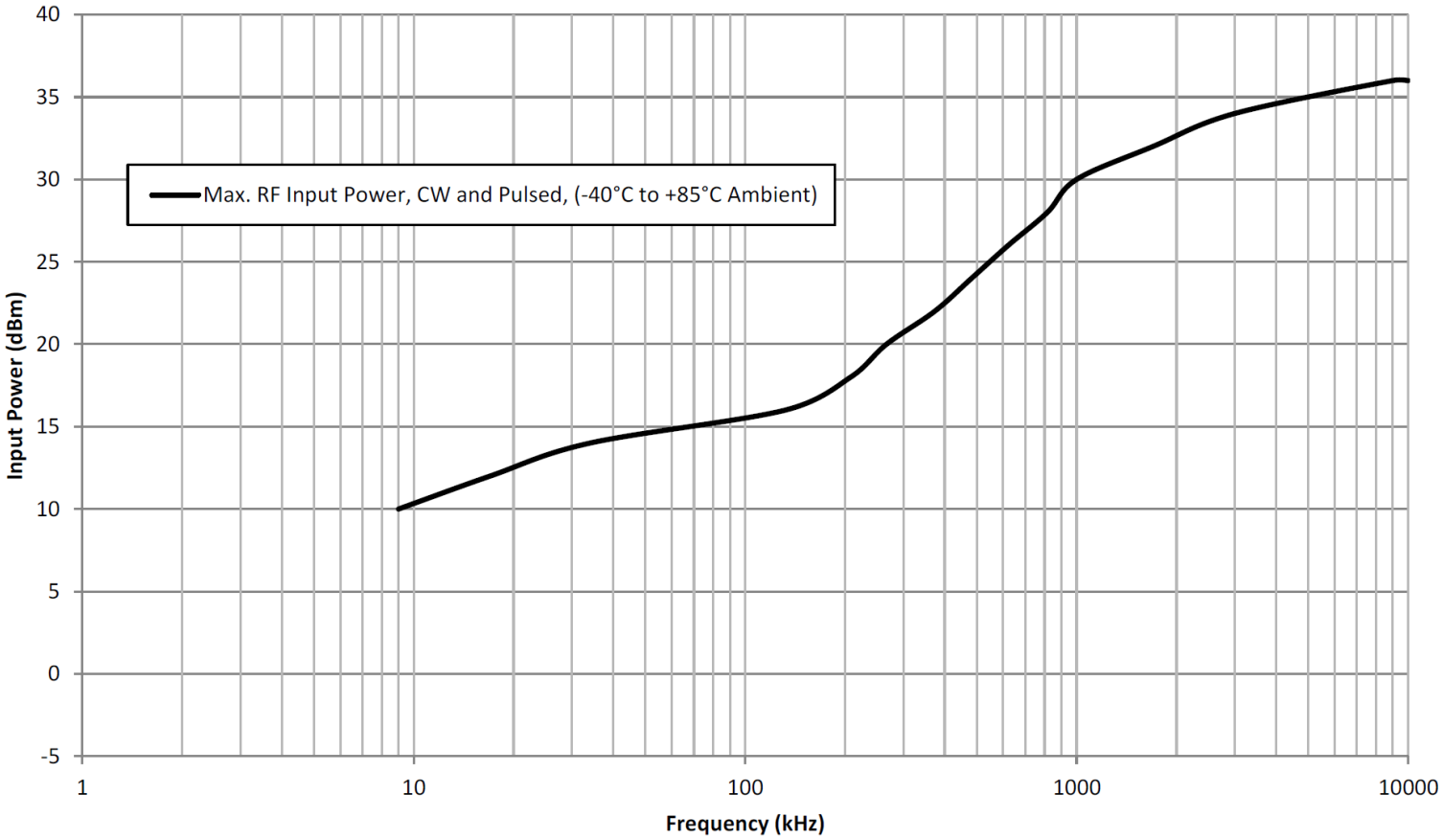


Figure 2. Power de-rating curve for 9 kHz–10 MHz (50Ω)

Power de-rating curves for 10 MHz–13 GHz

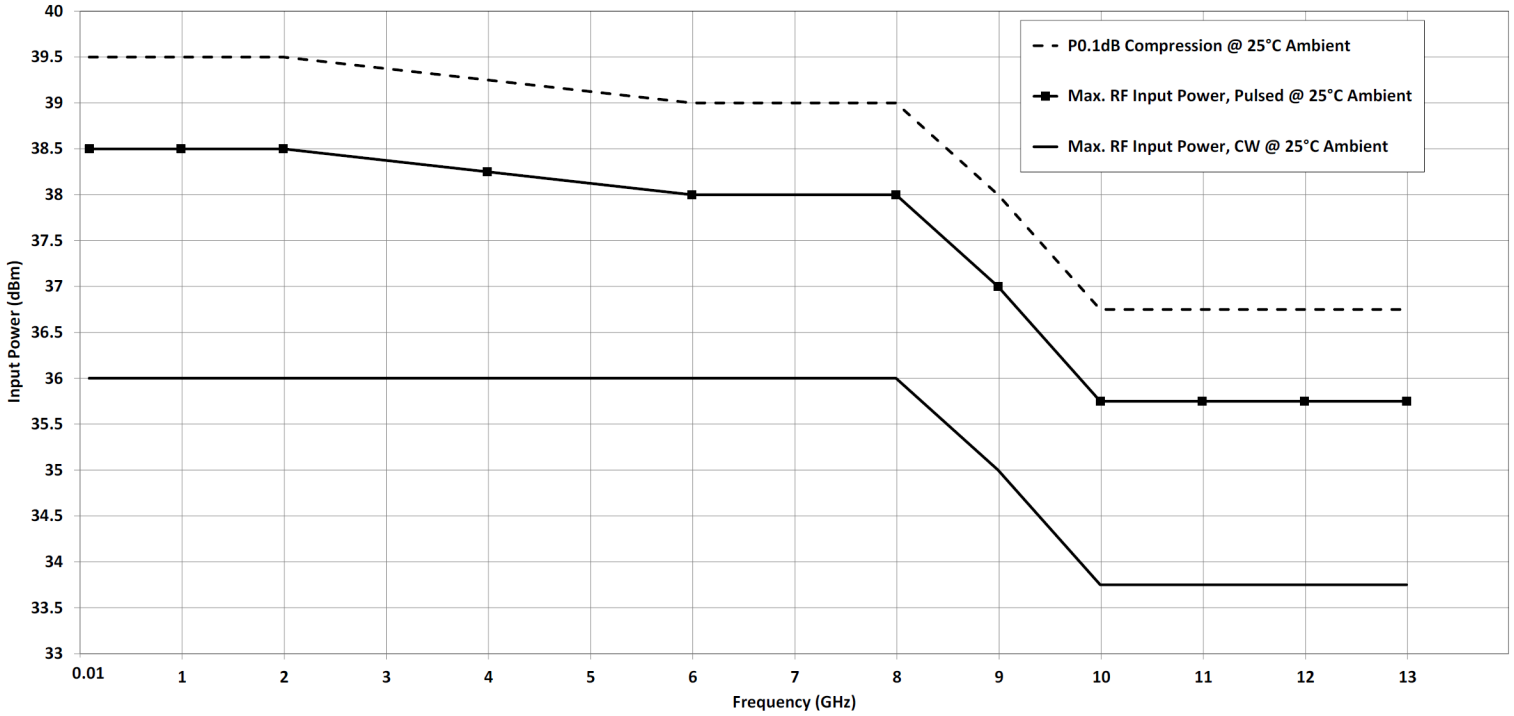


Figure 3. Power de-rating curve for 10 MHz–13 GHz @ +25 °C ambient (50Ω)

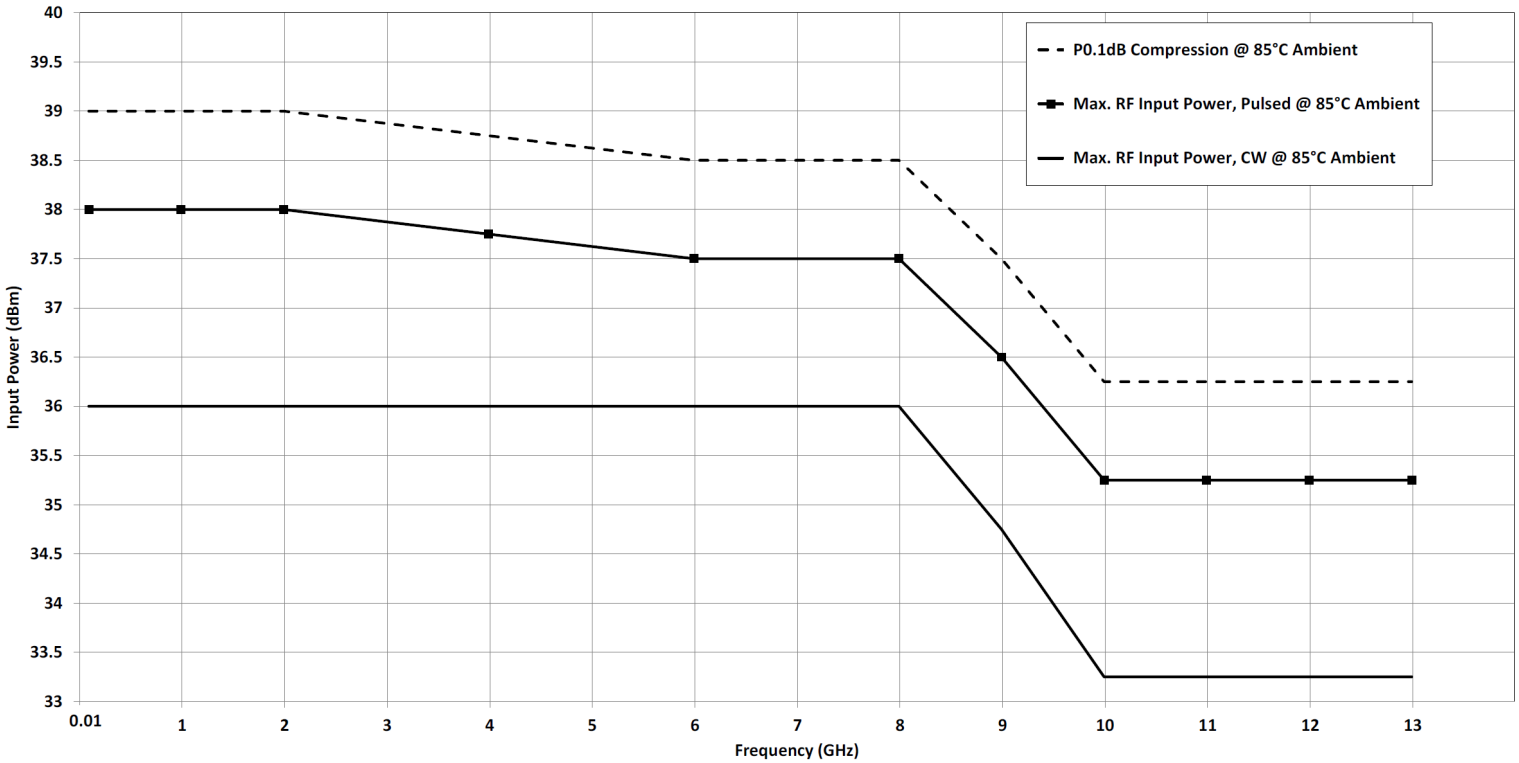


Figure 4. Power de-rating curve for 10 MHz–13 GHz @ +85 °C ambient (50Ω)

Typical performance data

Figure 5–Figure 28 show the typical performance data at +25 °C and V_{DD} = 3.4V, unless otherwise specified.

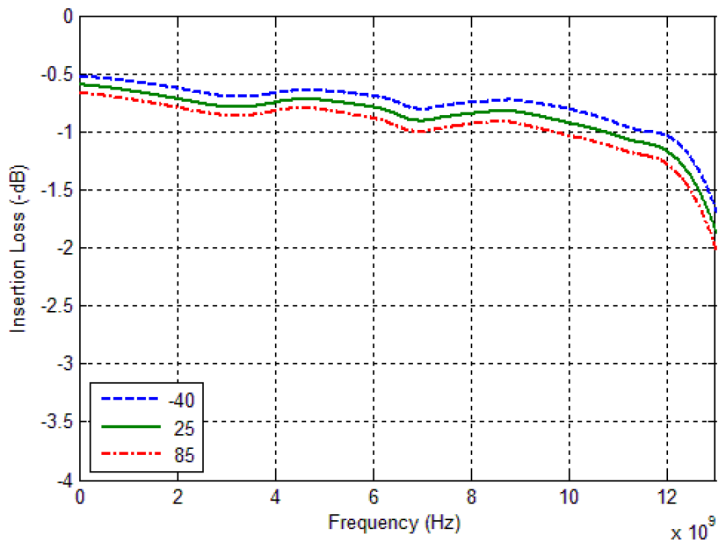


Figure 5. Insertion loss vs. temperature (RFC–RF1)

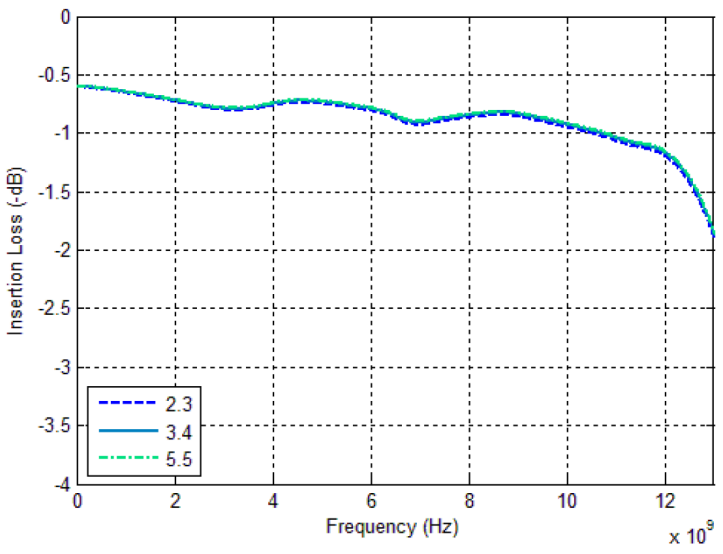


Figure 6. Insertion loss vs. V_{DD} (RFC–RF1)

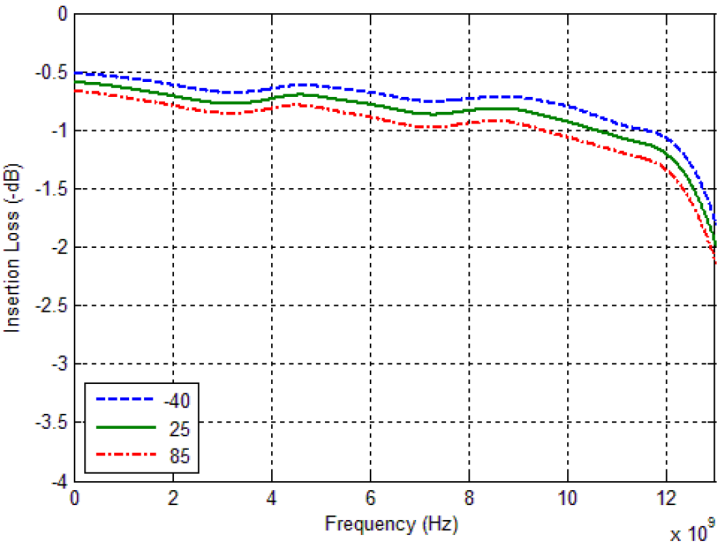


Figure 7. Insertion loss vs. temperature (RFC–RF2)

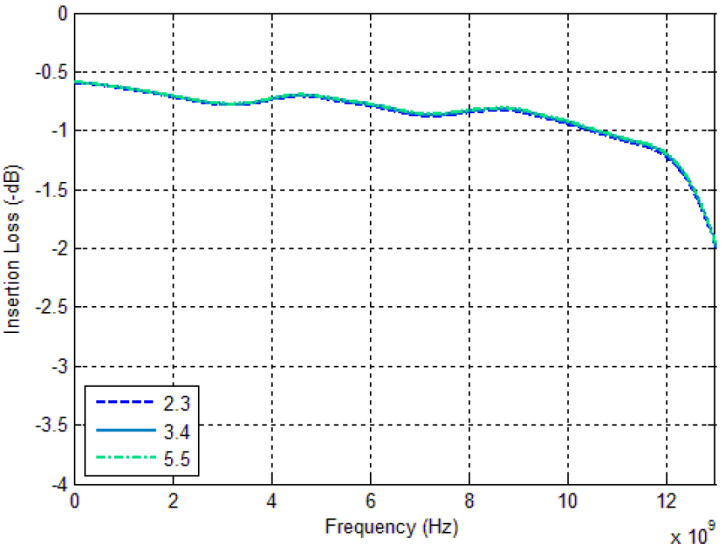


Figure 8. Insertion loss vs. V_{DD} (RFC–RF2)

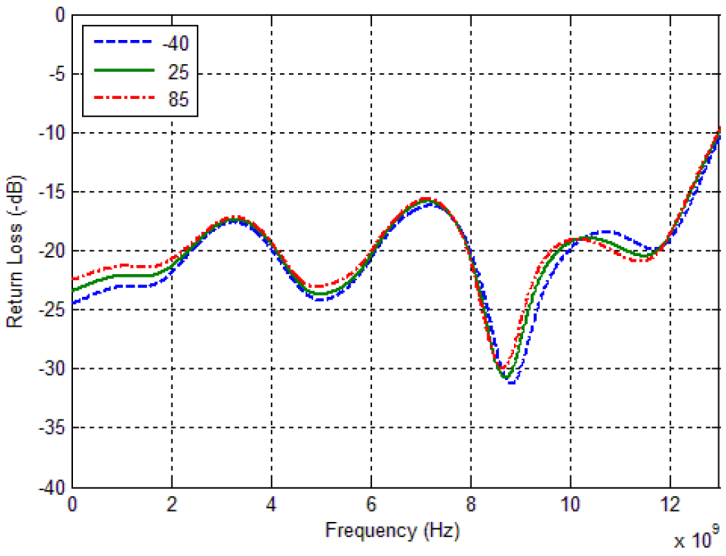


Figure 9. RFC port return loss vs. temperature (RF1 active)

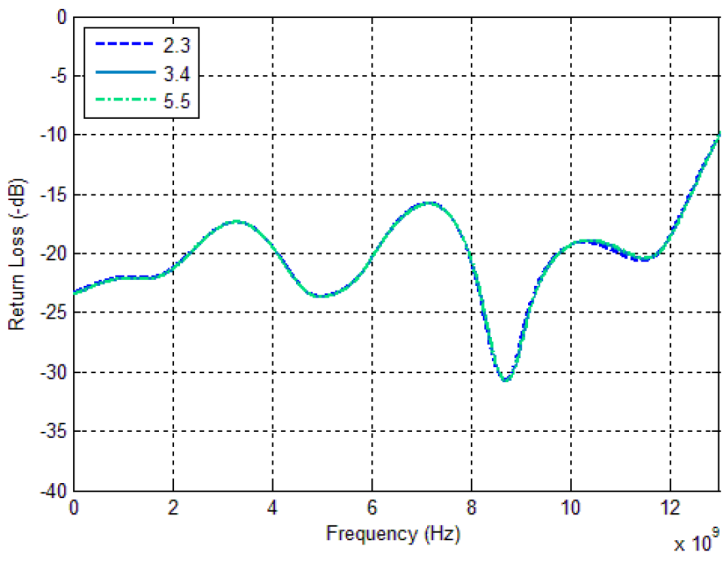


Figure 10. RFC port return loss vs. V_{DD} (RF1 active)

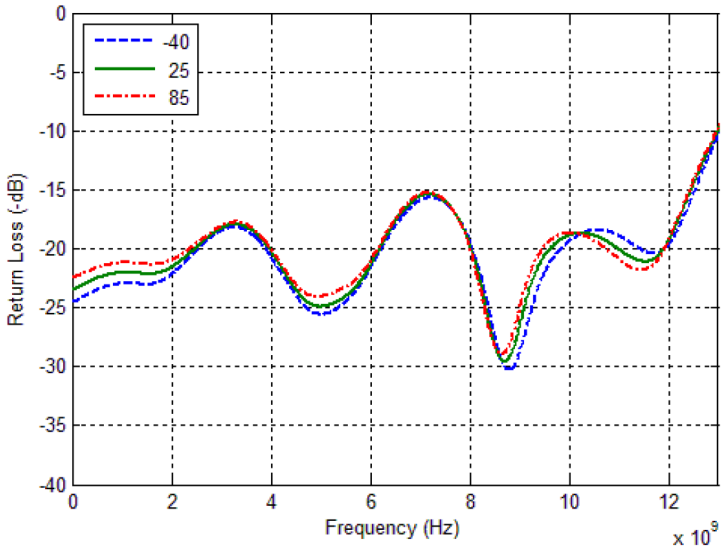


Figure 11. RFC port return loss vs. temperature (RF2 active)

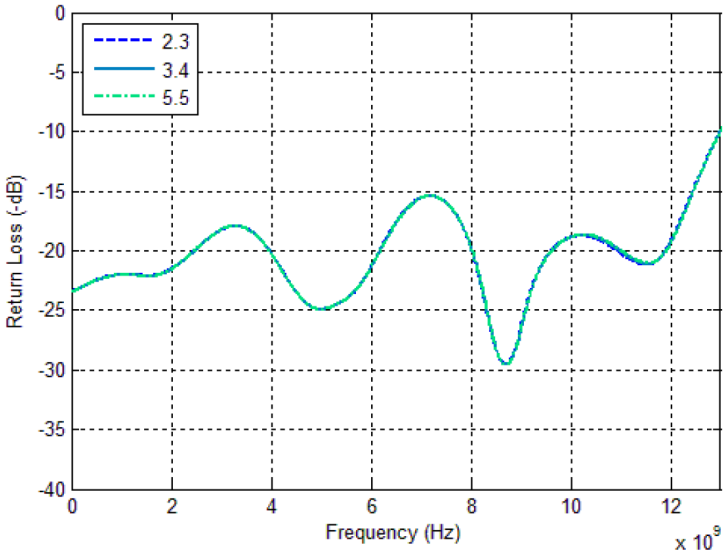


Figure 12. RFC port return loss vs. V_{DD} (RF2 active)

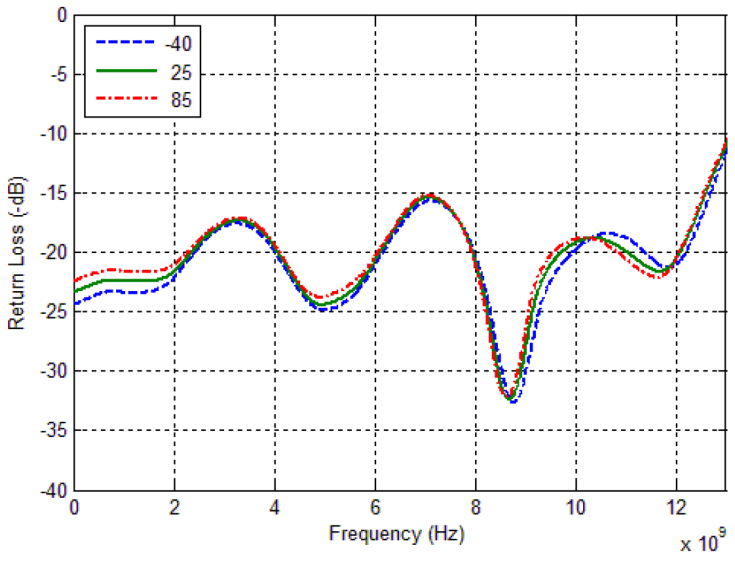


Figure 13. Active port return loss vs. temperature (RF1 active)

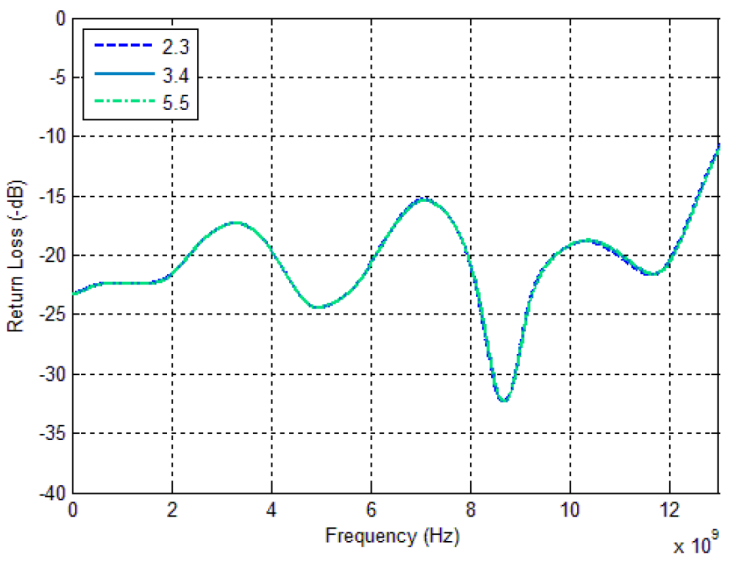


Figure 14. Active port return loss vs. V_{DD} (RF1 active)

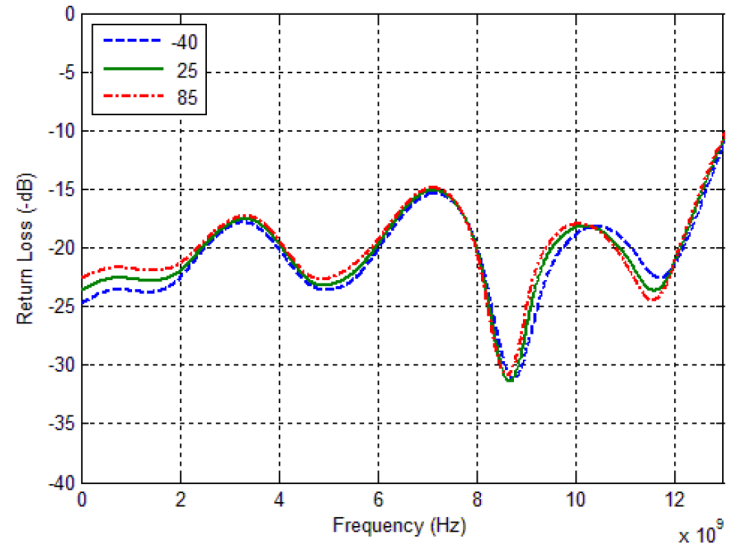


Figure 15. Active port return loss vs. temperature (RF2 active)

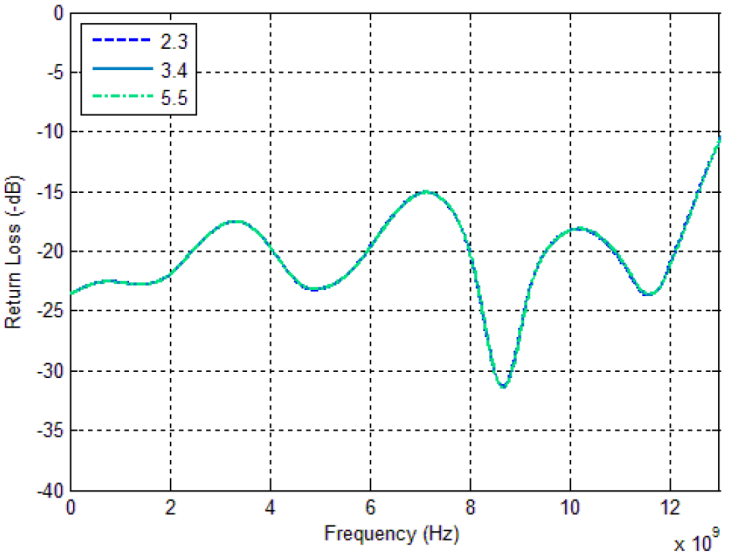


Figure 16. Active port return loss vs. V_{DD} (RF active)

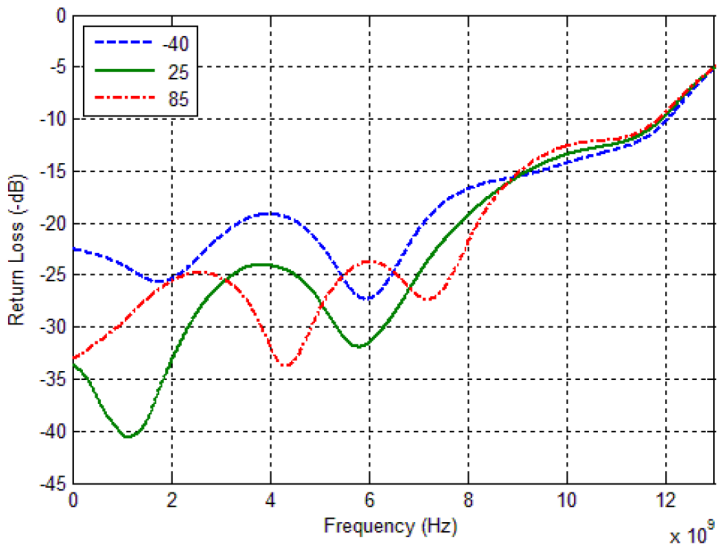


Figure 17. Terminated port return loss vs. temperature (RF1 active)

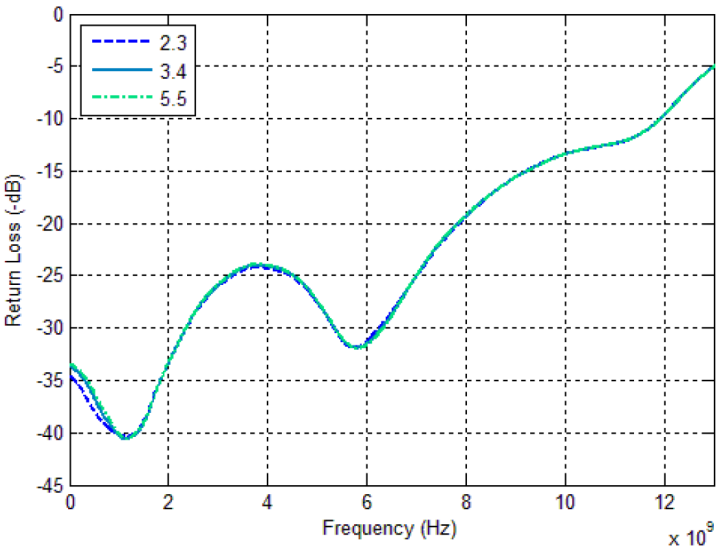


Figure 18. Terminated port return loss vs. V_{DD} (RF1 active)

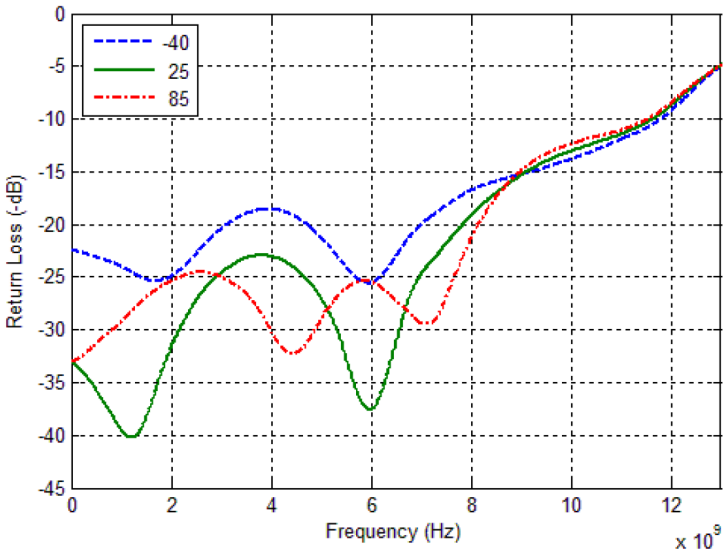


Figure 19. Terminated port return loss vs. temperature (RF2 active)

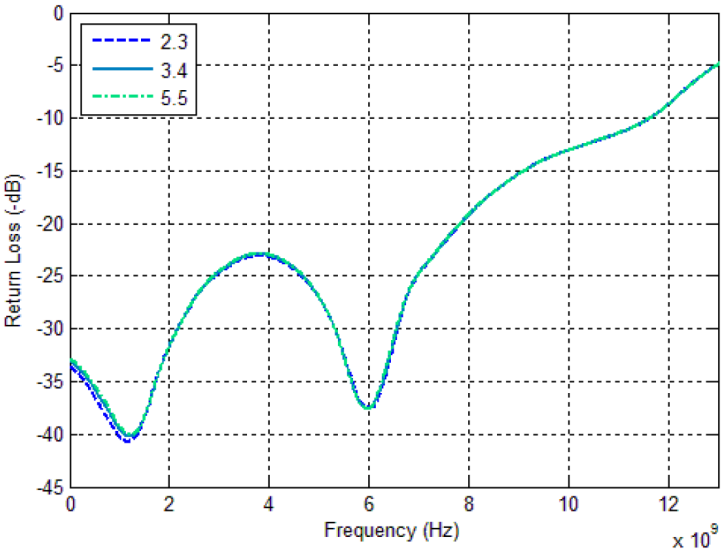


Figure 20. Terminated port return loss vs. V_{DD} (RF2 active)

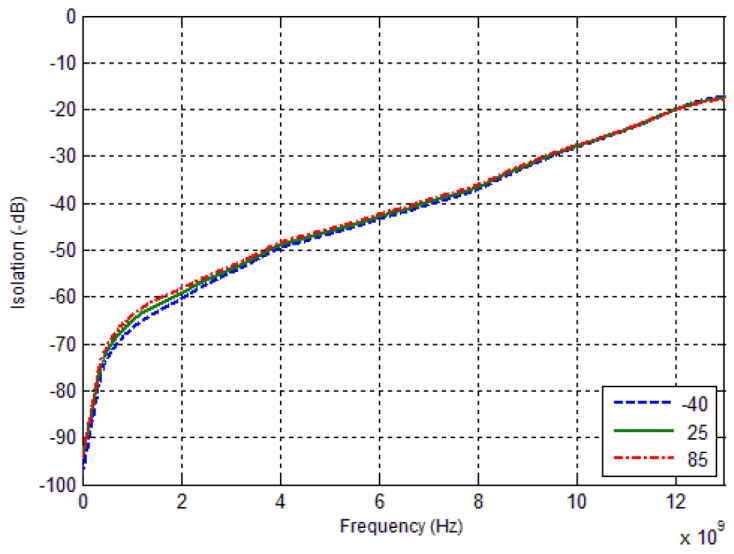


Figure 21. Isolation vs. temperature (RF1–RF2, RF1 active)

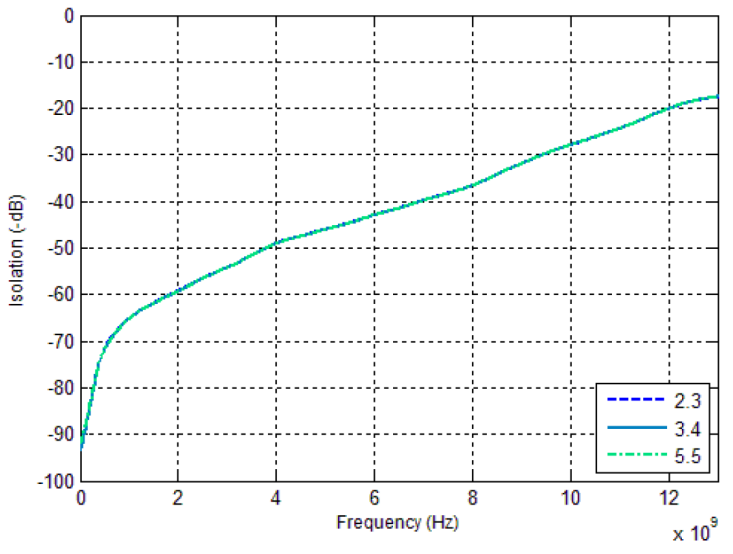


Figure 22. Isolation vs. V_{DD} (RF1–RF2, RF1 active)

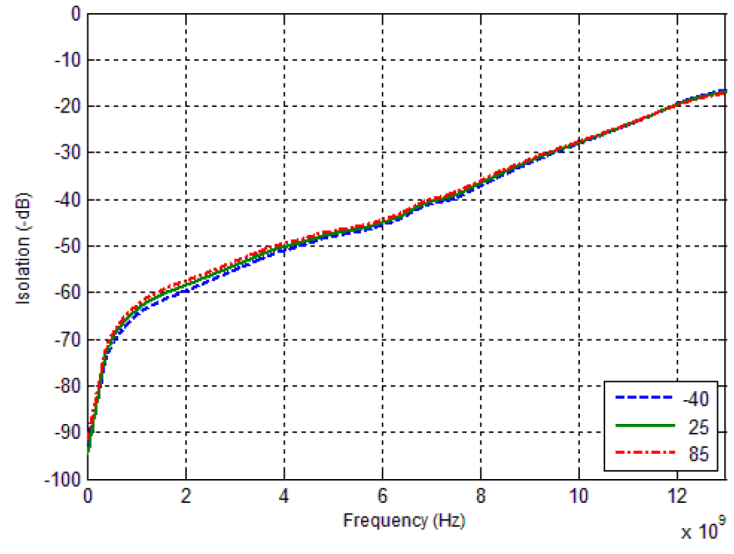


Figure 23. Isolation vs. temperature (RF2–RF1, RF2 active)

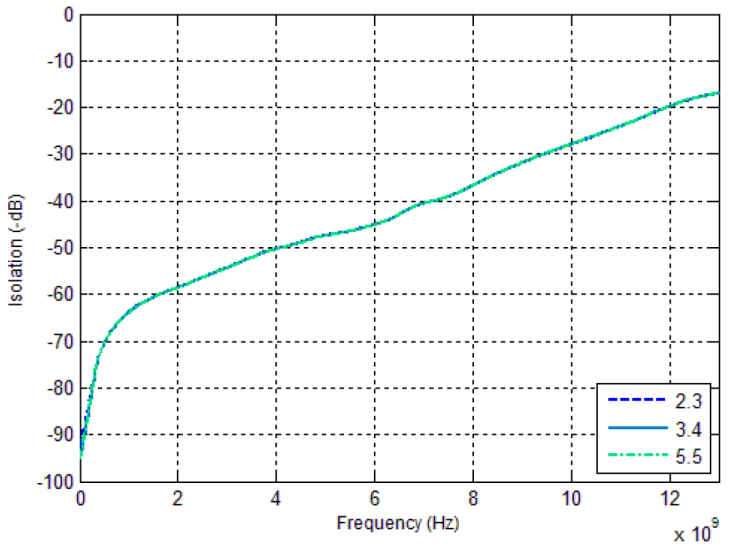


Figure 24. Isolation vs. V_{DD} (RF2–RF1, RF2 active)

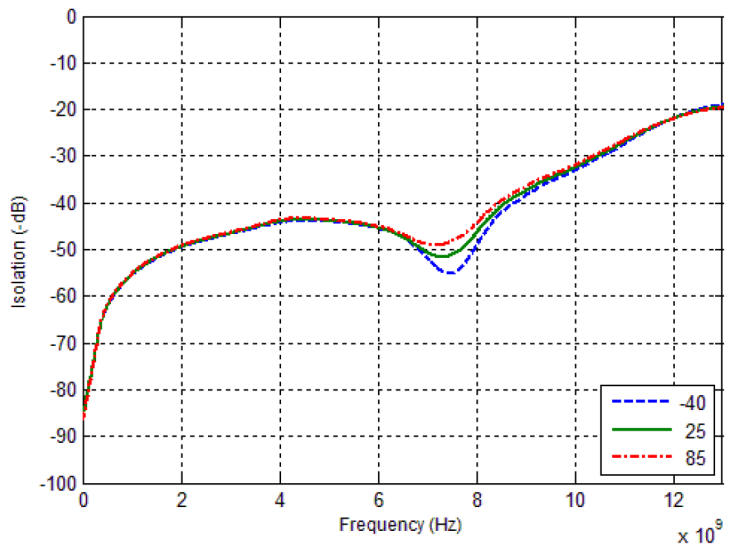


Figure 25. Isolation vs. temperature (RFC–RF2, RF1 active)

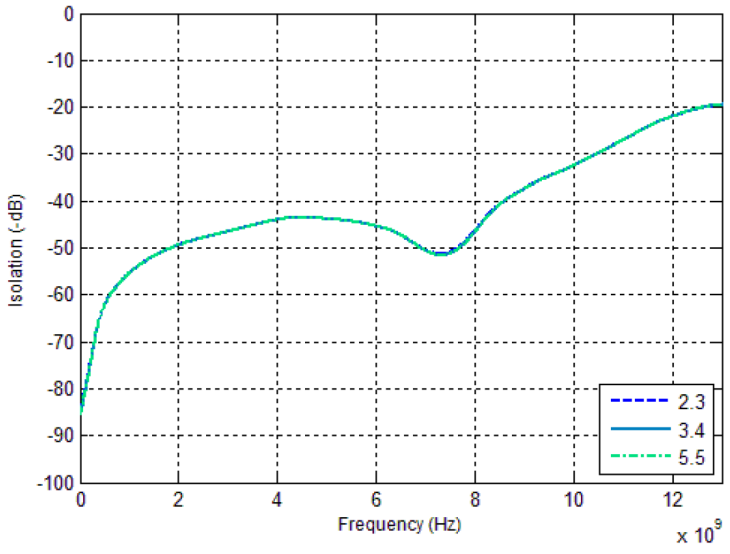


Figure 26. Isolation vs. V_{DD} (RFC–RF2, RF1 active)

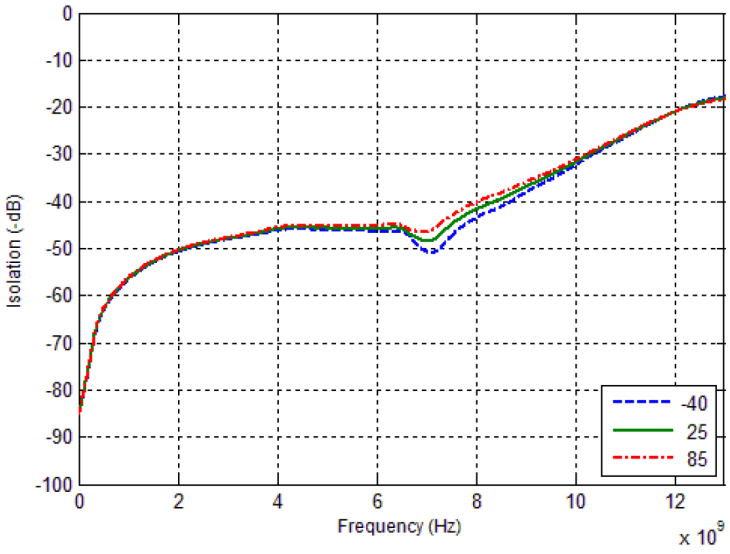


Figure 27. Isolation vs. temperature (RFC–RF1, RF2 active)

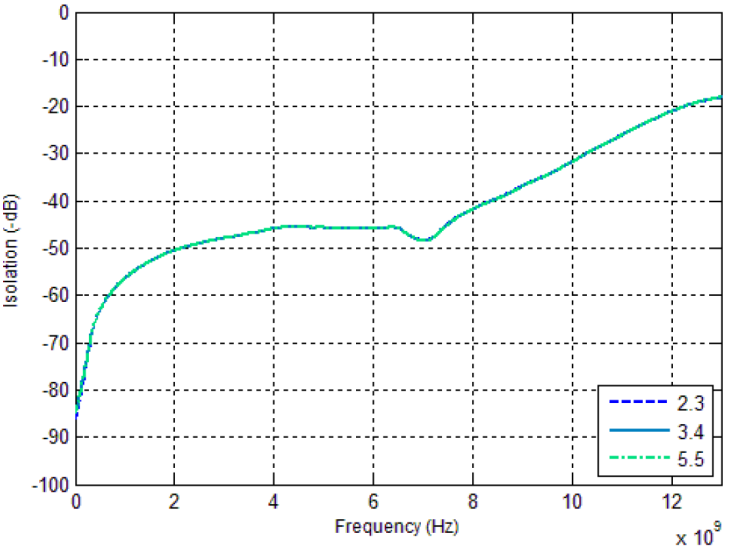


Figure 28. Isolation vs. V_{DD} (RFC–RF1, RF2 active)

Evaluation kit

pSemi designed the SPDT switch evaluation board to ease your evaluation of the pSemi PE42520. The RF common port is connected through a 50Ω transmission line via the SMA connector, J1. The RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which you can use to de-embed the loss of the PCB. Connector J4 provides the DC and digital inputs to the device.

To realize the true performance of the PE42520, design the PCB so that the RF transmission lines and the sensitive DC I/O traces are heavily isolated from one another.

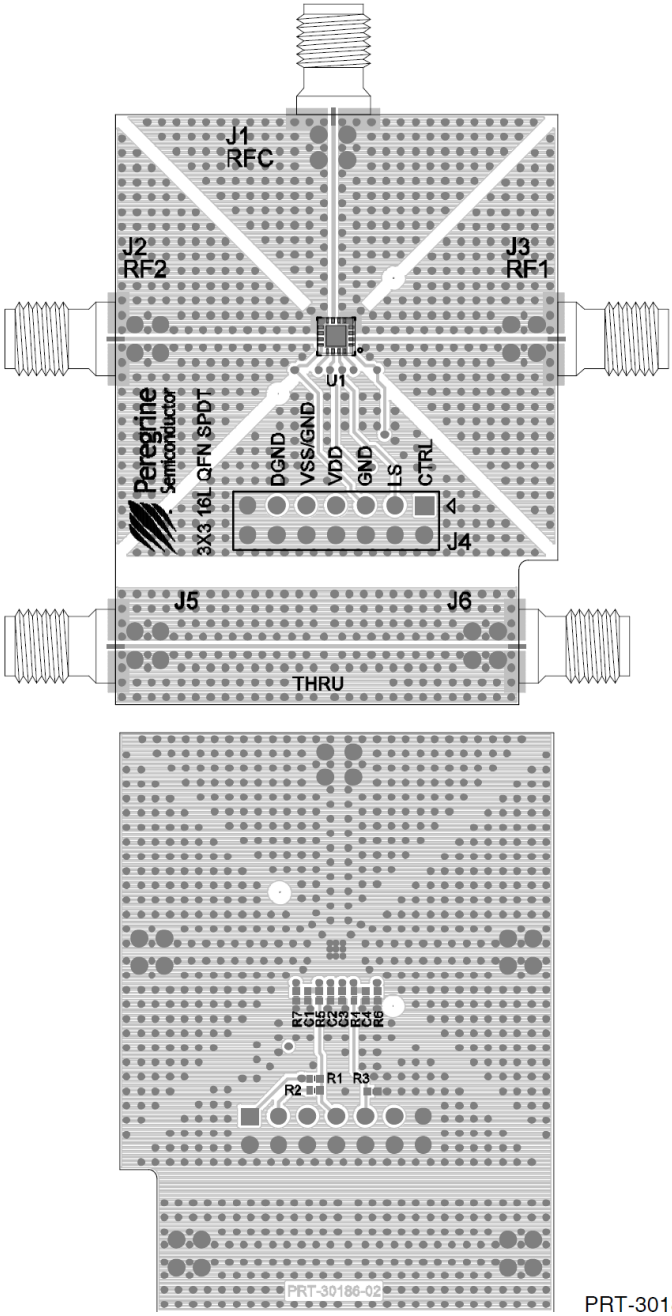


Figure 29. Evaluation board layouts

Evaluation board schematic

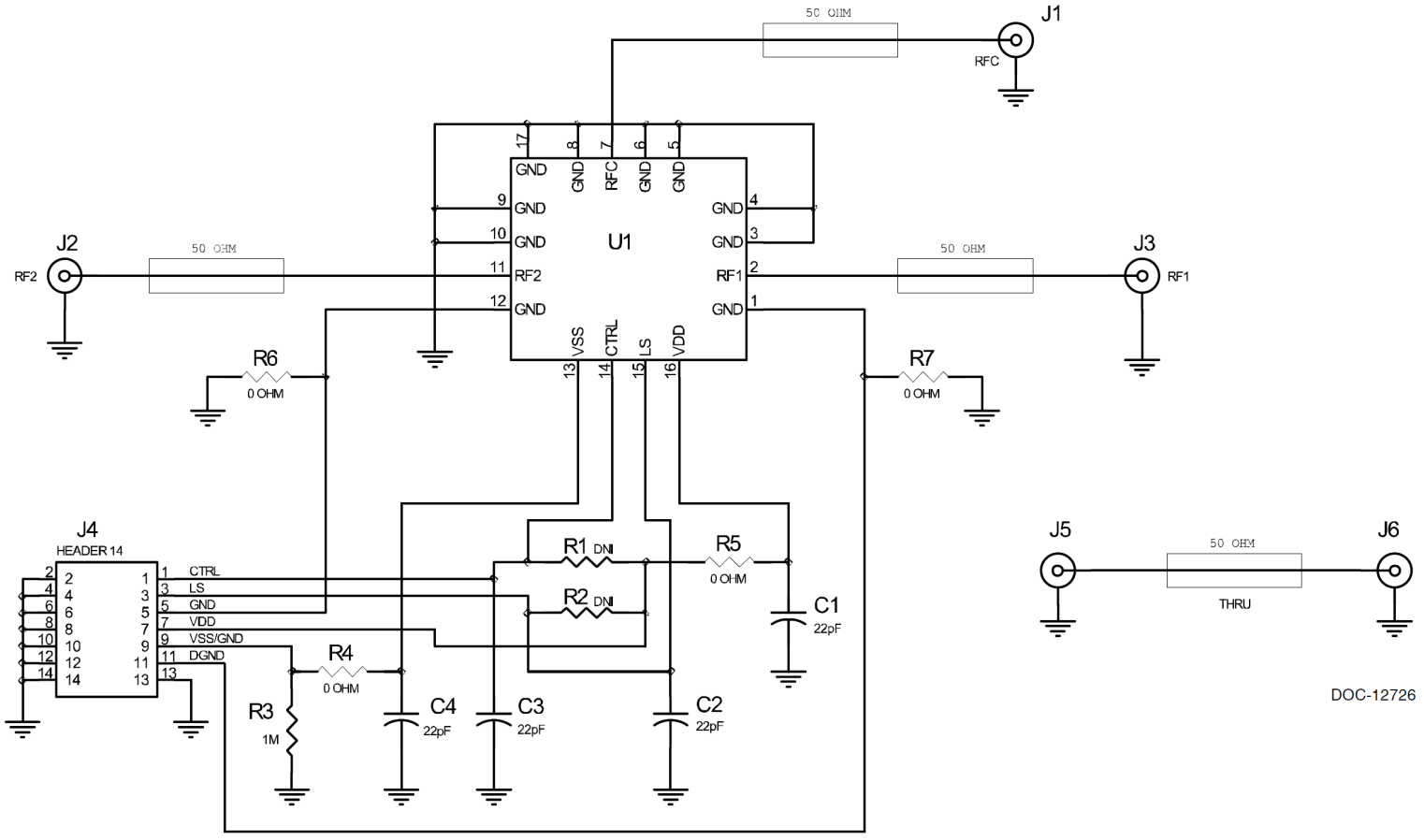


Figure 30. Evaluation board schematic

Use evaluation board PRT-30186-02.

The evaluation board contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

Pin information

Figure 31 shows the PE42520 pin map for the 16-lead 3 × 3 mm QFN package, and Table 5 lists the description for each pin.

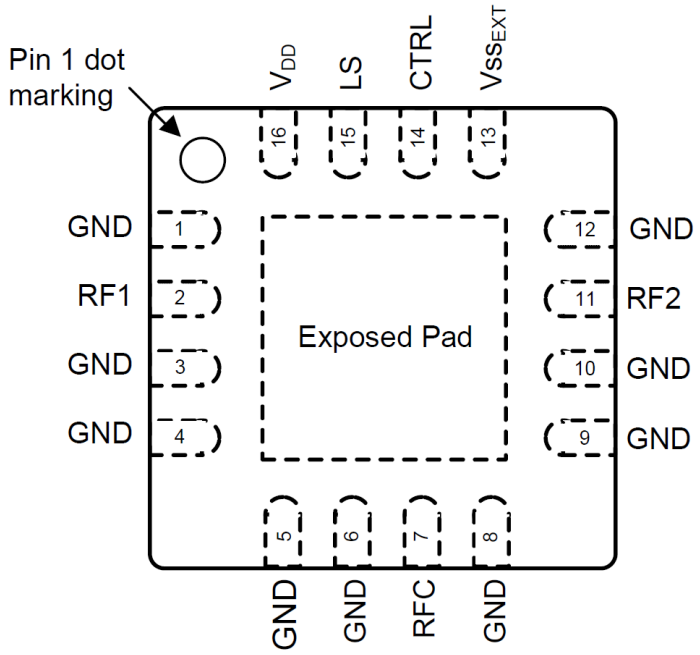


Figure 31. Pin configuration (top view)

Table 5. PE42520 pin descriptions

Pin no.	Pin name	Description
1, 3, 4, 5, 6, 8, 9, 10, 12	GND	Ground
2[1]	RF1	RF port 1
7[1]	RFC	RF common
11[1]	RF2	RF port 2
13[2]	V_{SS_EXT}	External V_{SS} negative voltage control
14	CTRL	Digital control logic input
15	LS	Logic select. Selects the definition for the CTRL pin (pin 14). For more information, see Table 4.
16	V_{DD}	Supply voltage
Pad	GND	Exposed pad. Ground for proper operation.

1. RF pins 2, 7 and 11 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Use V_{SS_EXT} (pin 13) to bypass and disable the internal negative voltage generator. Connect V_{SS_EXT} (pin 13) to GND (V_{SS_EXT} = 0V) to enable the internal negative voltage generator.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42520 moisture sensitivity level rating for the 16-lead 3 × 3 mm QFN package is MSL3.

Package drawing

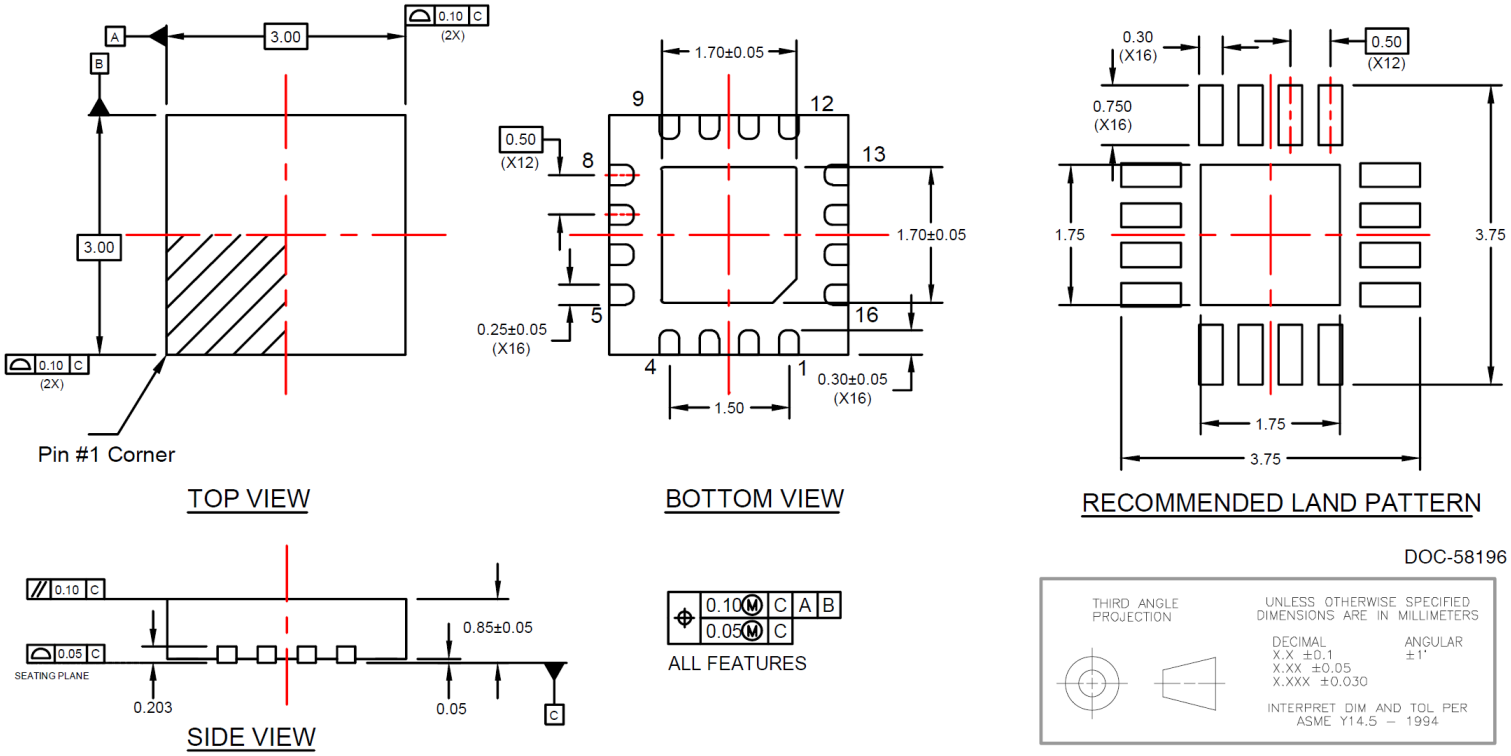
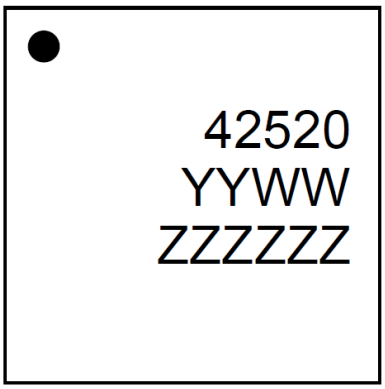


Figure 32. Package mechanical drawing for the 16-lead 3 × 3 mm QFN package

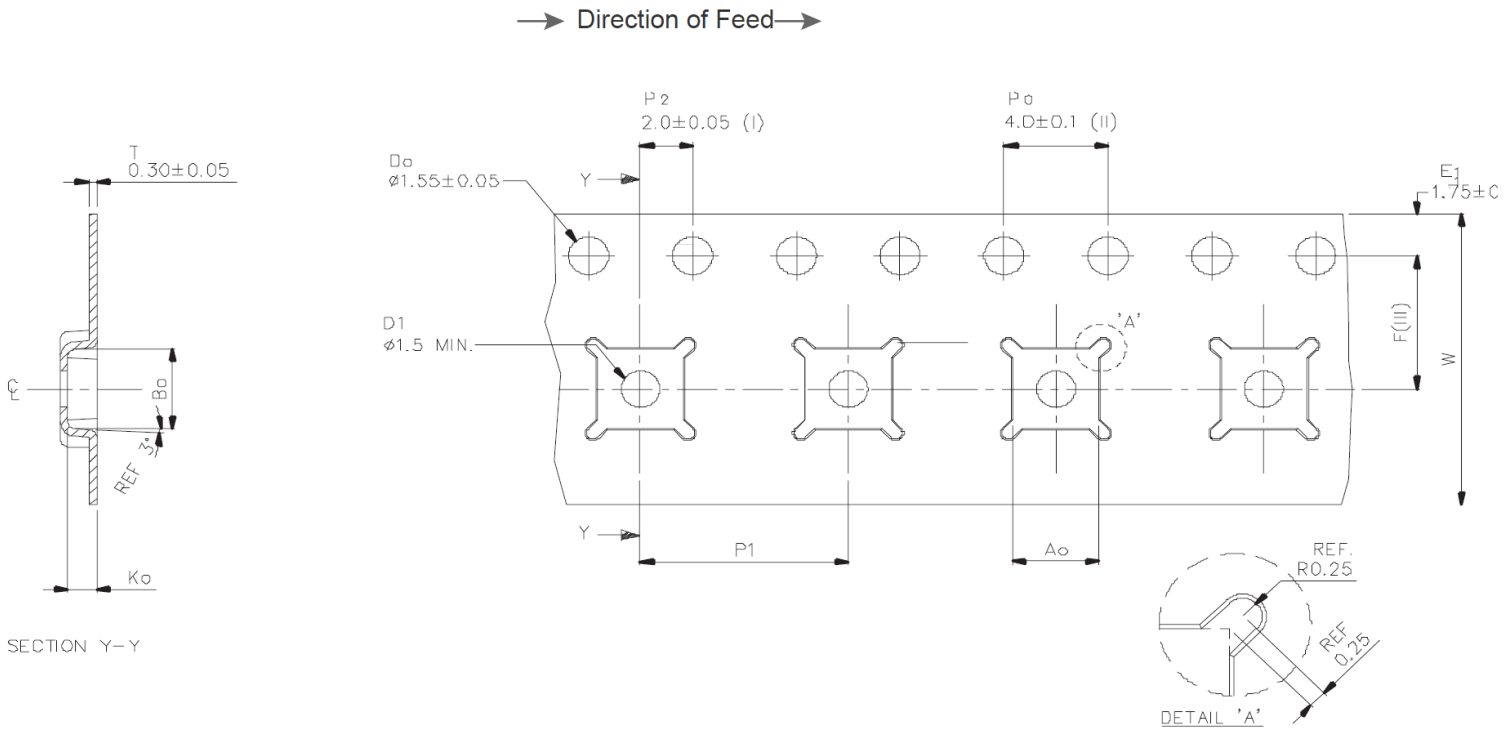
Top-marking specification



● = Pin 1 designator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZ = Assembly lot code (maximum six characters)

Figure 33. PE42520 package marking specification

Tape and reel specification

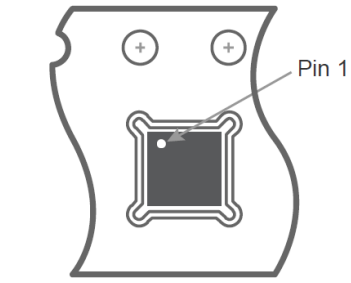


Ao	3.30 ± 0.1
Bo	3.30 ± 0.1
Ko	1.10 ± 0.1
F	5.50 ± 0.05
P1	8.00 ± 0.1
W	12.00 ± 0.3

Notes:

1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes ± 0.20.
3. Measured from centerline of sprocket hole to centerline of sprocket.

Dimensions are in millimeters unless otherwise specified.



Device Orientation in Tape

Figure 34. Tape and reel specification for the 16-lead 3 × 3 mm QFN package

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Ordering information

Order code	Description	Packaging	Shipping method
PE42520C-Z	PE42520 SPDT RF switch	Green 16-lead 3 × 3 mm QFN	3000 units/T&R
EK42520-03	PE42520 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
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