

PE4251

Document category: Product Specification

UltraCMOS® SPDT RF Switch, 10–4000 MHz, Absorptive



Features

- HaRP™ technology enhanced
- Low insertion loss: 0.60 dB @ 1000 MHz
- High isolation: 62 dB @ 1000 MHz
- P1dB typical: +30.5 dBm
- IIP3 typical: +59 dBm
- Fast switching time: 150 ns
- Flexible supply voltage: 3.3V ±10% or 5.0V ±10% supply (see [Table 2](#))
- Excellent ESD protection: 4000V HBM
- No blocking capacitors required
- Single pin or complementary control inputs
- Packaging: 8-lead MSOP with exposed paddle

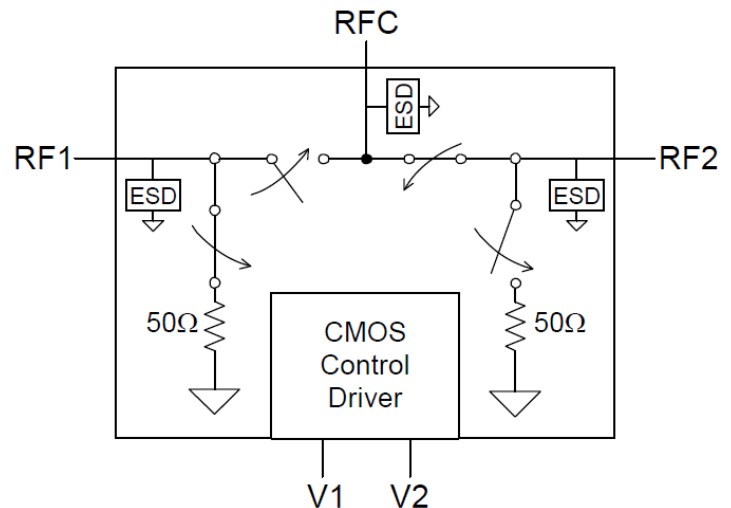


Figure 1. PE4251 functional diagram

Product description

The PE4251 is a HaRP™ technology-enhanced absorptive, single-pole, double-throw (SPDT) RF switch for use in general switching applications and mobile infrastructure. This device offers a flexible supply voltage of 3.3V or 5V, single-pin or complementary-pin control inputs, and 4000V ESD tolerance. It presents a simple alternative solution to PIN diode and mechanical relay switches.

The pSemi HaRP™ technology enhancements deliver high linearity and exceptional performance. It is an innovative feature of the UltraCMOS® process.

Absolute maximum ratings

 Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

 When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE4251 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	3	5.5	V
Voltage on any control input	V_I	-0.3	5.5	V
Storage temperature range	T_{ST}	-65	+150	°C
RF input power (50Ω): - 10 MHz–4 GHz, +85 °C - 50 MHz–4 GHz, +125 °C	P_{IN}	–	27 22	dBm
ESD voltage, HBM ⁽¹⁾	$V_{ESD,HBM}$	–	4000	V
ESD voltage, MM ⁽²⁾	$V_{ESD,MM}$	–	250	V

-  1. Human body model (MIL_STD 883 Method 3015).
2. Machine model (JEDEC JESD22-A115).

Recommended operating conditions

Table 2 lists the PE4251 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE4251 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage ^(*)	V _{DD}	3.0 4.5	3.3 5.0	3.6 5.5	V
Power supply current: - V _{DD} = V _{CTRL} = 3.3V - V _{DD} = V _{CTRL} = 5.0V	I _{DD}	–	55 75	60 80	μA
Control voltage high	V _{IH}	0.8 × V _{DD}	–	–	V
Control voltage low	V _{IL}	–	–	0.2 × V _{DD}	V
RF input power (50Ω): - 10 MHz–4 GHz, +85 °C - 50 MHz–4 GHz, +125 °C	P _{IN}	–	–	27 22	dBm
Operating temperature range	T _{OP}	-40	+25	+125	°C
Storage temperature range	T _{ST}	-65	+25	+150	°C



* Select the 3.3V or the 5.0V power supply range.

Electrical specifications

Table 3 lists the PE4251 key electrical specifications at +25 °C and $V_{DD} = 3.3V$ or $5V$.

Table 3. PE4251 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency ⁽¹⁾	–	–	10	–	4000	MHz
Insertion loss	RF1/RF2	10 MHz 1000 MHz 2000 MHz 3000 MHz 4000 MHz	–	0.55 0.60 0.75 0.75 1.0	0.60 0.70 0.85 0.90	dB
Isolation	RFC to RF1/ RF2	1000 MHz 2000 MHz 3000 MHz 4000 MHz	61 51 42	62 53 43 37	–	dB
Return loss	–	1000 MHz 2000 MHz 3000 MHz 4000 MHz	–	26 23 22 19	–	dB
Input 1-dB compression point ⁽²⁾	–	50–4000 MHz	–	30.5	–	dBm
Input IP3	–	50–4000 MHz, +18 dBm per tone, 5-MHz spacing	–	59	–	dBm
Switching time ⁽³⁾	–	50% CTRL to 10/90% RF	–	150	300	ns



1. The device linearity can start to degrade below 10 MHz.
2. The absolute maximum rating of $P_{IN} = 27$ dBm.
3. The PE4251 has a maximum 25-kHz switching rate.

Table 4 lists the PE4251 key electrical specifications at +125 °C and $V_{DD} = 3.3V$ or $5V$.

Table 4. PE4251 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	50	–	4000	MHz
Insertion loss	RF1/RF2	50 MHz 1000 MHz 2000 MHz 3000 MHz 4000 MHz	–	0.65 0.75 0.90 1.05 1.2	–	dB
Isolation	RFC to RF1/ RF2	1000 MHz 2000 MHz 3000 MHz 4000 MHz	–	62 52 43 36	–	dB
Return loss	–	1000 MHz 2000 MHz 3000 MHz 4000 MHz	–	24 23 19 18	–	dB
Input 1-dB compression point ⁽¹⁾	–	50–4000 MHz	–	30.5	–	dBm
Input IP3	–	50–4000 MHz, +18 dBm per tone, 5-MHz spacing	–	57	–	dBm
Switching time ⁽²⁾	–	50% CTRL to 10/90% RF	–	200	–	ns



1. The absolute maximum rating of $P_{IN} = 22$ dBm.
2. The PE4251 has a maximum 25-kHz switching rate.

SPDT control logic

Table 5. Single-pin control logic truth table

Control voltages	Signal path
Pin 1 (V2) = V _{DD} Pin 2 (V1) = High	RFC–RF1
Pin 1 (V2) = V _{DD} Pin 2 (V1) = Low	RFC–RF2

Table 6. Complementary-pin control logic truth table

Control voltages	Signal path
Pin 1 (V2) = Low Pin 2 (V1) = High	RFC–RF1
Pin 1 (V2) = High Pin 2 (V1) = Low	RFC–RF2

Control logic input

The PE4251 is a versatile RF CMOS switch that supports two operating control modes: single-pin control mode and complementary-pin control mode:

- Single-pin control mode: The switch operates with a single control pin (Pin 2) supporting a 3.3V or 5.0V CMOS logic input and requires a dedicated 3.3V or 5.0V power supply connection (Pin 1). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS microprocessor I/O port.
- Complementary-pin control mode: The switch operates using complementary control pins V1 and V2 (pins 2 and 1) that can be directly driven by 3.3V or 5.0V CMOS logic or a suitable microprocessor I/O port. This enables the PE4251 to operate in positive control voltage mode within the PE4251 operating limits.

Typical performance data

Figure 2–Figure 7 show the typical performance data.

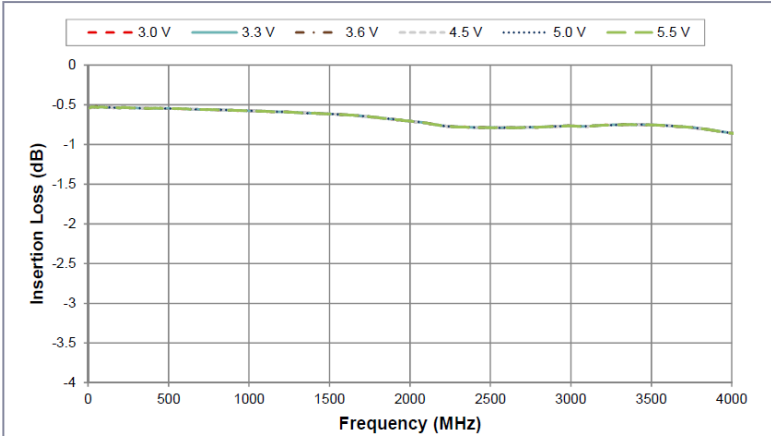


Figure 2. Insertion loss: RFC–RFx @ +25 °C

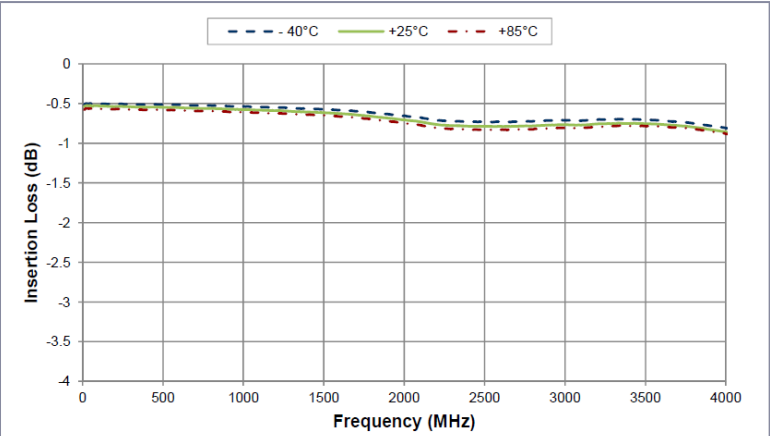


Figure 3. Insertion loss: RFC–RFx @ 3.3V

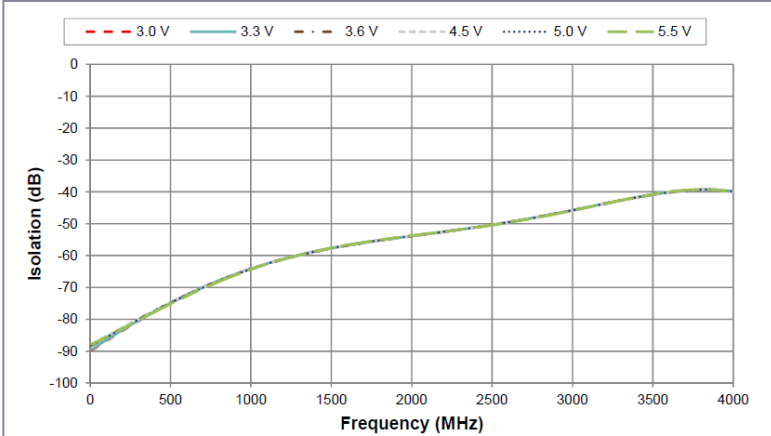


Figure 4. Isolation: RFC–RFx @ +25 °C

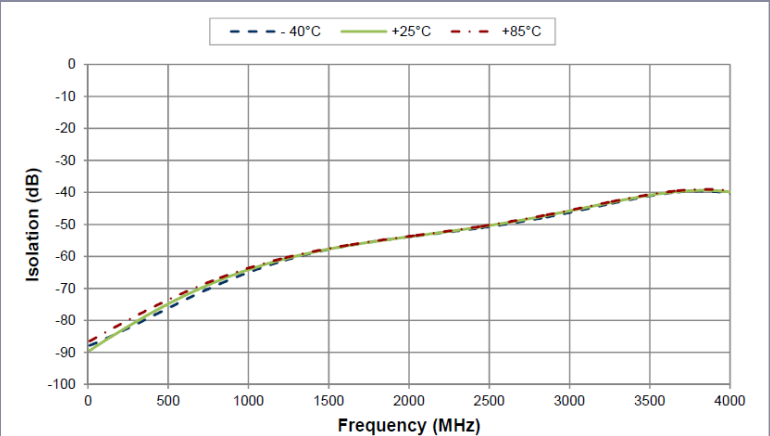


Figure 5. Isolation: RFC–RFx @ 3.3V

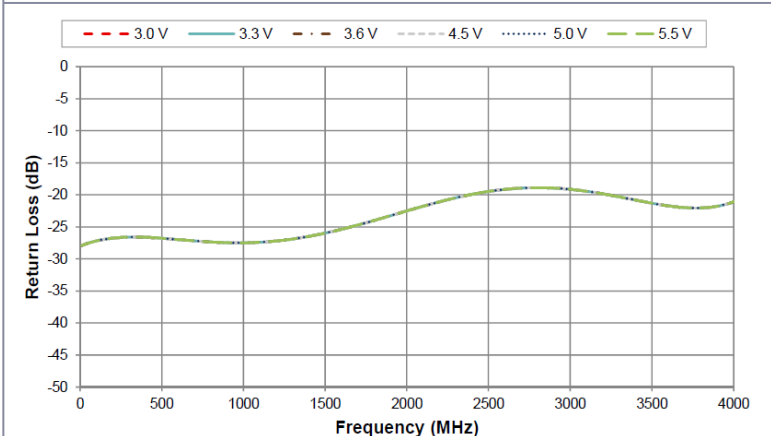


Figure 6. Return loss at active port @ +25 °C

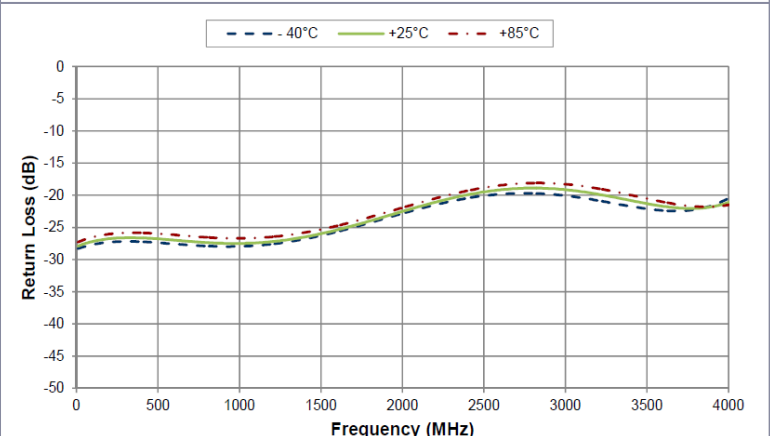


Figure 7. Return loss at active port @ 3.3V

Evaluation kit

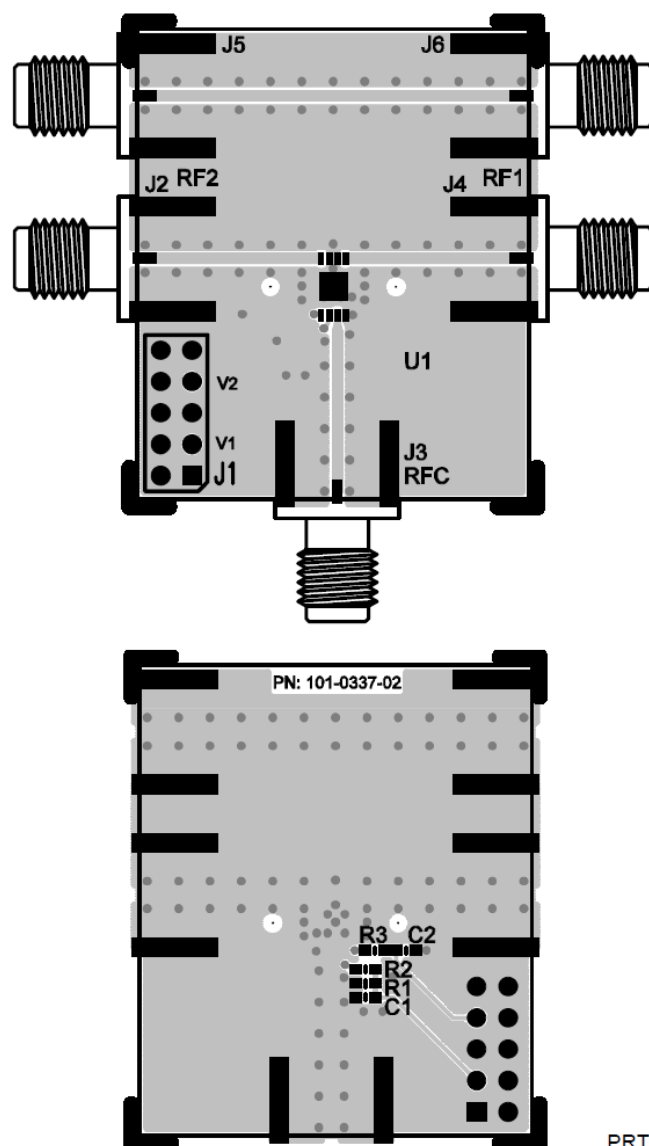
pSemi designed the SPDT switch evaluation board to ease your evaluation of the PE4251. The RF common port connects through a 50Ω transmission line to the bottom SMA connector, J3. Ports 1 and 2 connect through 50Ω transmission lines to two SMA connectors on either side of the board, J4 and J2. A through transmission line connects SMA connectors J5 and J6. You can use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.0322." The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.033," trace gaps of 0.010," dielectric thickness of 0.028," copper thickness of 0.0021," and ϵ_r of 4.3.

J1 provides a means for controlling the DC inputs to the device:

- J1–3 connects to the device V1 input (Pin 2).
- J1–7 connects to the device V2 input (Pin 1).

Footprints for decoupling capacitors are provided on both the V1 and V2 traces. You must determine the proper supply decoupling for your design application. Removing these components from the evaluation board has not been shown to degrade the RF performance.



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Figure 8. Evaluation board layout

Evaluation board schematic

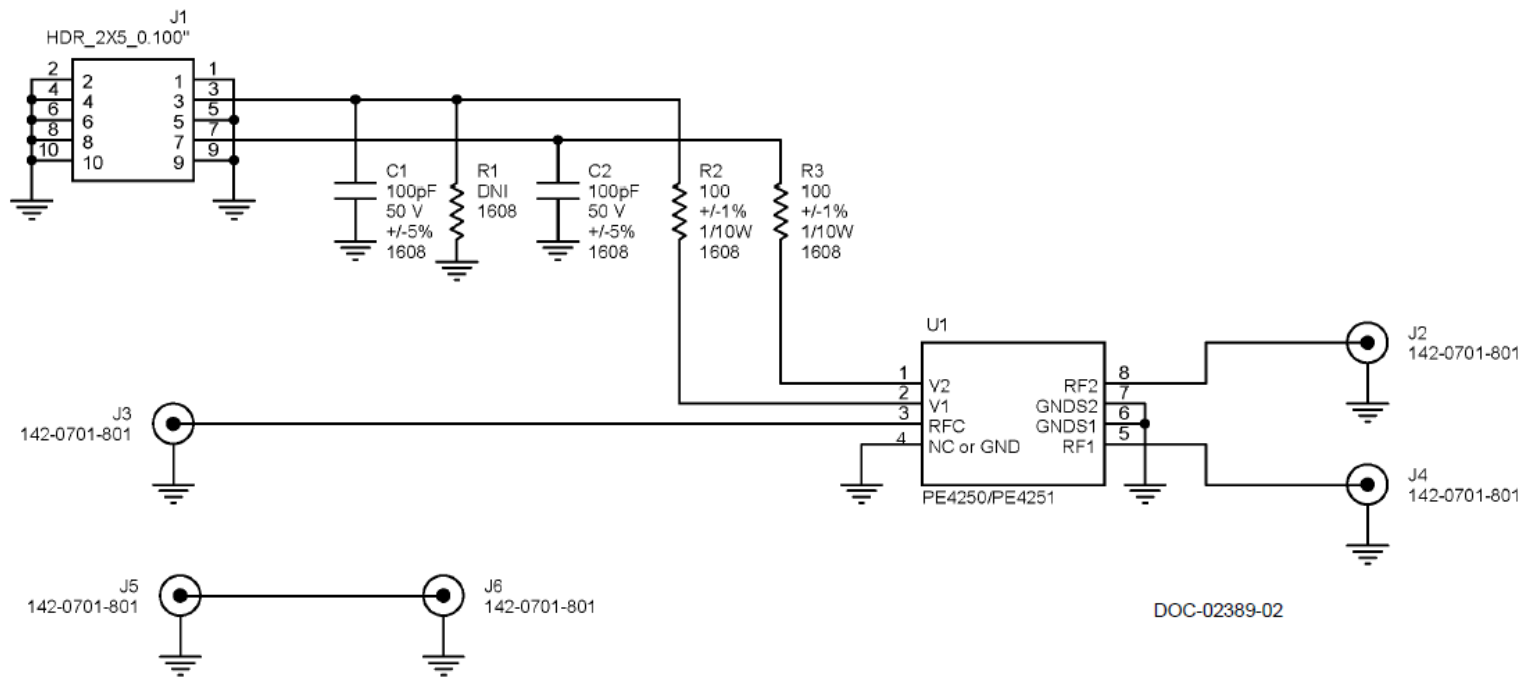


Figure 9. Evaluation board schematic

Pin information

Figure 10 shows the PE4251 pin map for the 8-lead MSOP package, and Table 7 lists the description for each pin.

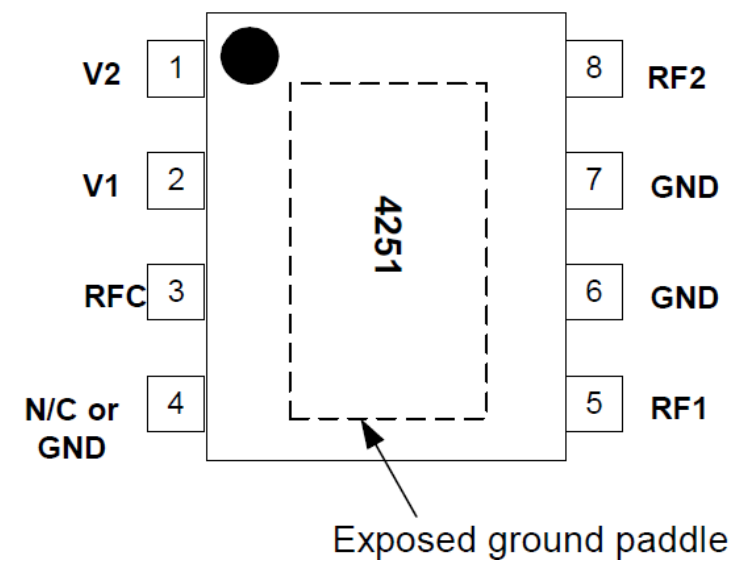


Figure 10. Pin configuration (top view)

Table 7. PE4251 pin descriptions

Pin no.	Pin name	Description
1	V2	This pin supports two interface options: • Single-pin control mode: A nominal 3V supply connection is required. • Complementary-pin control mode: A complementary CMOS control signal to V1 is supplied to this pin.
2	V1	Switch control input, CMOS logic level
3(*)	RFC	RF common
4	N/C or GND	No connect or ground
5(*)	RF1	RF port 1
6, 7	GND	Ground connections. For the best performance, ensure that the traces are physically short and connected to the ground plane.
8(*)	RF2	RF port 2
Pad	GND	Exposed pad. Ground for proper operation.

i * RF pins 3, 5, and 8 must be DC blocked with an external series capacitor or held at 0 VDC.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
 - Package drawing
- Package marking
 - Tape-and-reel information

Moisture sensitivity level

The PE4251 moisture sensitivity level rating for the 8-lead MSOP package is MSL1.

Package drawing

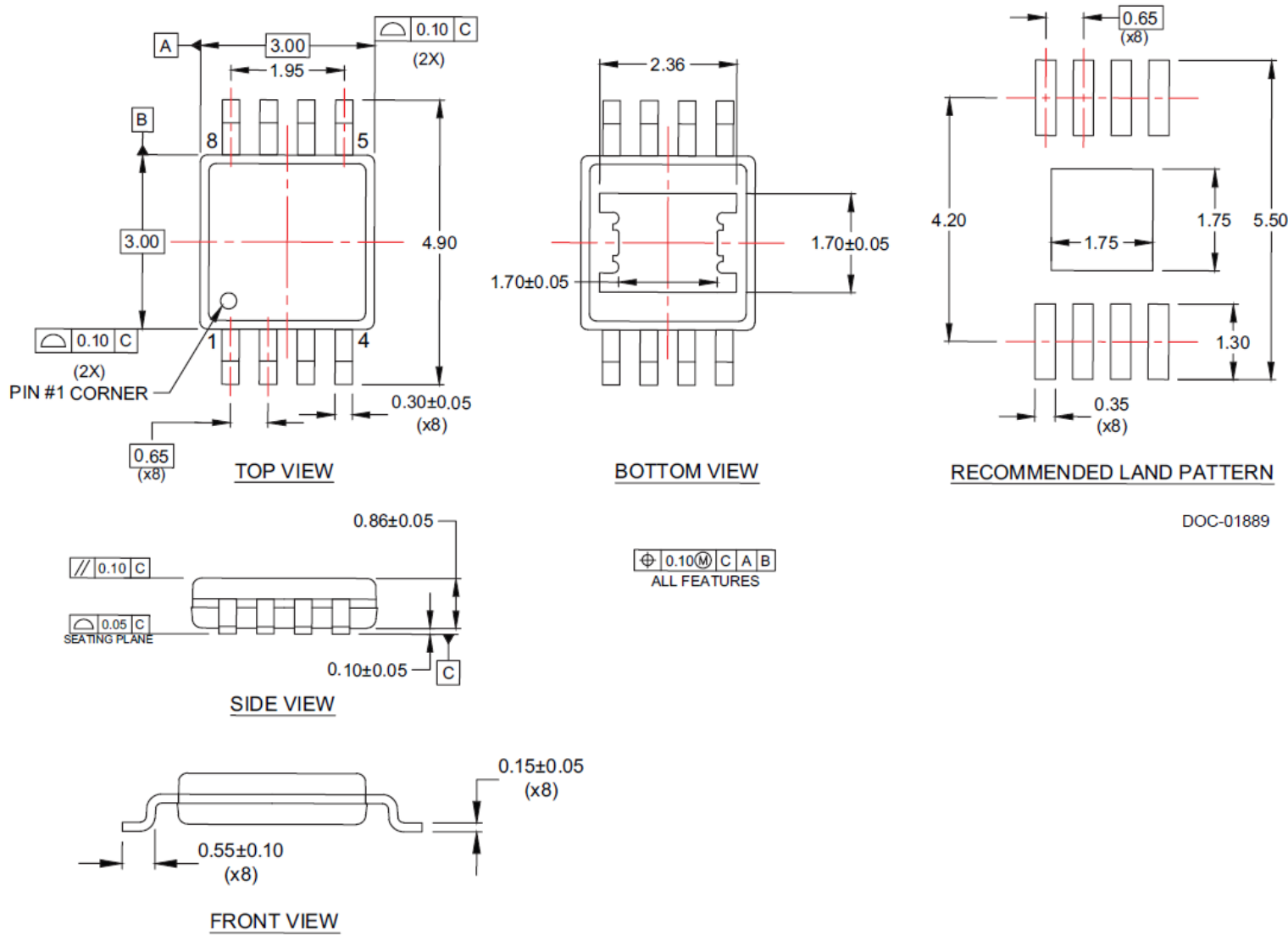
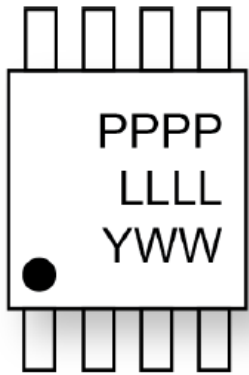


Figure 11. Package mechanical drawing for the 8-lead MSOP package

Top-marking specification



● = Pin 1 indicator
PPPP = Product part number (4251 for PE4251)
LLLL = Last four digits of the assembly lot number
YWW = Date code, last digit of the year, and work week

Figure 12. PE4251 package marking specification

Tape and reel specification

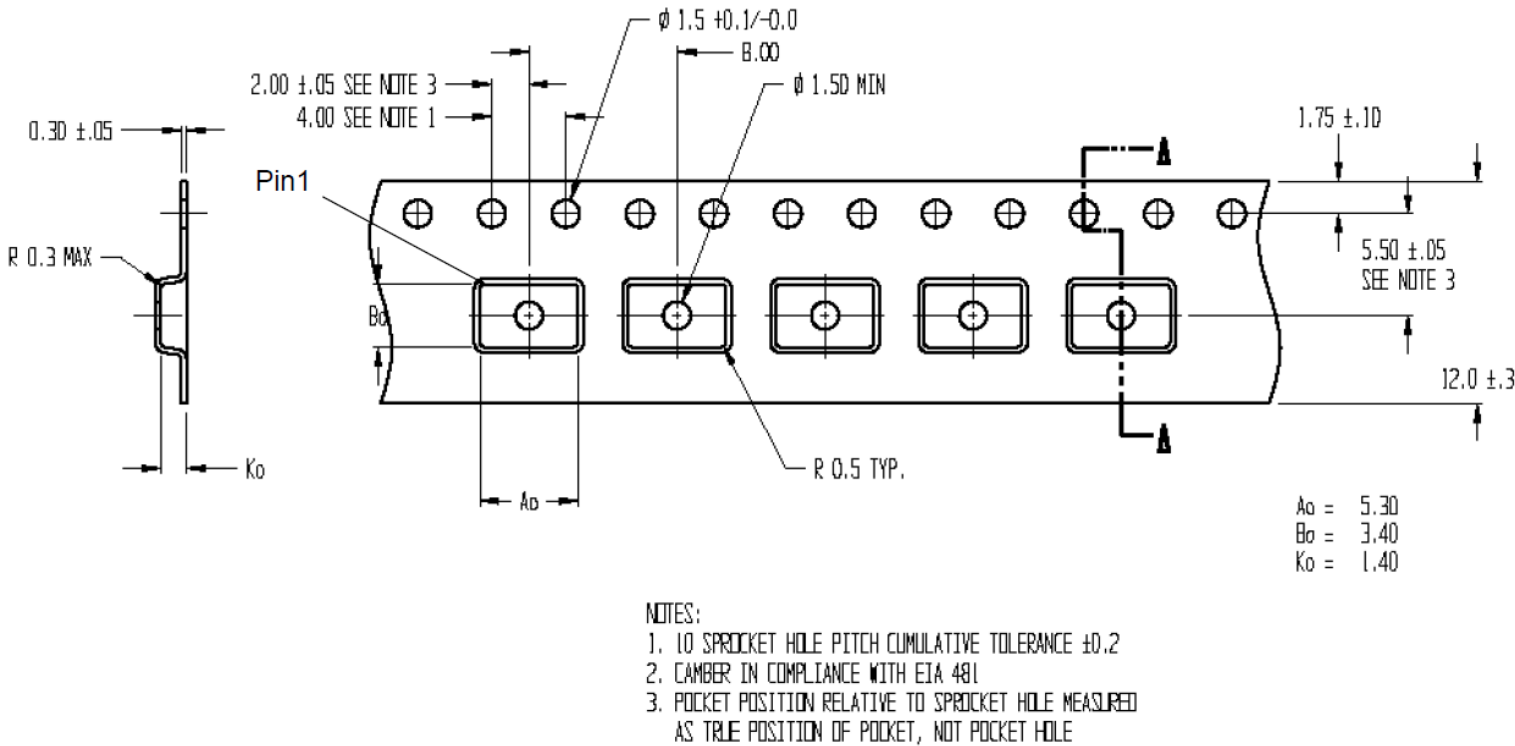


Figure 13. Tape and reel specification for the 8-lead MSOP package

Ordering information

Order code	Description	Packaging	Shipping method
PE4251MLI-Z	PE4251 SPDT RF switch	Green 8-lead MSOP, exposed paddle	2000 units/T&R
EK4251-01	PE4251 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
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