NSC74

Data Sheet

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1 General Description

NSC74 series are powerful sound controller chip by using ARM® Cortex-M0 32-bit microcontroller core. NSC74 series embed 256KB ~ 1,536 KB of non-volatile Flash memory with 6 KB boot loader, and 12 KB of SRAM. NSC74 provide peripheral devices including ADC, Timers, Peripheral Direct Memory Access (PDMA), IR carrier, Brown-Out Detector (BOD), Low Voltage Reset (LVR), and up to 30 GPIO to share with SPI, UART, Addressable LED, I2C, IR, PWM output, and CapTouch keys.
The NSC74 series product selection guide shown as below:

Part No.	VDD (V)	EF (KB)	Dur. (Sec) SR: 12KHz	GPIO	Interface	ADC (10 bit)	Cap Touch	MIC	Audio Output	ICE	Package
NSC74256L	1.8~5.5	256	128	30	SPI, UART, I2C, Addr. LED	5-ch	12	√	DPWM	√	LQFP48 (7x7mm^2)
NSC74512L		512	286								
NSC741K0L		1024	602								
NSC741K5L		1536	919								
NSC74256Z		256	128	19	SPI, UART, I2C	-	5				QFN32 (5x5mm^2)
NSC74512Z		512	286								
NSC741K0Z		1024	602								
NSC741K5Z		1536	919								

2 Feature

- **Core**
  - ARM® Cortex™-M0 core
  - One 24-bit System tick timer for operating system support
  - Single-cycle 32-bit hardware multiplier
  - NVIC (Nested Vector Interrupt Controller) for the interrupt inputs, each with 4 levels of priority
  - Serial Wire Debug (SWD) supports with 2 watch-points and 4 breakpoints
- **Power Management**
  - Operating voltage range: 1.8V to 5.5V (not include ADC and PGC)
  - Power Management Unit (PMU) provides different levels of power control
  - Deep Power Down (DPD) mode with specific register retention is the lowest power state (typically <1uA)
  - Wakeup from DPD via LIRC timed operation
  - Standby Power Down (SPD or STOP) mode is the lowest power state with keeping RAM (typically < 5uA) and with only LXT or LIRC is operating (typically < 7uA)
  - Wakeup from SPD can be from any GPIO, RTC, WDT and CapTouch interrupts
  - Fast wake-up mechanism, 20uS CPU can run instruction
- **Flash EPROM Memory**
  - 256KB ~ 1536 KB Flash EPROM for program code and data storage
  - Additional 6 KB of Flash can be configured as boot sector for ISP loader
  - Support ISP and ICP code update
  - 512 Byte page erase for embedded Flash
  - Configurable boundary to delineate code and data flash

- Support 2 wire In-Circuit-Programming (ICP) update from SWD ICE interface

- **SRAM Memory**
  - 12KB embedded SRAM
- **Clock Control**
  - Built-in high speed (HIRC, 39.936MHz, factory trimmed within +/- 1% @ normal temperature) and low speed (LIRC, 10KHz) oscillators, no external components necessary.
  - External 32 KHz crystal/resonator input
- **GPIO**
  - Max. 30 GPIO can be configured individually for below I/O modes:
    - ✓ Input with pull-up option (150KΩ, 1.0MΩ at VDD 4.5V)
    - ✓ Push-Pull output
    - ✓ Open-Drain output
  - Schmitt trigger input and slew rate selectable by quad
  - Each I/O pin can be configured as interrupt/wake-up source with edge/level setting
  - Support IR carrier generation circuit for simplifying firmware IR application
- **Support 12 H/W Cap Touch with Touch wake-up**
- **ADC**
  - 5-ch external single end input, 10-bit SAR ADC
  - Programmable gain amplifier with 64 steps from -18dB to 45dB in 1dB step size.
  - PDMA support for minimal CPU intervention.
  - Conversion rate is 500KHz @ 3.0V, and 250KHz @ 2.4V
- **Differential Audio PWM Output (DPWM)**
  - Direct connection of speaker
  - 0.5W drive capability into 8Ω load @ 5V
  - Configurable up-sampling to support sample rates from 8 ~ 24 KHz
  - PDMA support for minimal CPU intervention
  - 14 bit DPWM
- **UART**
  - UART ports with flow control (TX, RX)
  - 4 Byte FIFO
  - Programmable baud-rate
- **I2C**
  - Master Mode
- **PDMA**
  - 2-channel DMAs support data transfer between SRAM and peripherals of DPWM, ADC, SPI
- **Addressable LED Interface**
- **Timers**
  - Three timers with 8-bit pre-scalar and 16-bit resolution

- Counter auto-reload.
- IR carrier generator
- One fixed frequency timer

- **Watch Dog Timer**
  - Multiple clock sources
  - 8 selectable time-out periods from micro seconds to seconds (depends on clock source)
  - WDT can wake-up power down/sleep.
  - Interrupt or reset selectable on watchdog time-out.
- **RTC Timer**
  - Clock from LIRC 10KHz or LXT 32KHz
  - Selectable interrupt frequencies (0.25, 0.5, 1, 2, 4, 8, 16, 32 Hz based on LXT 32KHz)
  - Support wake-up function.
- **Two sets of PWM/Capture**
  - Built-in one 16-bit timer and four 16-bit comparators for 4 or 8 PWM outputs as a set
  - 2 sets support up to 12 individual PWM outputs
  - The PWM generator equipped with a clock source selector, a clock divider, an 8-bit pre-scalar for complementary PWM
  - PWM interrupt synchronous to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) provide rising/falling capture inputs
  - Support Capture interrupt
- **SPI**
  - Master up to 20 Mbps / Slave up to 8 Mbps
  - Support MICROWIRE/SPI master/slave mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - 2 slave/device select lines when used in master mode
  - Two 32-bit buffer or PDMA support for burst transfers
- **Brown-Out Detector (BOD)**
  - With 16 levels: 1.8V / 1.9V / 2.0V / 2.1V / 2.2V / 2.4V / 2.6V / 2.8V / 3.0V / 3.1V / 3.4V / 3.6V / 3.7V / 3.9V / 4.2V / 4.6V
  - Supports BOD Interrupt
- **Low Voltage Reset: 1.6V**
- **Package Form: (Package is Halogen-free, RoHS-compliant and TSCA-compliant)**
  - QFN32 (5 x 5 mm^2): 19 I/O
  - LQFP48 (7 x 7 mm^2): 30 I/O

3 PAD Description

LQFP48 Pin No.	QFN32 Pin No.	Name	Type	Alt CFG	Description
3	2	RESETB	I		Reset input, low active, internal pull-high
4	3	ICE_DAT	I/O	0	General purpose input/output pin; port A, bit7 SWD Interface, Serial Data
5	4	GPB5	I/O	0	General purpose input/output pin, port B, bit5
		SDOUT	O	1	Data output of 1-wire addressable LED
		IR	O	2	IR carrier generator based on Timer1 interval
		SDO	O	3	Data output of 2-wire addressable LED
6	-	VSSPST	P		Digital ground, connect to VSS
7	5	VSS	P		Digital ground
8	-	GPB0	I/O	0	General purpose input/output pin; port B, bit0
		PWM00	O	2	PWM0 channel 0 output
9	6	VDDL	P		Regulator output decoupling pin for core logic. A 1uF cap returning to VSS must be placed on it.
10	7	VDD	P		Main Digital Power Supply
11	-	VDDPST	P		Digital power, connect to VDD
13	8	AVDD	AP		Power Supply for Analog Circuitry
14	9	GPA15	I/O	0	General purpose input/output pin; port A, bit15
		PGCVMID	AO	1	Mid Rail Reference, Connect 4.7uF to AVSS
15	10	GPA12	I/O	0	General purpose input/output pin; port A, bit12
		MICBIAS	AO	1	Microphone Bias Output
16	-	GPA11	I/O	0	General purpose input/output pin; port A, bit11
17	11	GPA14	I/O	0	General purpose input/output pin; port A, bit14
		MICN	AI	1	Negative Microphone Input
18	12	GPA13	I/O	0	General purpose input/output pin; port A, bit13
		MICP	AI	1	Positive Microphone Input
19	13	AVSS	AP		Ground for Analog Circuitry
20	14	GPA0 (AIN0)	I/O	0	General purpose input/output pin; port A, bit0 ADC input channel 0
		PWM00	O	1	PWM0 channel 0 output
21	-	GPA1 (AIN1)	I/O	0	General purpose input/output pin; port A, bit1 ADC input channel 1
		PWM01	O	1	PWM0 channel 1 output
22	-	GPA2 (AIN2)	I/O	0	General purpose input/output pin; port A, bit2 ADC input channel 2
		PWM02	O	1	PWM0 channel 2 output
23	-	GPA3 (AIN3)	I/O	0	General purpose input/output pin; port A, bit3 ADC input channel 3
		PWM03	O	1	PWM0 channel 3 output
24	-	GPA4 (AIN4)	I/O	0	General purpose input/output pin; port A, bit4 ADC input channel 4
		PWM10	O	1	PWM1 channel 0 output
25	15	GPA5	I/O	0	General purpose input/output pin; port A, bit5
		PWM11	O	1	PWM1 channel 1 output
		TM0	I	2	Timer0 external clock input
		CXA0	I/O	3	CSCAN touch input channel 0
26	16	GPA10	I/O	0	General purpose input/output pin; port A, bit10
		CXA1	I/O	1	CSCAN touch input channel 1
27	17	GPB2	I/O	0	General purpose input/output pin; port B, bit2

LQFP48 Pin No.	QFN32 Pin No.	Name	Type	Alt CFG	Description
		CXA3	I/O	1	CSCAN touch input channel 3
		PWM02	O	2	PWM0 channel 2 output
28	18	GPB4	I/O	0	General purpose input/output pin, port B, bit4
		CXA5	I/O	1	CSCAN touch input channel 5
		CPR0	I	2	Capture input based on PWM0 timer
		CKO	O	3	Clock output of 2-wire addressable LED
29	-	GPB11	I/O	0	General purpose input/output pin, port B, bit11
		IR	O	1	IR carrier generator based on Timer1 interval
		CXA7	I/O	2	CSCAN touch input channel 7
30	-	GPB12	I/O	0	General purpose input/output pin; port B, bit12
		TM1	I	1	Timer1 external clock input
		CXA8	I/O	2	CSCAN touch input channel 8
31	-	GPB10	I/O	0	General purpose input/output pin, port B, bit10
		SPI_SS1	O	1	SPI Slave Select 1
		CXA6	I/O	2	CSCAN touch input channel 6
		PWM17	O	3	PWM1 channel 7 output
32	-	GPB13	I/O	0	General purpose input/output pin; port B, bit13
		CPR1	I	1	Capture input based on PWM1 timer
		CXA9	I/O	2	CSCAN touch input channel 9
33	19	GPB14	I/O	0	General purpose input/output pin; port B, bit14
		I2C_SCL	O	1	I2C0 Master Mode clock output
		CXA10	I/O	2	CSCAN touch input channel 10
34	-	GPB1	I/O	0	General purpose input/output pin; port B, bit1
		PWM01	O	2	PWM0 channel 1 output
35	20	GPB15	I/O	0	General purpose input/output pin; port B, bit15
		I2C_SDA	I/O	1	I2C0 Master Mode Data
		CXA11	I/O	2	CSCAN touch input channel 11
36	21	GPB3	I/O	0	General purpose input/output pin, port B, bit3
		CXA4	I/O	1	CSCAN touch input channel 4
		PWM03	O	2	PWM0 channel 3 output
37	-	VSSPST1	P		Digital ground, connect to VSS
38	22	ICE_CLK	I/O	0	General purpose input/output pin; port A, bit6 SWD Interface, Serial Clock
39	23	GPA8	I/O	0	General purpose input/output pin; port A, bit8
		UARTTX	O	2	UART Transmitter Serial Out
		X32I	I	3	32K Crystal Oscillator Input
40	24	GPA9	I/O	0	General purpose input/output pin; port A, bit9
		UARTRX	I	2	UART Receiver Serial In
		X32O	O	3	32K Crystal Oscillator Output
41	25	GPB9	I/O	0	General purpose input/output pin, port B, bit9
		SPI_SS0	I/O	1	SPI Slave Select 0
		I2C_SDA	I/O	2	I2C0 Master Mode Data
42	26	GPB8	I/O	0	General purpose input/output pin, port B, bit8
		SPI_MISO	I/O	1	SPI Master In Slave Out
		I2C_SCL	O	2	I2C0 Master Mode clock
		PWM16	O	3	PWM1 channel 6 output
43	27	GPB7	I/O	0	General purpose input/output pin, port B, bit7
		SPI_CLK	I/O	1	SPI Serial Clock
		UARTRX	I	2	UART Receiver Serial In
		PWM15	O	3	PWM1 channel 5 output

LQFP48 Pin No.	QFN32 Pin No.	Name	Type	Alt CFG	Description
44	28	GPB6	I/O	0	General purpose input/output pin, port B, bit6
		SPI_MOSI	I/O	1	SPI Master Out Slave In
		UARTTX	O	2	UART Transmitter Serial Out
		PWM14	O	3	PWM1 channel 4 output
45	29	VDDP	P		Power Supply for DPWM Speaker Driver
46	30	SPKN	O		Negative Speaker Driver Output
47	31	VSSP	P		Ground for DPWM Speaker Driver
48	32	SPKP	O		Positive Speaker Driver Output
1	1	VDDP	P		Power Supply for DPWM Speaker Driver

Note: AVDD, VDD, VDDPST must be same voltage level.

I: Input, O: Output, AI: Analog input, AO: Analog output, P: Power Pin, AP: Analog Power.

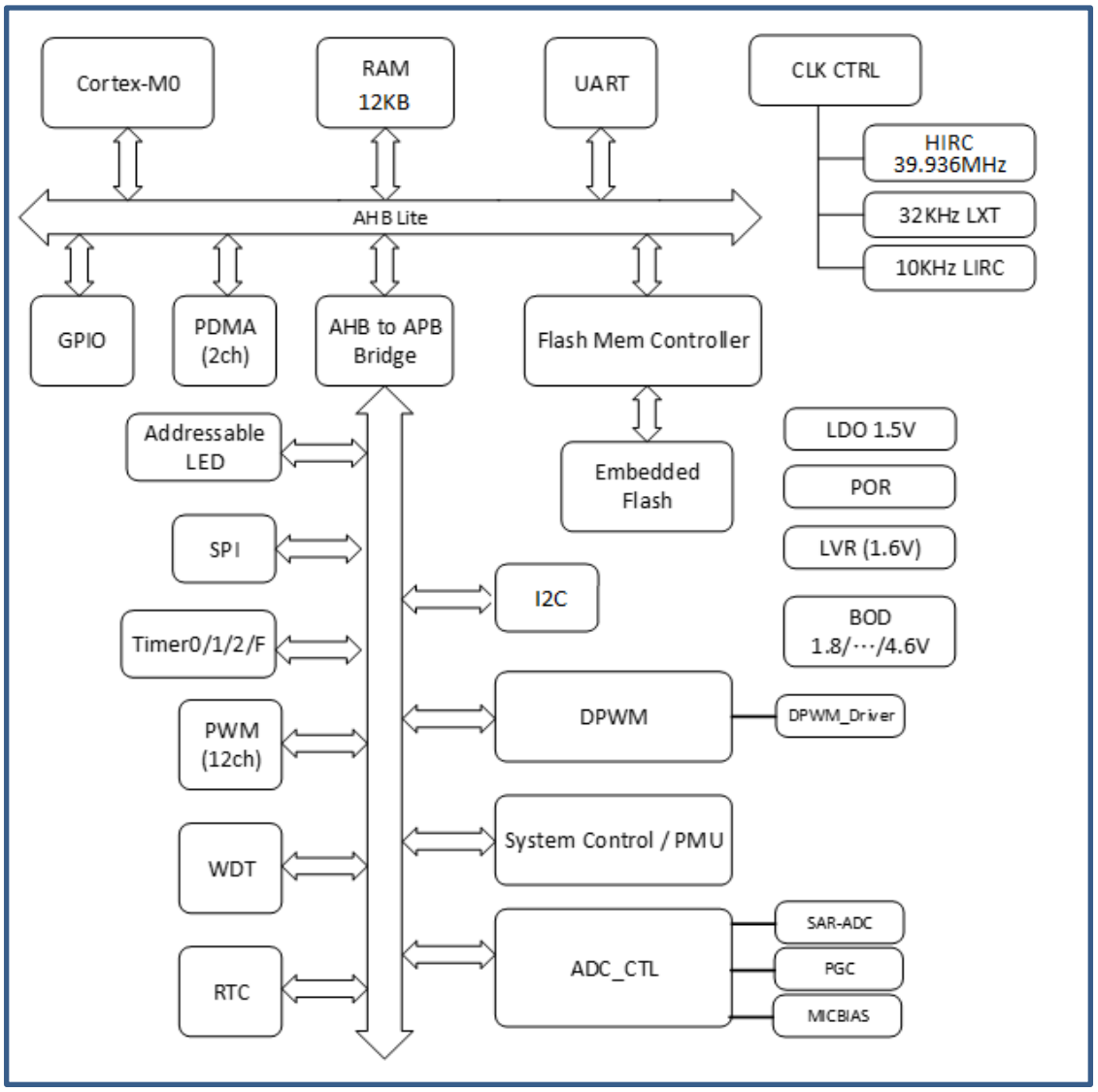
3.1 Alternative Function List of GPIO

GPIO	Power	ALT =1	I/O of ALT = 1	ALT =2	I/O of ALT = 2	ALT =3	I/O of ALT = 3	Special Modes
GPA0	VDD	PWM00	O					AIN0
GPA1	VDD	PWM01	O					AIN1
GPA2	VDD	PWM02	O					AIN2
GPA3	VDD	PWM03	O					AIN3
GPA4	VDD	PWM10	O					AIN4
GPA5	VDD	PWM11	O	TM0	I	CXA0	I/O	
GPA6	VDD	PWM12	O					ICE_CLK
GPA7	VDD	PWM13	O					ICE_DAT
GPA8	VDD			UARTTX	O	X32I	I	
GPA9	VDD			UARTRX	I	X32O	O	
GPA10	VDD	CXA1	I/O					
GPA11	AVDD							
GPA12	AVDD	MICBIAS	AO					
GPA13	AVDD	MICP	AI					
GPA14	AVDD	MICN	AI					
GPA15	AVDD	PGCVMID	AO					
GPB0	VDD			PWM00	O			
GPB1	VDD	CXA2		PWM01	O			
GPB2	VDD	CXA3	I/O	PWM02	O			
GPB3	VDD	CXA4	I/O	PWM03	O			
GPB4	VDD	CXA5	I/O	CPR0	I	CKO	O	
GPB5	VDD	SDOUT	O	IR	O	SDO	O	
GPB6	VDD	SPI_MOSI	I/O	UARTTX	O	PWM14	O	
GPB7	VDD	SPI_CLK	I/O	UARTRX	I	PWM15	O	
GPB8	VDD	SPI_MISO	I/O	I2C_SCL	O	PWM16	O	
GPB9	VDD	SPI_SS0	I/O	I2C_SDA	I/O			
GPB10	VDD	SPI_SS1	O	CXA6	I/O	PWM17	O	
GPB11	VDD	IR	O	CXA7	I/O			
GPB12	VDD	TM1	I	CXA8	I/O			

GPB13	VDD	CPR1	I	CXA9	I/O			
GPB14	VDD	I2C_SCL	O	CXA10	I/O			
GPB15	VDD	I2C_SDA	I/O	CXA11	I/O			

I: Input, O: Output, AI: Analog input, AO: Analog output
AVDD : Analog power domain.
VDD : Digital power domain.

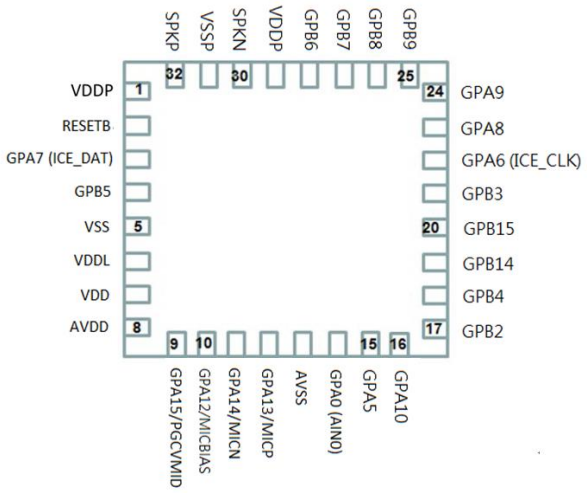
4 Block Diagram



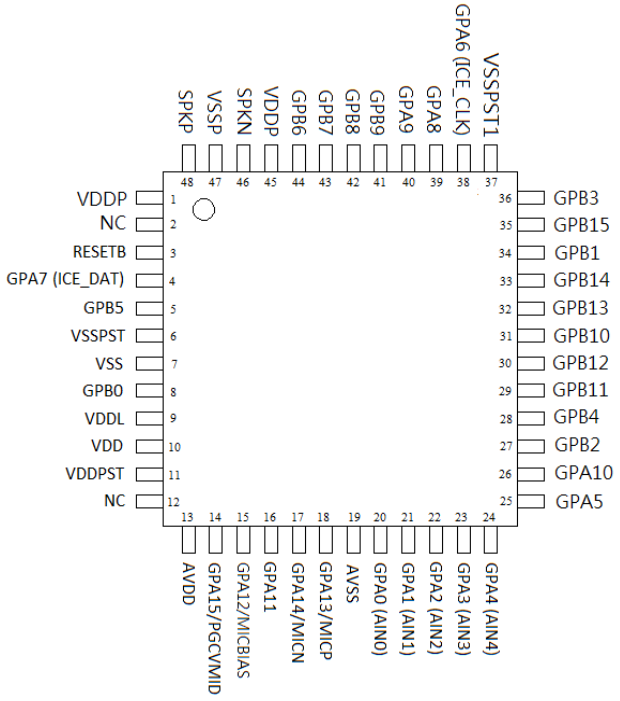
5 Package Information

5.1 Package PIN Assignment

NSC256 ~ NSC1K5
QFN32, 5 x 5 mm^2, 19 I/O

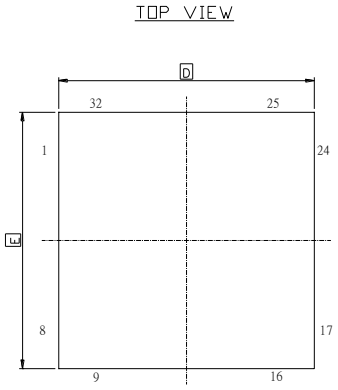


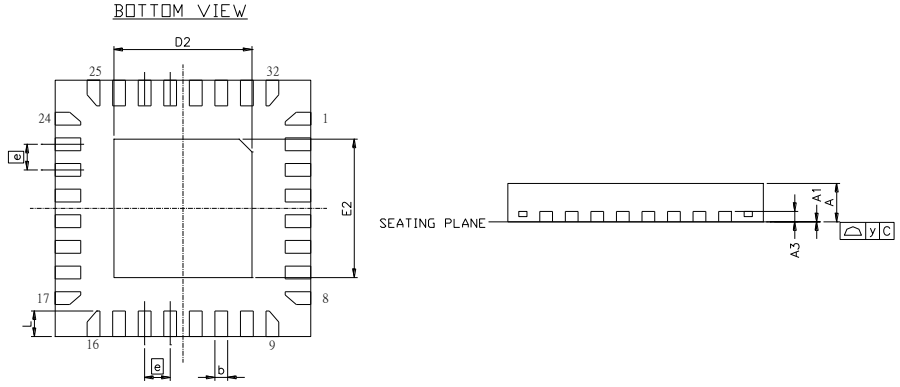
NSC256 ~ NSC1K5
LQFP48, 7 x 7 mm^2, 30 I/O



5.2 Package Dimension

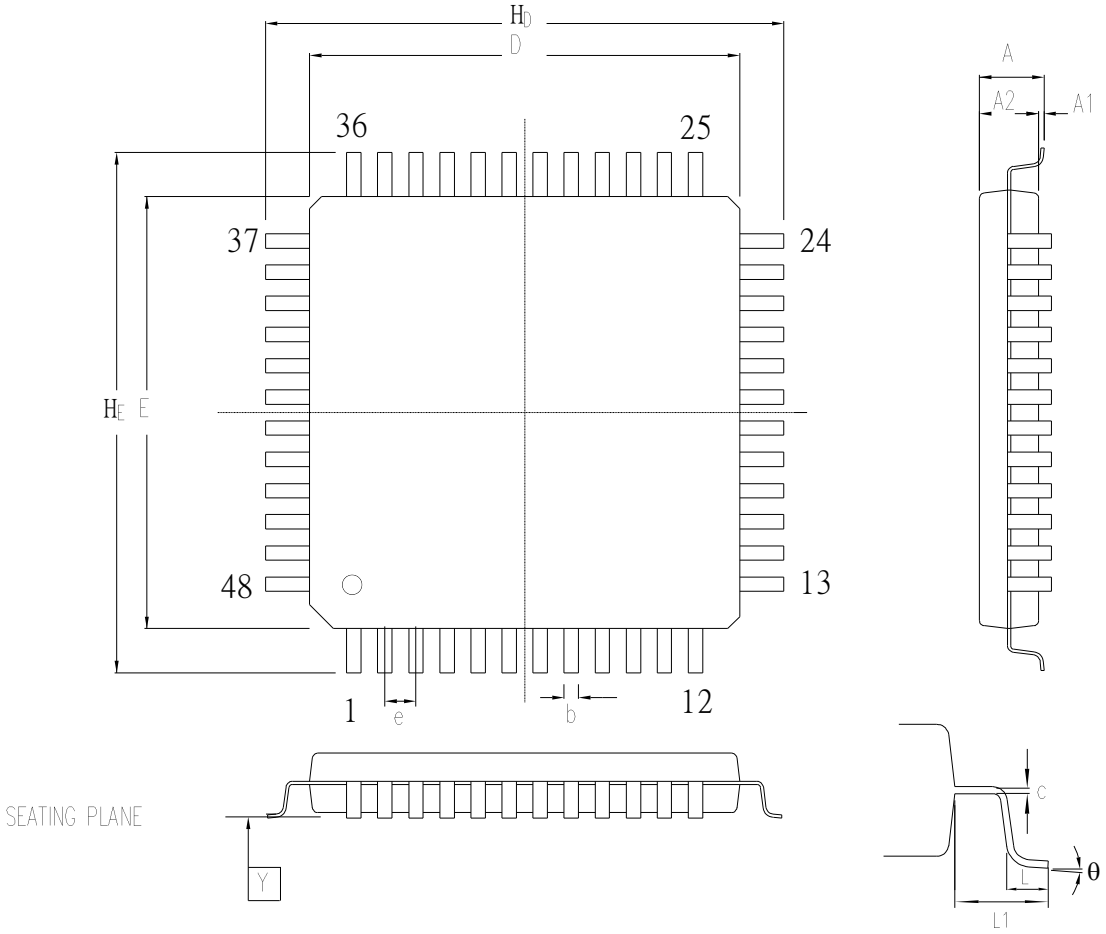
QFN32, 5 x 5mm^2





SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
D2	2.60	2.70	2.80	0.1024	0.1063	0.1102
E	5.00 BSC			0.197 BSC		
E2	2.60	2.70	2.80	0.1024	0.1063	0.1102
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

LQFP48, 7x7x1.4mm^2, footprint 2.0mm



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}			120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

6.2 DC Electrical Characteristics

(VDD-VSS=4.5V, TA = 25°C, No load unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	1.8		5.5	V	
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AVDD	1.8		5.5	V	
Supply Current at Normal Run Mode	I_{DD1}		15		mA	Enable all IP
	I_{DD1}		10		mA	Disable all IP
Supply Current at Idle Mode	I_{IDLE1}		7		mA	Enable all IP
	I_{IDLE2}		5		mA	Disable all IP
Supply Current at STOP Mode	I_{STP}		3	10	μA	Disable all IP, except LXT or LIRC is operating (Flash power off)
Deep Power Down (DPD) Mode	I_{DPD}		0.8	2	μA	Disable all IP and LIRC
Input Pull up Resistance GPA/GPB	R_{PU}	105	150	195	KΩ	V_{IN}=0V
		0.7	1	1.3	MΩ	V_{IN}=0V
Input Leakage Current GPA/GPB	I_{LK}	-1		+1	μA	$0<V_{IN}<V_{DD}$
Input Low Voltage GPA/GPB	V_{IL1}	-0.3		$0.2V_{DD}$	V	
Input High Voltage GPA/GPB	V_{IH1}	$0.7V_{DD}$		V_{DD}+0.2	V	V_{DD}=5.5V
Negative Going Threshold (Schmitt input)	V_{ILS}		$0.4V_{DD}$		V	Schmitt trigger selected
Positive Going Threshold (Schmitt input)	V_{IHS}		$0.6V_{DD}$		V	Schmitt trigger selected
Hysteresis Voltage	V_{HY}		$0.2V_{DD}$		V	Schmitt trigger selected
High level output voltage	V_{OH}	2.8			V	I_{OH}=4mA, VDD≥3.3V
Low level output voltage	V_{OL}			0.4	V	I_{OL}=3mA
Sink Current	I_{Osink}	5.6			mA	V_{OL}=0.2V, $4.5≤V_{DD}≤5.5V$
	I_{Osink}	4.3			mA	V_{OL}=0.2V, $3.3≤V_{DD}<4.5V$
	I_{Osink}	2.1			mA	V_{OL}=0.2V, $1.8≤V_{DD}<3.3V$
Source Current	$I_{Osource}$	2.6			mA	$V_{OH}=V_{DD}$-0.2V, $4.5≤V_{DD}≤5.5V$
	$I_{Osource}$	2.0			mA	$V_{OH}=V_{DD}$-0.2V, $3.3≤V_{DD}<4.5V$
	$I_{Osource}$	1.0			mA	$V_{OH}=V_{DD}$-0.2V, $1.8≤V_{DD}<3.3V$

Notes:

- RESETB pin is a Schmitt trigger input.

- VDD, AVDD and VDDPST must be supplied same voltage level.

6.3 AC Electrical Characteristics

(VDD-VSS=4.5V, TA = 25°C, No load unless otherwise specified.)

6.3.1 External 32 KHz XTAL Oscillator

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input clock frequency		-	32.768	-	KHz	External crystal
Start up time	$t_{startup}$		300		ms	

6.3.2 Internal RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Oscillation Frequency	T=25℃		39.936		MHz
Startup time			90		ns
Stability Calibrated Internal Oscillator Frequency	+25°C; V_{DD}=5V	-1		+1	%
	-0°C~+70°C; V_{DD}=5V	-3	-	+3	%
Standby current	V_{DD}=3.3V			30	nA

6.3.3 Internal 10 KHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Oscillation Frequency	T=25℃		10		kHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD}=3V	-5		+5	%
	0°C~+70°C; V_{DD}=5V	-20		+20	%
Supply Current			1		µA
Standby Current	V_{DD}=5V			100	nA

6.4 Analog Characteristics

6.4.1 10-bit SAR ADC

Parameter	Symbol	Min	Typ	Max	Unit
Resolution	-	-	10		bit
Offset Error	EO	-4	±0.5	+3.5	LSB
Gain Error (Transfer gain)	EG		±1	-2.5	%
ADC Clock Frequency	FADC	-	-	6	MHz
Sample & Conversion Time	TADC	-	12	-	Clock
Sample Rate	FS	-	-	500	Ksps
Supply Voltage	AVDD	2		5.5	V
Supply Current (Avg.)	IDD	-	-	1.5	mA
Input Voltage Range	VIN	0	-	AVDD	V
Integral Non-Linearity Error	INL	-2	±1	+2	LSB
Differential Non-Linearity	DNL	-1	±0.5	+1	LSB

6.4.2 LDO15

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input voltage		1.8	-	5.5	V
LDO output voltage		1.425	1.5	1.575	V
Load current		0		20	mA
Output Voltage tolerance			±5		%

6.4.3 PGC

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	AVDD		2.4	3.3	5.5	V
Operation Current	IDD			1.5		mA
Programmable gain			-18		45	dB
Programmable gain step size		Guaranteed Monotonic		1		dB

6.4.4 BOD/LVR

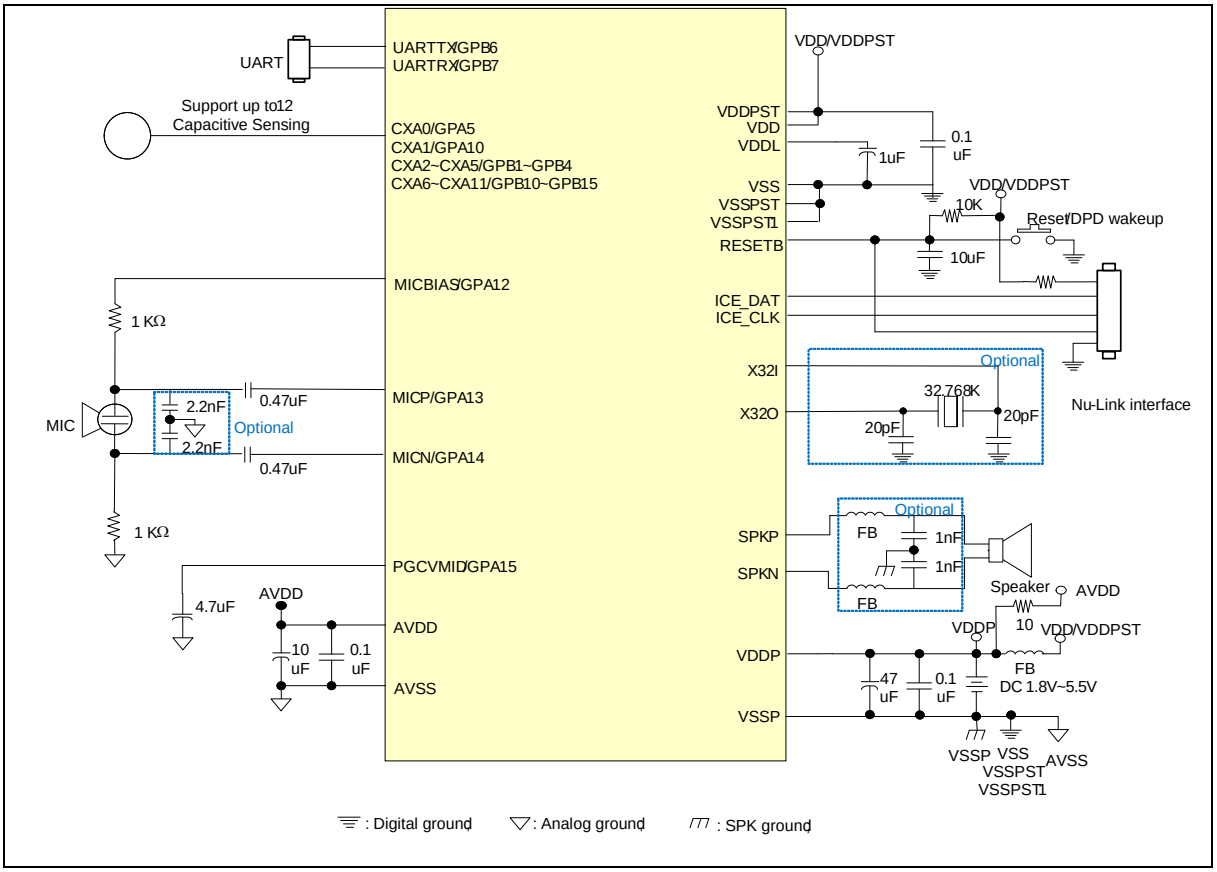
PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Current	IDD		19		μA

Brown-out voltage	BOD_SEL[3:0] =1111	4.37	4.6	4.83	V
	BOD_SEL[3:0] =1110	3.99	4.2	4.41	V
	BOD_SEL[3:0] =1101	3.71	3.9	4.1	V
	BOD_SEL[3:0] =1100	3.52	3.7	3.89	V
	BOD_SEL[3:0] =1011	3.42	3.6	3.78	V
	BOD_SEL[3:0] =1010	3.23	3.4	3.57	V
	BOD_SEL[3:0] =1001	2.95	3.1	3.26	V
	BOD_SEL[3:0] =1000	2.85	3.0	3.15	V
	BOD_SEL[3:0] =0111	2.66	2.8	2.94	V
	BOD_SEL[3:0] =0110	2.47	2.6	2.73	V
	BOD_SEL[3:0] =0101	2.28	2.4	2.52	V
	BOD_SEL[3:0] =0100	2.09	2.2	2.31	V
	BOD_SEL[3:0] =0011	2.00	2.1	2.21	V
	BOD_SEL[3:0] =0010	1.90	2.0	2.10	V
	BOD_SEL[3:0] =0001	1.81	1.9	2.00	V
	BOD_SEL[3:0] =0000	1.71	1.8	1.89	V
LVR	V_{LVR}		1.6		V
BOD Hysteresis	V_{hys}	42	60	125	mV

6.4.5 DPWM

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Power				500	mW
Load Impedance			8		Ω
Switching Frequency	Derived from HIRC clock	102		1536	KHz
Bandwidth			12		KHz
THD+N	No Load		0.1		%

7 Typical Application Circuit



8 Ordering Information

Part No. (Blank)	Type	GPIO
NSC74256Z NSC74512Z NSC741K0Z NSC741K5Z	QFN32 (5x5mm^2)	19 I/O
NSC74256L NSC74512L NSC741K0L NSC741K5L	LQFP48 (7x7mm^2)	30 I/O

9 Revision History

Revision	Date	Substantial Changes	Page
1.0	May. 2023	First Revision Release	