Self-Protected Low Side Driver with Temperature and Current Limit
42 V, 14 A, Single N-Channel

NCV8403A, NCV8403B

NCV8403A/B is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
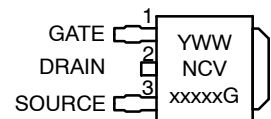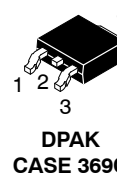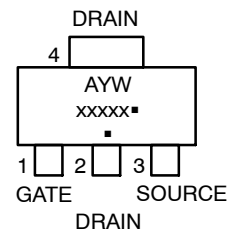- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D MAX (Limited)
42 V	53 mΩ @ 10 V	15 A

MARKING DIAGRAM

SOT−223
CASE 318E
STYLE 3

DPAK
CASE 369C
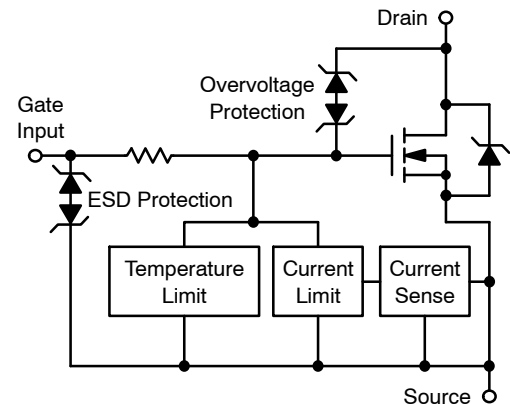
A = Assembly Location
Y = Year
W, WW = Work Week
xxxxx = 8403A or 8403B
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

Publication Order Number:
NCV8403/D

MAXIMUM RATINGS ($T_J = 25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	42	Vdc
Gate−to−Source Voltage	V_{GS}	± 14	Vdc
Drain Current Continuous	I_D	Internally Limited	

Total Power Dissipation − SOT−223 Version
     @ $T_A = 25°C$ (Note 1)
     @ $T_A = 25°C$ (Note 2)
Total Power Dissipation − DPAK Version
     @ $T_A = 25°C$ (Note 1)
     @ $T_A = 25°C$ (Note 2)
	P_D	
		1.13
		1.56
		
		1.32
		2.5
			W

Thermal Resistance − SOT−223 Version
     Junction−to−Soldering Point
     Junction−to−Ambient (Note 1)
     Junction−to−Ambient (Note 2)
Thermal Resistance − DPAK Version
     Junction−to−Soldering Point
     Junction−to−Ambient (Note 1)
     Junction−to−Ambient (Note 2)
	
	$R_{\theta JS}$
	$R_{\theta JA}$
	$R_{\theta JA}$
	
	$R_{\theta JS}$
	$R_{\theta JA}$
	$R_{\theta JA}$
		
		12
		110
		80
		
		2.5
		95
		50
			°C/W

Single Pulse Inductive Load Switching Energy ($V_{DD} = 25$ Vdc, $V_{GS} = 5.0$ V, $I_L = 2.8$ A, $L = 120$ mH, $R_G = 25\ \Omega$)	E_{AS}	470	mJ
Load Dump Voltage ($V_{GS} = 0$ and 10 V, $R_I = 2.0\ \Omega$, $R_L = 4.5\ \Omega$, $t_d = 400$ ms)	V_{LD}	55	V
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{stg}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Surface mounted onto minimum pad size (0.412″ square) FR4 PCB, 1 oz cu.
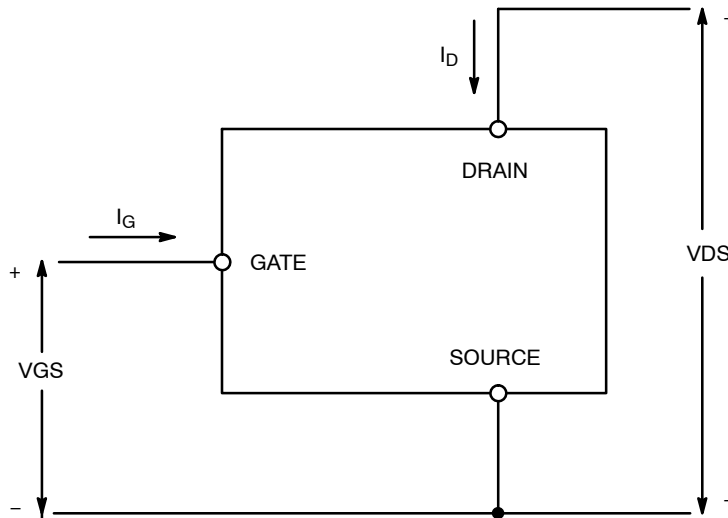2. Mounted onto 1″ square pad size (1.127″ square) FR4 PCB, 1 oz cu.

Figure 1. Voltage and Current Convention

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Clamped Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) (V_{GS} = 0 Vdc, I_D = 250 μAdc, T_J = −40°C to 150°C) (Note 3)	$V_{(BR)DSS}$	42 40	46 45	51 51	Vdc Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc, T_J = 150°C) (Note 3)	I_{DSS}	– –	0.6 2.5	5.0 –	μAdc
Gate Input Current (V_{GS} = 5.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	–	50	125	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.2 mAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 –	1.7 5.0	2.2 –	Vdc mV/°C
Static Drain–to–Source On–Resistance (Note 4) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J @ 25°C) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J @ 150°C) (Note 3)	$R_{DS(on)}$	– –	53 95	68 123	mΩ
Static Drain–to–Source On–Resistance (Note 4) (V_{GS} = 5.0 Vdc, I_D = 3.0 Adc, T_J @ 25°C) (V_{GS} = 5.0 Vdc, I_D = 3.0 Adc, T_J @ 150°C) (Note 3)	$R_{DS(on)}$	– –	63 105	76 135	mΩ
Source–Drain Forward On Voltage (I_S = 7.0 A, V_{GS} = 0 V)	V_{SD}	–	0.95	1.1	V

SWITCHING CHARACTERISTICS (Note 3)

Characteristic		Symbol	Min	Typ	Max	Unit
Turn–ON Time (10% V_{IN} to 90% I_D)	V_{IN} = 0 V to 5 V, V_{DD} = 25 V I_D = 1.0 A, Ext R_G = 2.5 Ω	t_{ON}		44		μs
Turn–OFF Time (90% V_{IN} to 10% I_D)		t_{OFF}		84		
Turn–ON Time (10% V_{IN} to 90% I_D)	V_{IN} = 0 V to 10 V, V_{DD} = 25 V, I_D = 1.0 A, Ext R_G = 2.5 Ω	t_{ON}		15		
Turn–OFF Time (90% V_{IN} to 10% I_D)		t_{OFF}		116		
Slew–Rate ON (20% V_{DS} to 50% V_{DS})	V_{in} = 0 to 10 V, V_{DD} = 12 V, R_L = 4.7 Ω	$-dV_{DS}/dt_{ON}$		2.43		V/μs
Slew–Rate OFF (80% V_{DS} to 50% V_{DS})		dV_{DS}/dt_{OFF}		0.83		

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

Characteristic		Symbol	Min	Typ	Max	Unit
Current Limit	V_{GS} = 5.0 V, V_{DS} = 10 V V_{GS} = 5.0 V, T_J = 150°C (Note 3)	I_{LIM}	10 5.0	15 10	20 15	Adc
Current Limit	V_{GS} = 10 V, V_{DS} = 10 V V_{GS} = 10 V, T_J = 150°C (Note 3)	I_{LIM}	12 8.0	17 13	22 18	Adc
Temperature Limit (Turn–off)	V_{GS} = 5.0 Vdc (Note 3)	$T_{LIM(off)}$	150	175	200	°C
Thermal Hysteresis	V_{GS} = 5.0 Vdc	$\Delta T_{LIM(on)}$	–	15	–	°C
Temperature Limit (Turn–off)	V_{GS} = 10 Vdc (Note 3)	$T_{LIM(off)}$	150	165	185	°C
Thermal Hysteresis	V_{GS} = 10 Vdc	$\Delta T_{LIM(on)}$	–	15	–	°C

GATE INPUT CHARACTERISTICS (Note 3)

Characteristic		Symbol	Min	Typ	Max	Unit
Device ON Gate Input Current	V_{GS} = 5 V I_D = 1.0 A	I_{GON}		50		μA
	V_{GS} = 10 V I_D = 1.0 A			400		
Current Limit Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V	I_{GCL}		0.1		mA
	V_{GS} = 10 V, V_{DS} = 10 V			0.6		
Thermal Limit Fault Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V	I_{GTL}		0.45		mA
	V_{GS} = 10 V, V_{DS} = 10 V			1.5		

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 3)

Characteristic		Symbol	Min	Typ	Max	Unit
Electro–Static Discharge Capability	Human Body Model (HBM)	ESD	4000	–	–	V
Electro–Static Discharge Capability	Machine Model (MM)	ESD	400	–	–	V

3. Not subject to production testing.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
5. Fault conditions are viewed as beyond the normal operating range of the part.
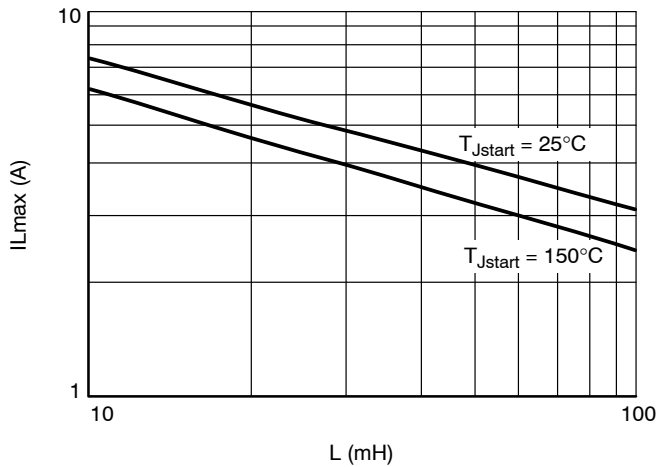
TYPICAL PERFORMANCE CURVES

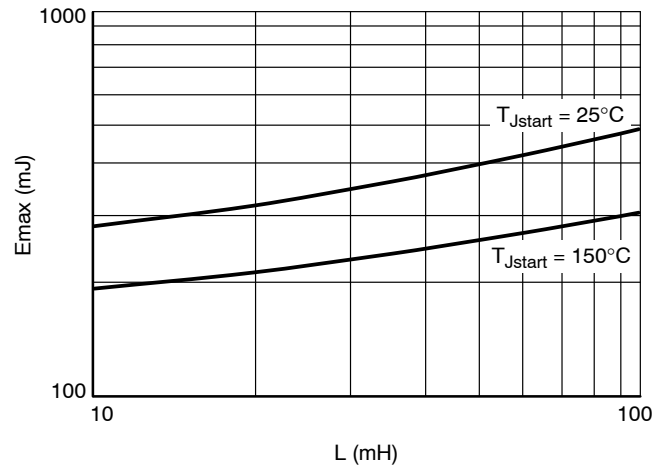**Figure 2. Single Pulse Maximum Switch−off Current vs. Load Inductance**

Figure 3. Single−Pulse Maximum Switching Energy vs. Load Inductance
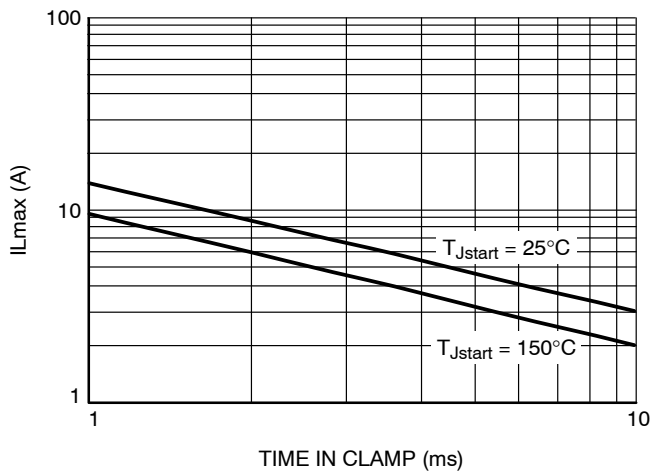

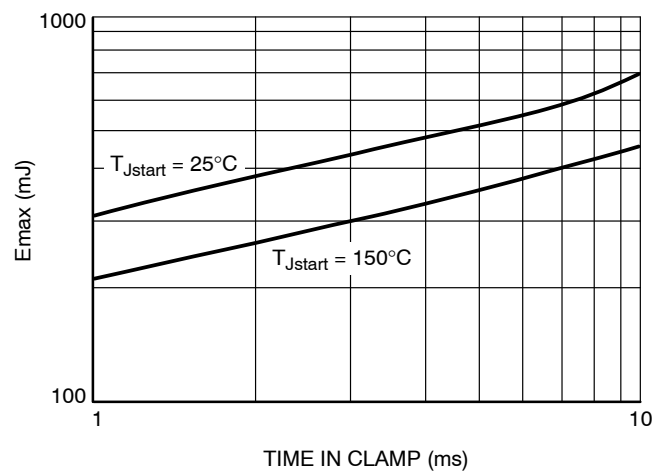**Figure 4. Single Pulse Maximum Inductive Switch−off Current vs. Time in Clamp**

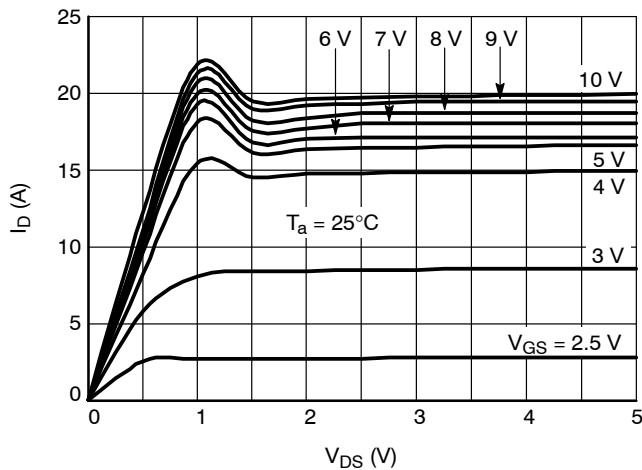**Figure 5. Single−Pulse Maximum Inductive Switching Energy vs. Time in Clamp**

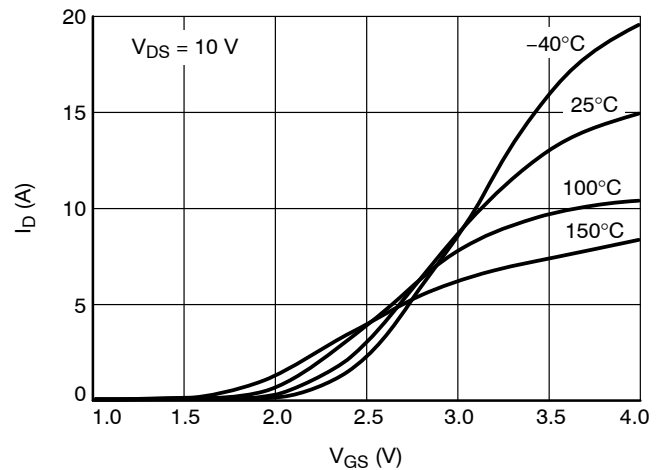**Figure 6. On−state Output Characteristics**
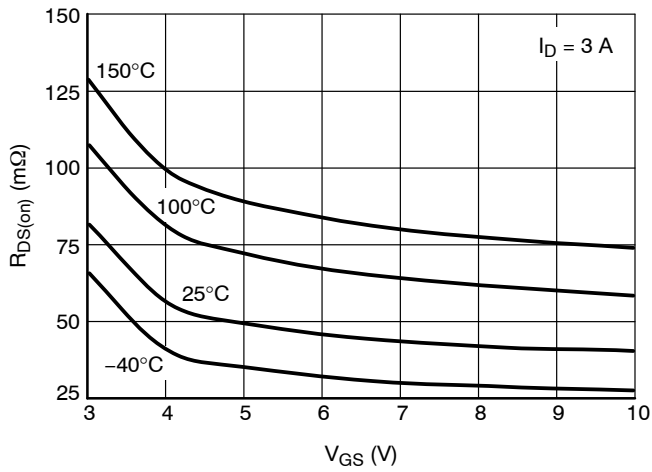

Figure 7. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

Figure 8. R$_{DS(on)}$ vs. Gate−Source Voltage
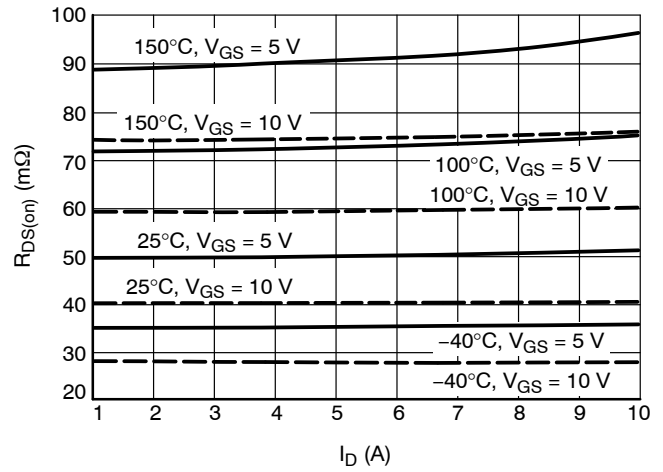
Figure 9. R$_{DS(on)}$ vs. Drain Current
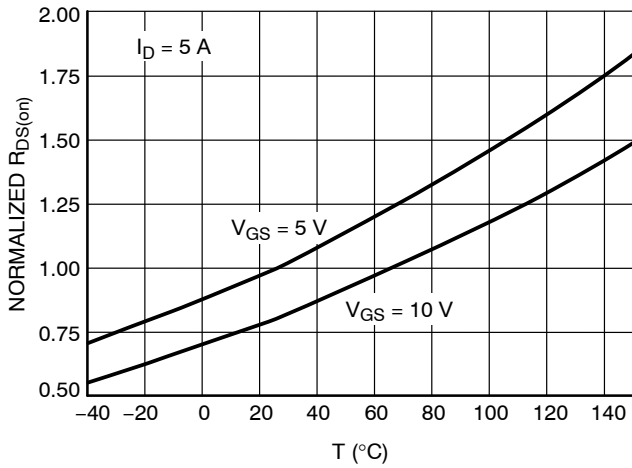
Figure 10. Normalized R$_{DS(on)}$ vs. Temperature
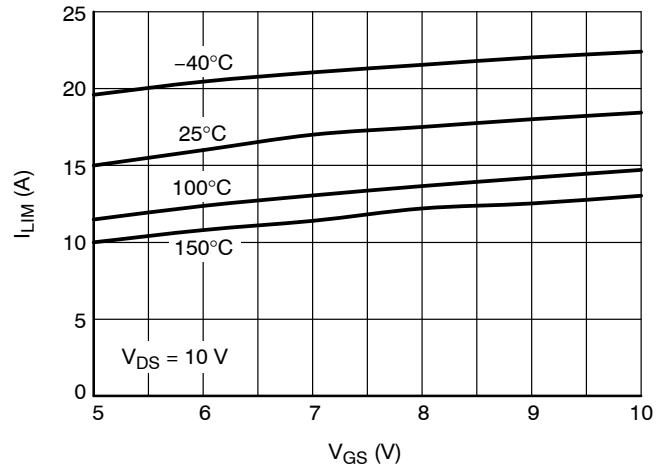
Figure 11. Current Limit vs. Gate−Source
Voltage
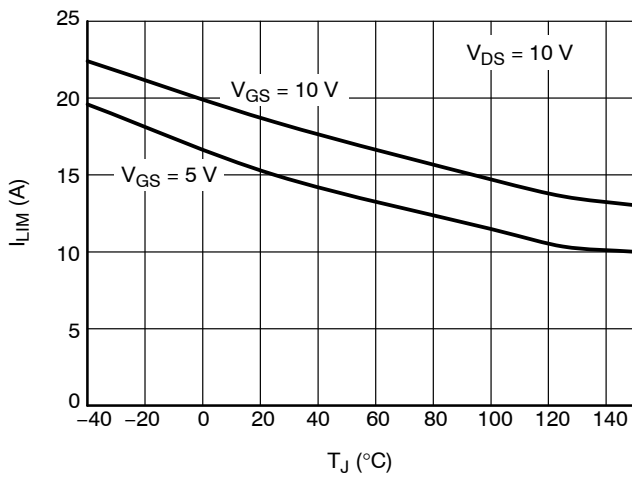
Figure 12. Current Limit vs. Junction
Temperature
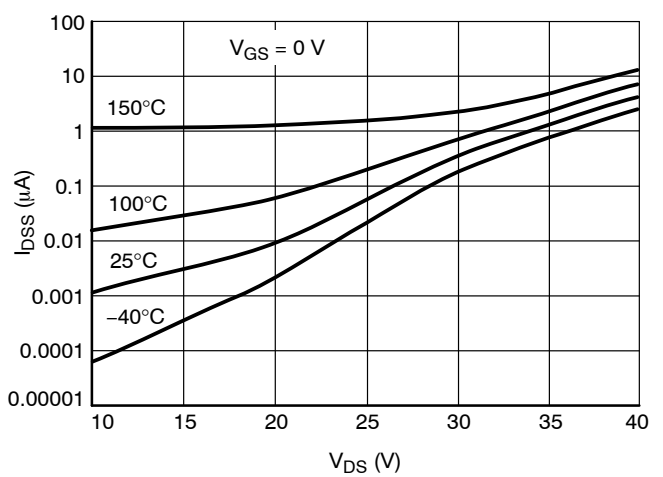
Figure 13. Drain−to−Source Leakage Current

TYPICAL PERFORMANCE CURVES
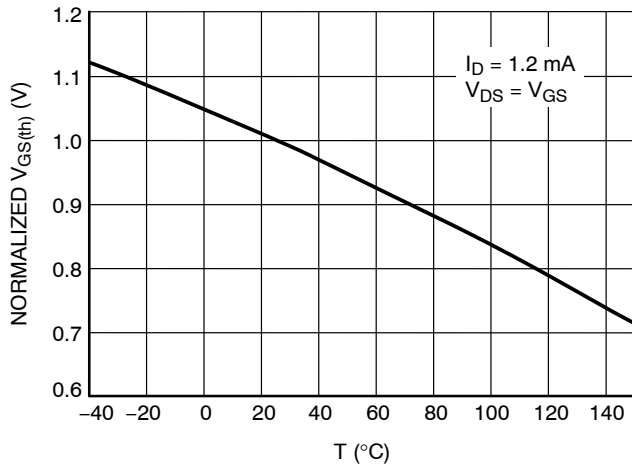
Figure 14. Normalized Threshold Voltage vs. Temperature
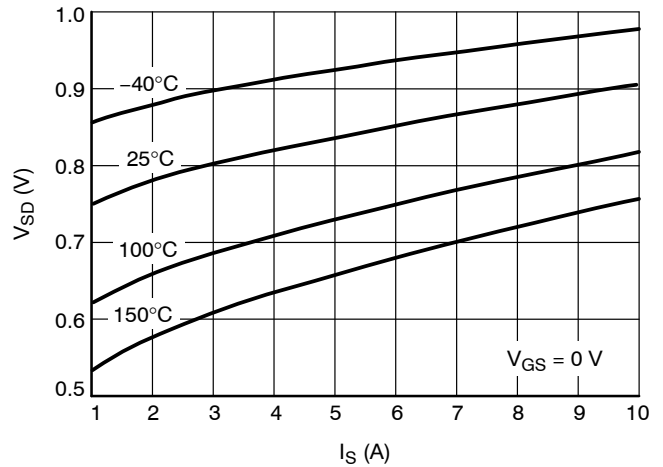
Figure 15. Source−Drain Diode Forward Characteristics
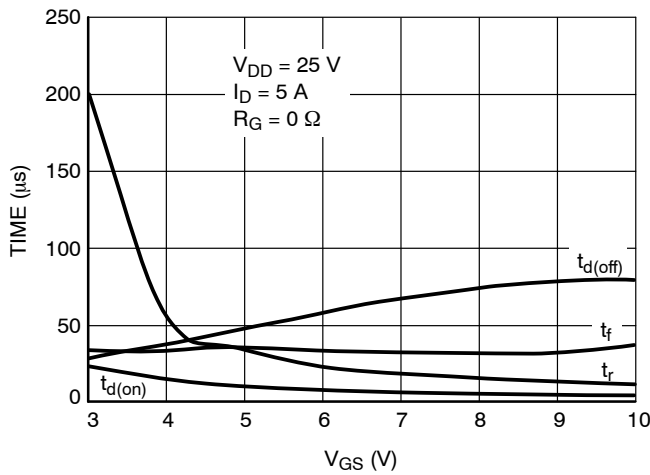
Figure 16. Resistive Load Switching Time vs. Gate−Source Voltage
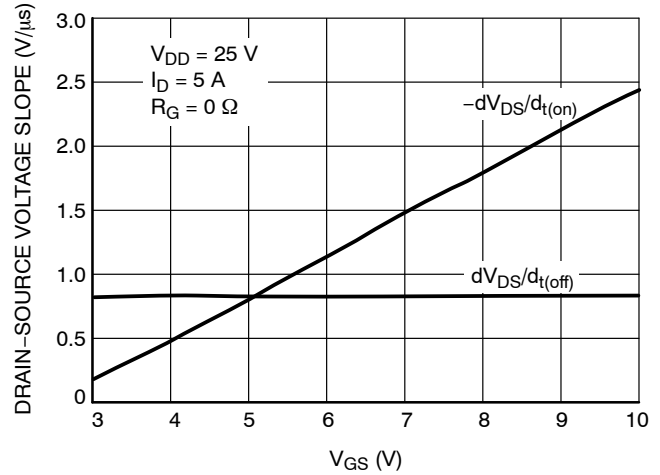
Figure 17. Resistive Load Switching Drain−Source Voltage Slope vs. Gate−Source Voltage
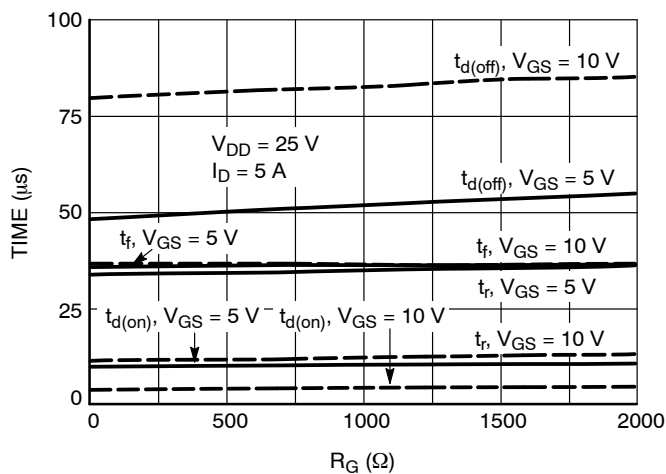
Figure 18. Resistive Load Switching Time vs. Gate Resistance
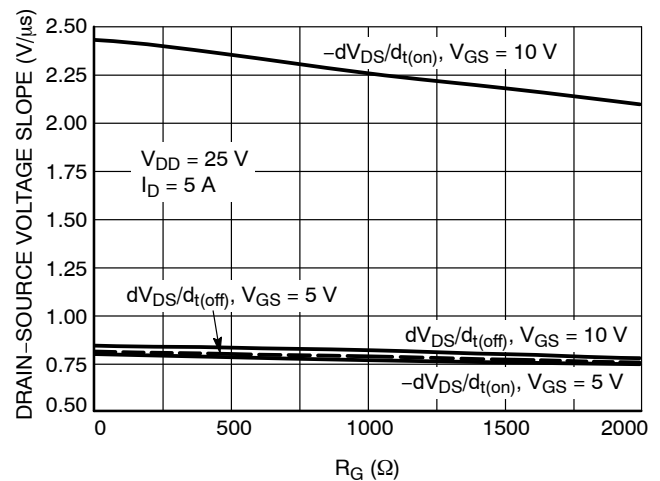
Figure 19. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

TYPICAL PERFORMANCE CURVES
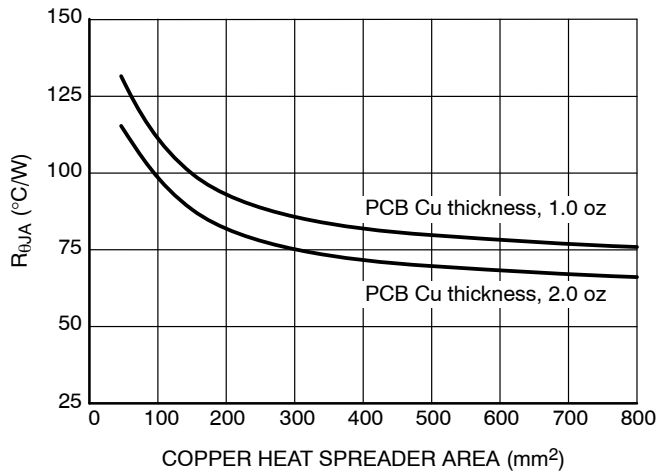
Figure 20. R$_{\theta JA}$ vs. Copper Area – SOT–223
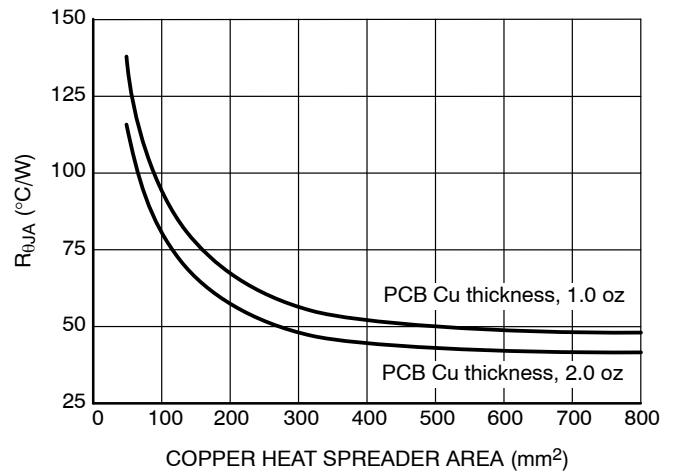
Figure 21. R$_{\theta JA}$ vs. Copper Area – DPAK
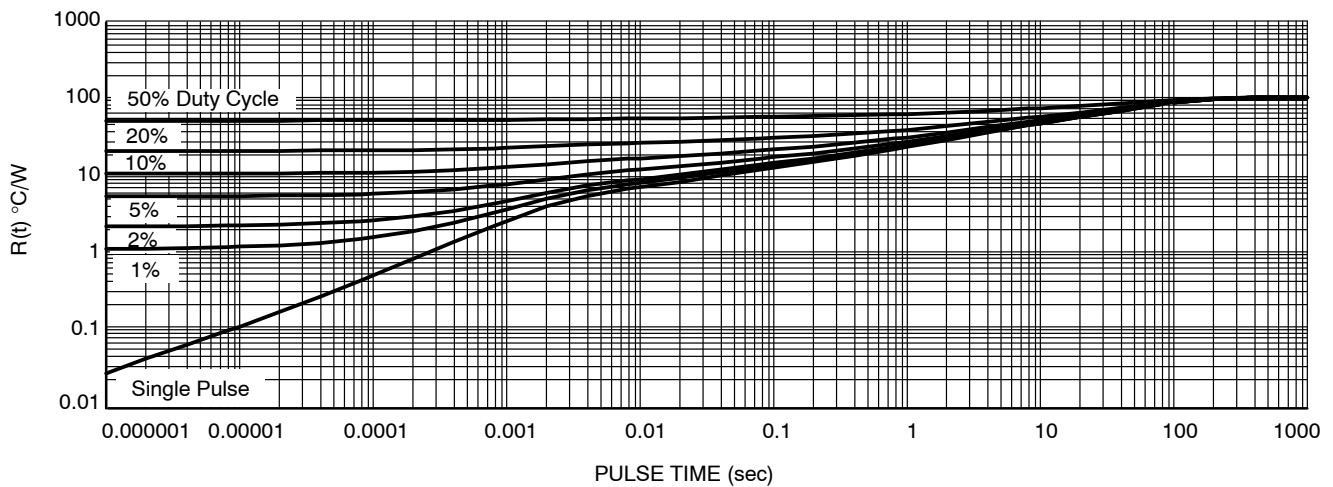
Figure 22. Transient Thermal Resistance – SOT–223 Version
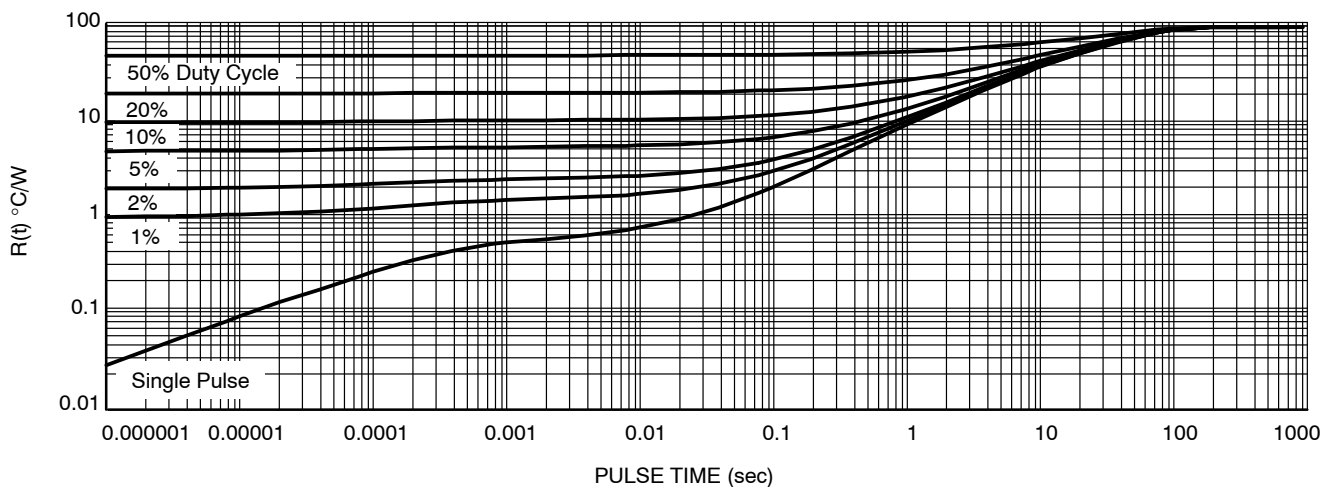
Figure 23. Transient Thermal Resistance – DPAK Version

TEST CIRCUITS AND WAVEFORMS
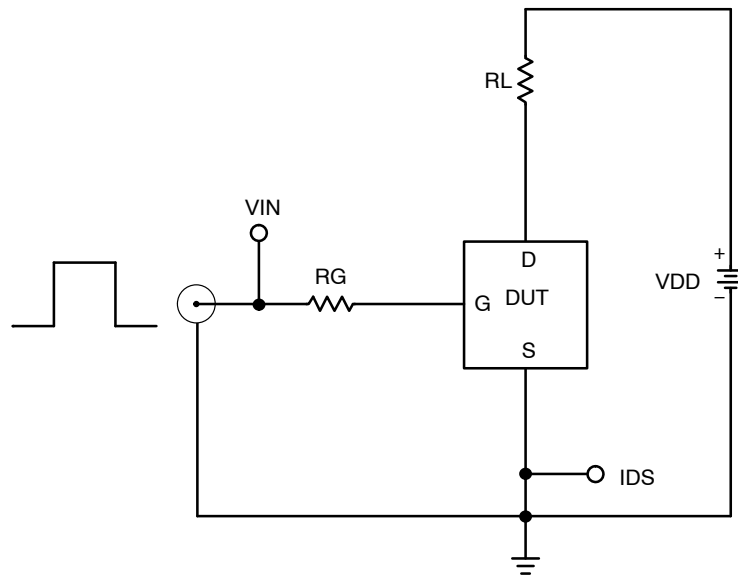
Figure 24. Resistive Load Switching Test Circuit
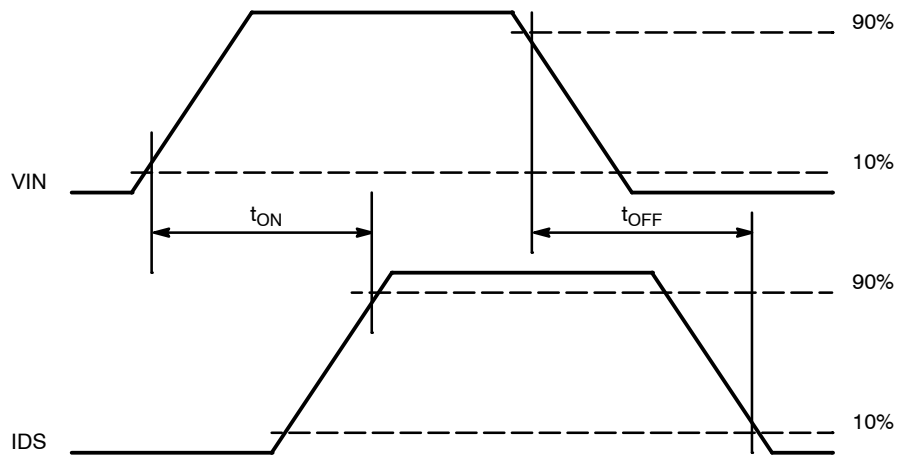
Figure 25. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS
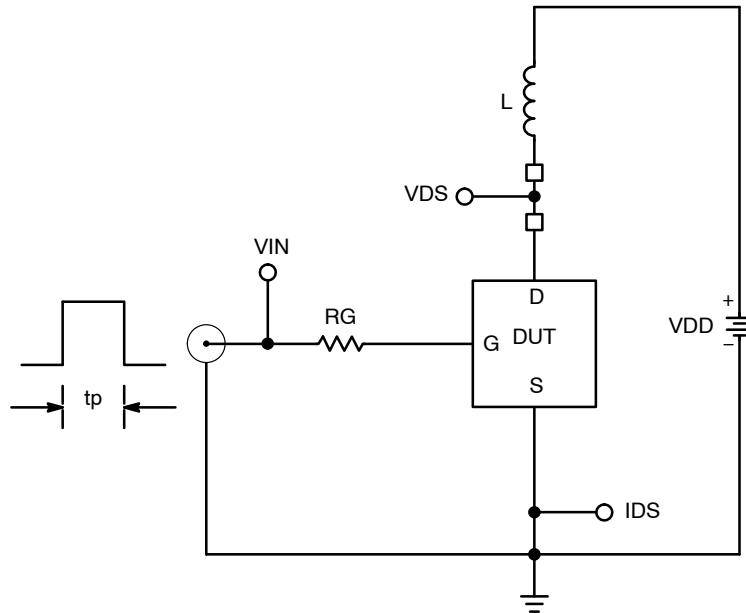
Figure 26. Inductive Load Switching Test Circuit
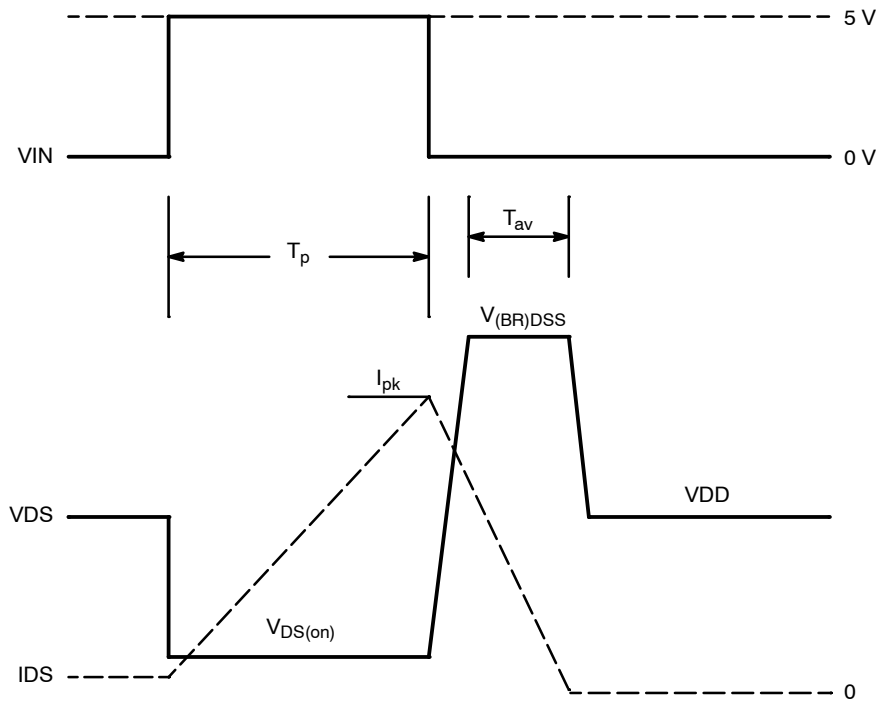
Figure 27. Inductive Load Switching Waveforms

ORDERING INFORMATION

Device	Package	Shipping[†]
NCV8403ASTT1G	SOT−223 (Pb−Free)	1000 / Tape & Reel
NCV8403ASTT3G	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV8403ADTRKG	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8403BDTRKG	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

SCALE 1:1

DATE 02 OCT 2018
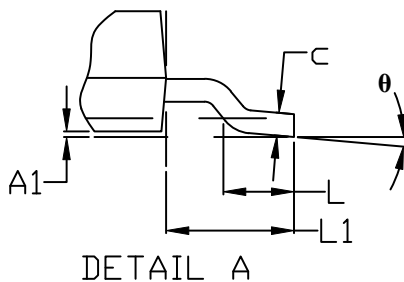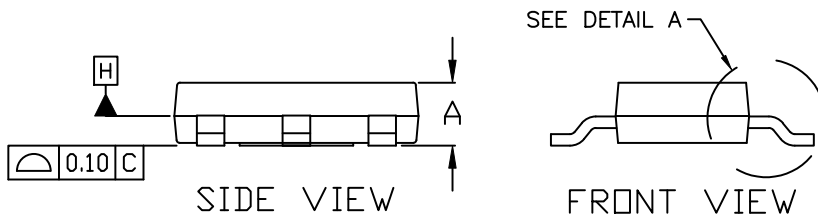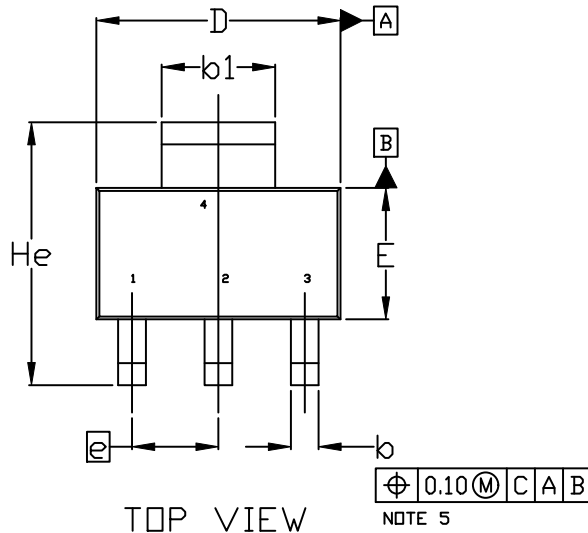
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

TOP VIEW

NOTE 5

SIDE VIEW

SEE DETAIL A

FRONT VIEW

DETAIL A

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°

3.80
2.00
6.30
3× 2.00
2.30 PITCH
3× 1.50

RECOMMENDED MOUNTING FOOTPRINT

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOT−223 (TO−261)		PAGE 1 OF 2

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

**GENERIC
MARKING DIAGRAM***

AYW
XXXXX■
■
1
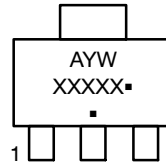
A   = Assembly Location
Y   = Year
W   = Work Week
XXXXX = Specific Device Code
■   = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOT−223 (TO−261)		PAGE 2 OF 2

onsemi

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

DATE 21 JUL 2015

SCALE 1:1

TOP VIEW

⊕ | 0.005 (0.13) Ⓜ | C

SIDE VIEW

DETAIL A

BOTTOM VIEW

DETAIL A
ROTATED 90° CW

GAUGE PLANE

SEATING PLANE
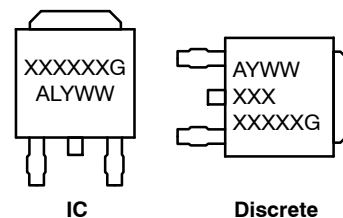
BOTTOM VIEW
ALTERNATE CONSTRUCTIONS
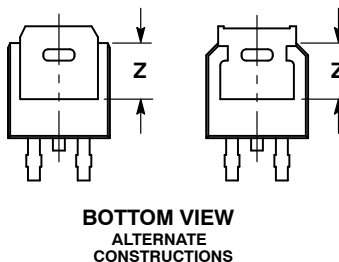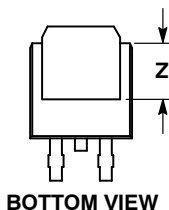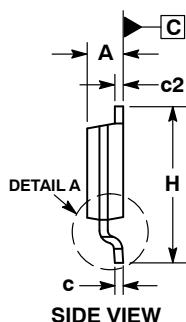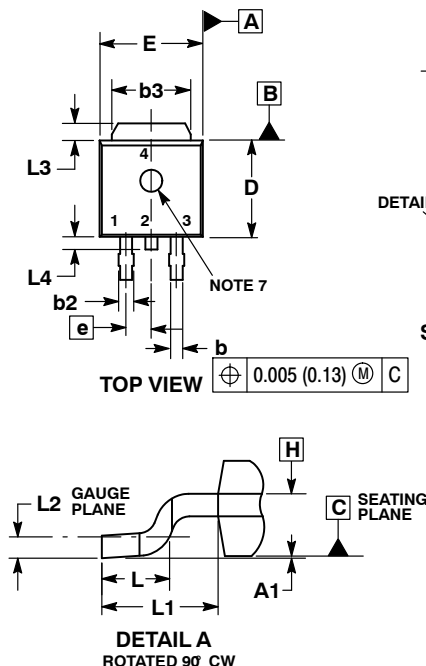
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

SOLDERING FOOTPRINT*

6.20 / 0.244

3.00 / 0.118

2.58 / 0.102

5.80 / 0.228

1.60 / 0.063

6.17 / 0.243
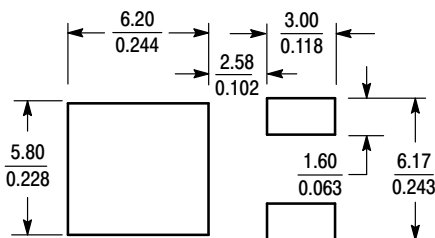
SCALE 3:1   (mm / inches)

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXXG
ALYWW

IC

AYWW
XXX
XXXXXG

Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON10527D	
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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