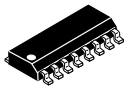
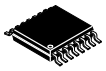
Dual Precision Monostable Multivibrator (Retriggerable, Resettable)

MC74HC4538A



SOIC−16
D SUFFIX
CASE 751B



TSSOP−16
DT SUFFIX
CASE 948F

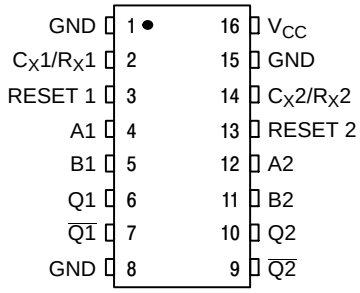
The MC74HC4538A is identical in pinout to the MC14538B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and produces a precision output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger−input rise and fall time restrictions. The output pulse width is determined by the external timing components, R_x and C_x. The device has a reset function which forces the Q output low and the $\overline{Q}$ output high, regardless of the state of the output pulse circuitry.

Features

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse is Independent of the Trigger Pulse Width
- ± 10% Guaranteed Pulse Width Variation from Part to Part (Using the Same Test Jig)
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 145 FETs or 36 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

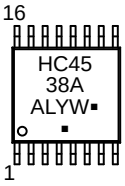
PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC−16



TSSOP−16

A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

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FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\overline{Q}$
H	↑	H	⊓	⊔
H	L	↓	⊓	⊔
H	X	L	Not Triggered	
H	H	X	Not Triggered	
H	L,H,↓	H	Not Triggered	
H	L	L,H,↑	Not Triggered	
L	X	X	L	H
↓ ↑	X	X	Not Triggered	

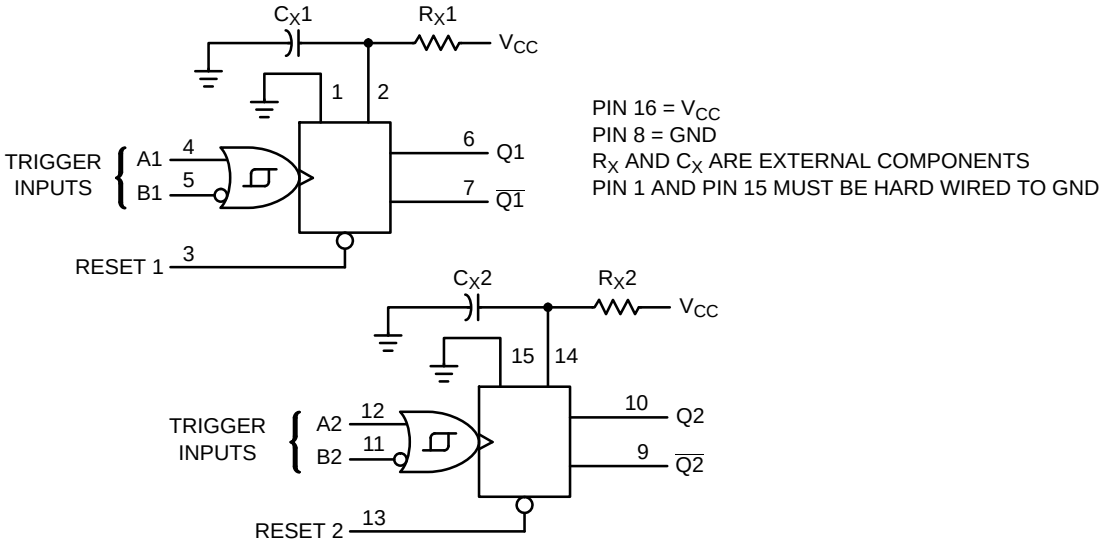


Figure 1. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC4538ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel

DISCONTINUED (Note 1)

MC74HC4538ADG	SOIC−16 (Pb−Free)	48 Units / Rail
NLV74HC4538ADR2G*	SOIC−16 (Pb−Free)	2500 / Tape & Reel
MC74HC4538ADTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
NLVHC4538ADTR2G*	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

1. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		$-0.5 \le V_I \le V_{CC} + 0.5$	V
V_O	DC Output Voltage	(Note 2)	$-0.5 \le V_O \le V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	A, B, Reset C_X, R_X	±20 ±30	mA
I_{OK}	DC Output Diode Current		±25	mA
I_O	DC Output Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction temperature under Bias		+150	°C
θ_{JA}	Thermal resistance	SOIC TSSOP	112 148	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL−94−VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 100 > 500	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 6)	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22−A114−A.
4. Tested to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		–55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 6) A or B (Figure 4)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 –	1000 500 400 No Limit	ns
R_X	External Timing Resistor	V_{CC} < 4.5 V $V_{CC} \ge$ 4.5 V	1.0 2.0	† †	kΩ
C_X	External Timing Capacitor		0	†	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

†The maximum allowable values of R_X and C_X are a function of the leakage of capacitor C_X, the leakage of the HC4538A, and leakage due to board layout and surface resistance. For most applications, C_X/R_X should be limited to a maximum value of 10 μF/1.0 MΩ. Values of C_X > 1.0 μF may cause a problem during power down (see Power Down Considerations). Susceptibility to externally induced noise signals may occur for R_X > 1.0 MΩ.

7. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limits									Unit
				–55 to 25°C			≤ 85°C			≤ 125°C			
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2			1.5 3.15 4.2			V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0			0.5 1.35 1.8			0.5 1.35 1.8			0.5 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9			1.9 4.4 5.9			1.9 4.4 5.9			V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le -4.0$ mA $\|I_{out}\| \le -5.2$ mA	 4.5 6.0	 3.98 5.48			 3.84 5.34			 3.7 5.2			
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0			0.1 0.1 0.1			0.1 0.1 0.1			0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	 4.5 6.0			 0.26 0.26			 0.33 0.33			 0.4 0.4	
I_{in}	Maximum Input Leakage Current (A, B, Reset)	V_{in} = V_{CC} or GND	6.0			±0.1			±1.0			±1.0	μA
I_{in}	Maximum Input Leakage Current (R_x, C_x)	V_{in} = V_{CC} or GND	6.0			± 50			±500			±500	nA
I_{CC}	Maximum Quiescent Supply Current (per package) Standby State	V_{in} = V_{CC} or GND Q1 and Q2 = Low I_{out} = 0 μA	6.0			130			220			350	μA
I_{CC}	Maximum Supply Current (per package) Active State	V_{in} = V_{CC} or GND Q1 and Q2 = High I_{out} = 0 μA Pins 2 and 14 = 0.5 V_{CC}	6.0	25°C			−45°C to 85°C			−55°C to 125°C			μA
					400			600				800	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limits						Unit
			–55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{PLH}	Maximum Propagation Delay Input A or B to Q (Figures 5 and 7)	2.0 4.5 6.0		175 35 30		220 44 37		265 53 45	ns
t_{PHL}	Maximum Propagation Delay Input A or B to NQ (Figures 5 and 7)	2.0 4.5 6.0		195 39 33		245 49 42		295 59 50	ns
t_{PHL}	Maximum Propagation Delay Reset to Q (Figures 6 and 7)	2.0 4.5 6.0		175 35 30		220 44 37		265 53 45	ns
t_{PLH}	Maximum Propagation Delay Reset to NQ (Figures 6 and 7)	2.0 4.5 6.0		175 35 30		220 44 37		265 53 45	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 6 and 7)	2.0 4.5 6.0		75 15 13		95 19 16		110 22 19	ns
C_{in}	Maximum Input Capacitance (A. B, Reset) (C_x, R_x)	–		10 25		10 25		10 25	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (per Multivibrator)*	150	pF

*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING CHARACTERISTICS (Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limits						Unit
			–55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{rr}	Minimum Retrigger Time, Input A or B (Figure 6) (Note 8)	2.0 4.5 6.0	– – –		– – –				ns
t_{rec}	Minimum Recovery Time, Inactive to A or B (Figure 6)	2.0 4.5 6.0	0 0 0		0 0 0		0 0 0		ns
t_w	Minimum Pulse Width, Input A or B (Figure 5)	2.0 4.5 6.0	60 12 10		75 15 13		90 18 15		ns
t_w	Minimum Pulse Width, Reset (Figure 6)	2.0 4.5 6.0	60 12 10		75 15 13		90 18 15		ns
t_r, t_f	Maximum Input Rise and Fall Times, Reset (Figure 6)	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns
	A or B (Figure 6)	2.0 4.5 6.0	No Limit						

8.
$$t_{rr}(ns) = \frac{V_{CC}\,(volts) \times C_x\,(pF)}{30.5}$$

OUTPUT PULSE WIDTH CHARACTERISTICS (R_x = 10 kΩ, C_x = 0.1 μF, C_L = 50 pF)

Symbol	Parameter	Conditions		Guaranteed Limits						Unit
				−55 to 25°C		≤ 85°C		≤ 125°C		
		Timing Components	V_{CC} V	Min	Max	Min	Max	Min	Max	
τ	Output Pulse Width (Note 9) (Figures 5 and 6)	R_x = 10 kΩ, C_x = 0.1 μF	5.0	0.63	0.77	0.6	0.8	0.59	0.81	ms
	Pulse Width Match Between Circuits in the same Package			±5.0						%
	Pulse Width Match Variation (Part to Part) (Note 11)			±10						%

OUTPUT PULSE WIDTH CHARACTERISTICS (R_x = 100 kΩ, C_x = 1 nF, C_L = 50 pF)

Symbol	Parameter	Conditions			Guaranteed Limits			Unit
		Timing Components	V_{CC} V	Ambient Temperature	Min	Typ	Max	
τ	Output Pulse Width (Note 10)	R_x = 100 kΩ, C_x = 1 nF	5.0	25°C	−	79	−	μs
	Pulse Width Match Between Circuits in the same Package			−55 to 125°C	−5.0	−	+5.0	%
	Pulse Width Match Variation (Part to Part) (Note 11)			−55 to 125°C	−10	−	+10	%
−	Temperature Variance			−55 to 125°C	−	+0.05	−	μs/°C
−	Power Supply Variance			−55 to 125°C	−	−8.0	−	μs/V

9. $\tau = kR_xC_x$ and k = 0.7 for the output pulse width corresponding to R_x = 10 kΩ, C_x = 0.1 μF.
10. $\tau = kR_xC_x$ and k = 0.79 for the output pulse width corresponding to R_x = 100 kΩ, C_x = 1 nF.
11. Pulse width match variation between ICs (part−to−part) is defined with identical R_x, C_x, V_{CC} and a specific temperature.

TYPICAL CHARACTERISTICS

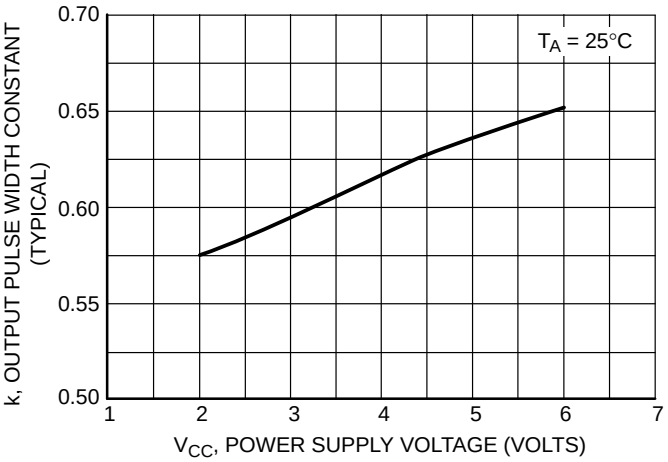


Figure 2. Typical Output Pulse Width Constant, k, versus Supply Voltage (For output pulse widths > 100 μs: $\tau = kR_xC_x$)

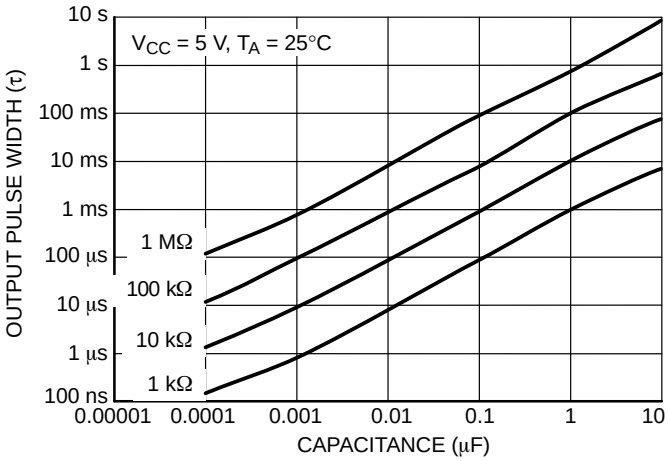


Figure 3. Output Pulse Width versus Timing Capacitance

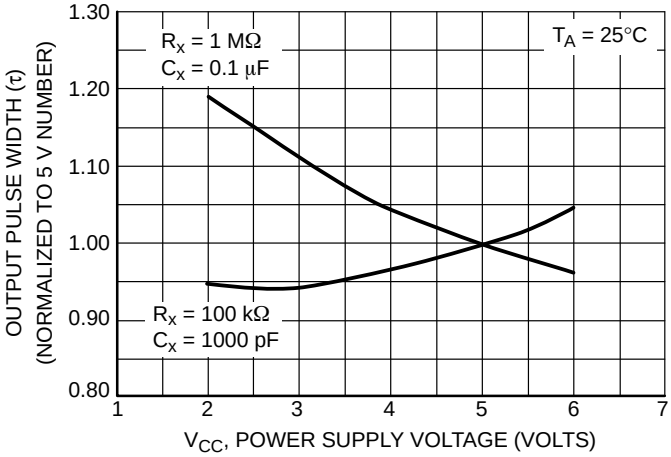


Figure 4. Normalized Output Pulse Width versus Power Supply Voltage

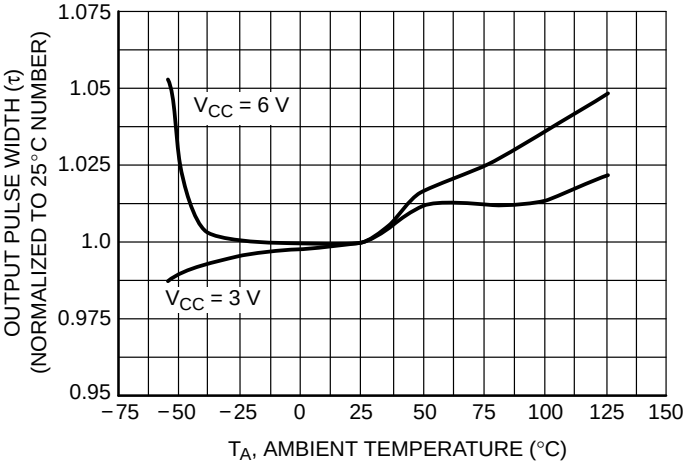


Figure 5. Normalized Output Pulse Width versus Power Supply Voltage

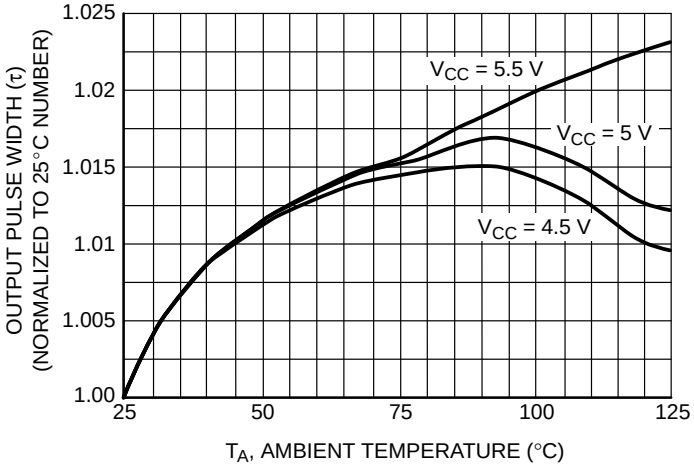


Figure 6. Normalized Output Pulse Width versus Power Supply Voltage

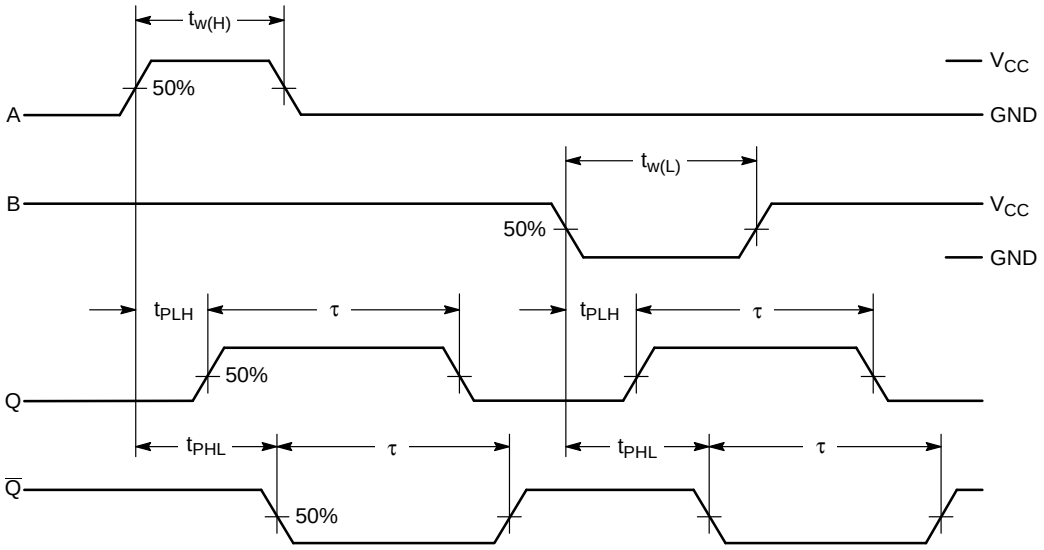


Figure 7. Switching Waveform

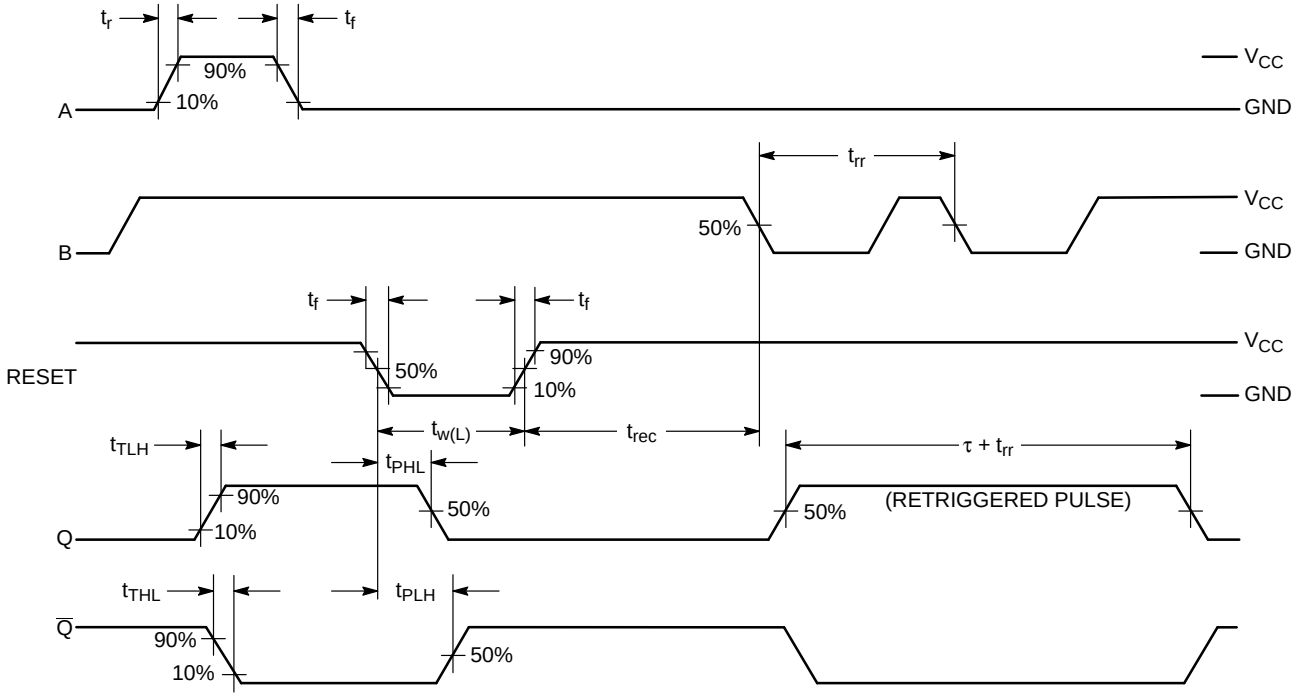
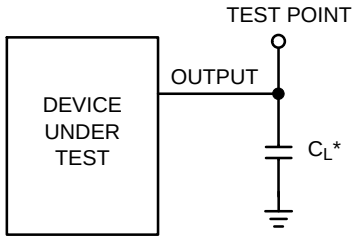


Figure 8. Switching Waveform



*Includes all probe and jig capacitance

Figure 9. Test Circuit

PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 4, 12)

Positive−edge trigger inputs. A rising−edge signal on either of these pins triggers the corresponding multivibrator when there is a high level on the B1 or B2 input.

B1, B2 (Pins 5, 11)

Negative−edge trigger inputs. A falling−edge signal on either of these pins triggers the corresponding multivibrator when there is a low level on the A1 or A2 input.

Reset 1, Reset 2 (Pins 3, 13)

Reset inputs (active low). When a low level is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low level and the $\overline{Q}$ output is set to a high level.

C_X1/R_X1 and C_X2/R_X2 (Pins 2 and 14)

External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram). Polystyrene capacitors are recommended for optimum pulse width control. Electrolytic capacitors are not recommended due to high leakages associated with these type capacitors.

GND (Pins 1 and 15)

External ground. The external timing capacitors discharge to ground through these pins.

OUTPUTS

Q1, Q2 (Pins 6, 10)

Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R_X and C_X.

$\overline{Q1}$, $\overline{Q2}$ (Pins 7, 9)

Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

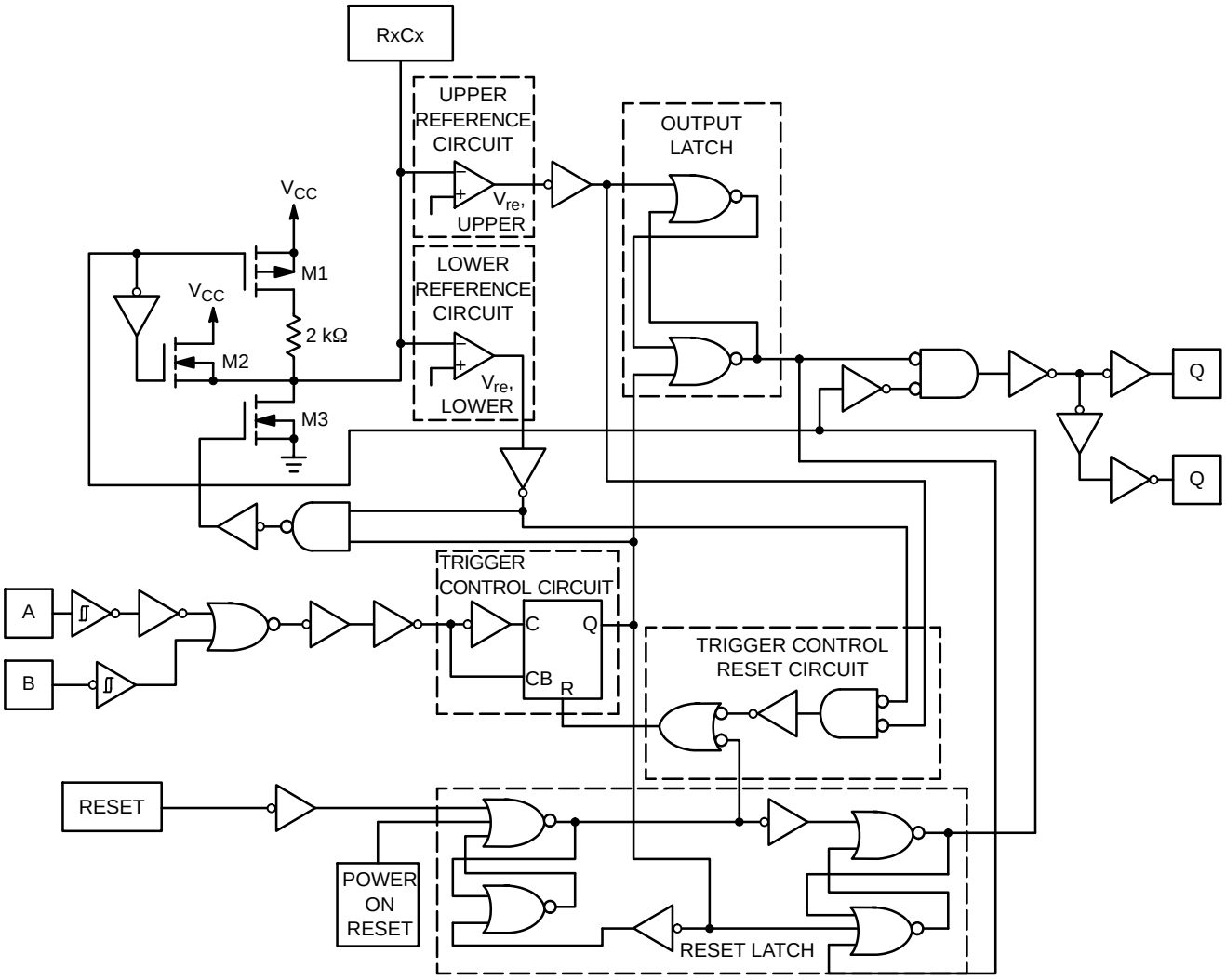


Figure 10. Logic Detail (1/2 the Device)

CIRCUIT OPERATION

Figure 11 shows the HC4538A configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 10): In the quiescent state, the external timing capacitor, C_x, is charged to V_{CC}. When a trigger occurs, the Q output goes high and C_x discharges quickly to the lower reference voltage (V_{ref} Lower $\approx$ 1/3 V_{CC}). C_x then charges, through R_x, back up to the upper reference voltage (V_{ref} Upper $\approx$ 2/3 V_{CC}), at which point the one−shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic detail (Figure 10) and the timing diagram (Figure 11).

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 11). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 11).

The output of the trigger−control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_x, is charged to V_{CC} (#4), and both the upper and lower reference circuit has a low output (#5).

In addition, the output of the trigger−control reset circuit is low.

TRIGGER OPERATION

The HC4538A is triggered by either a rising−edge signal at input A (#7) or a falling−edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger−control circuit to go high (#9).

The trigger−control circuit going high simultaneously initiates two events. First, the output latch goes low, thus taking the Q output of the HC4538A to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_x, to rapidly discharge toward ground (#11). (Note that the voltage across C_x appears at the input of both the upper and lower reference circuit comparator).

When C_x discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger−control reset circuit goes high, resetting the trigger−control circuit flip−flop to a low state (#14). This turns transistor M3 off again, allowing C_x to begin to charge back up toward V_{CC}, with a time constant $t = R_xC_x$ (#15). Once the voltage across C_x charges to above the lower reference voltage, the lower reference circuit will go low allowing the monostable multivibrator to be retriggered.

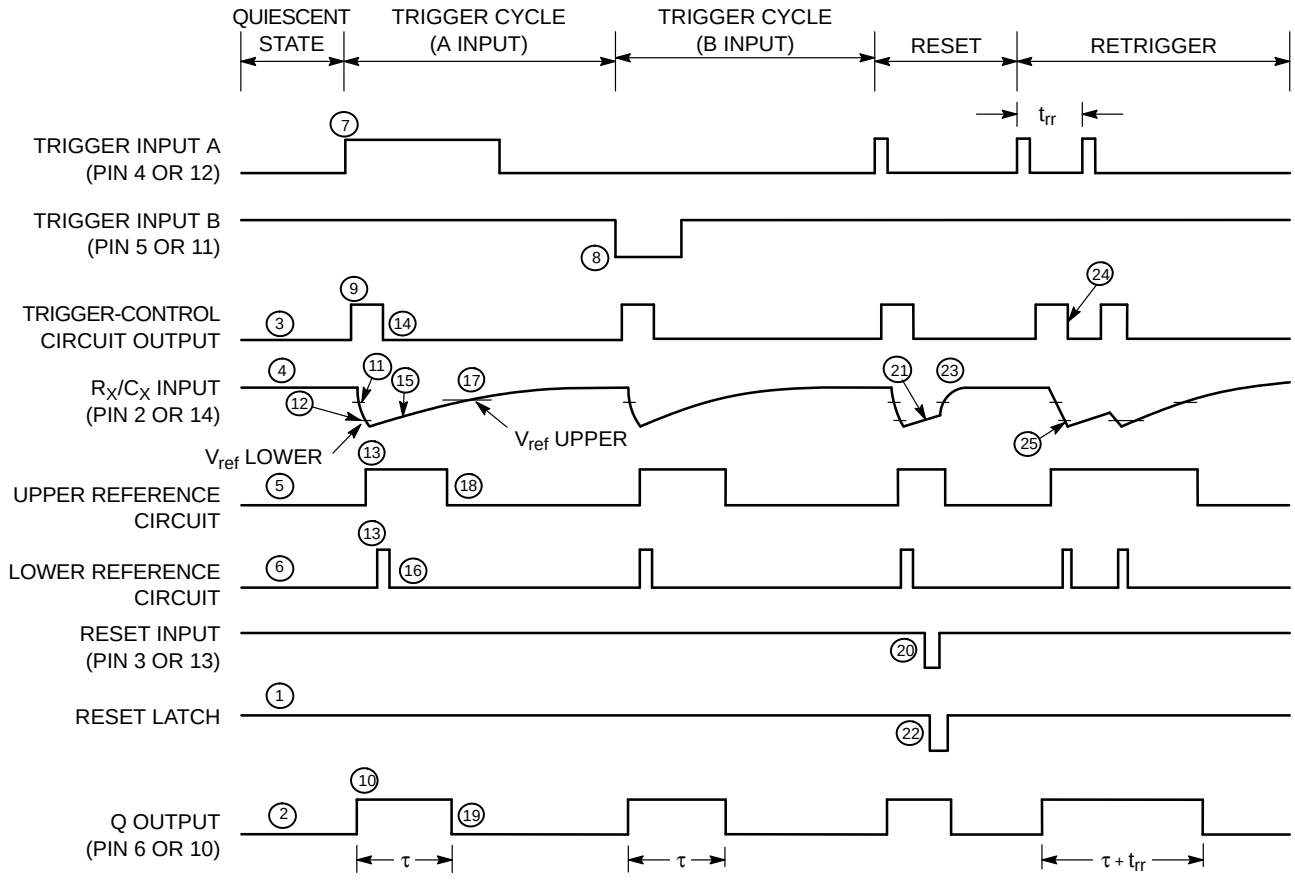


Figure 11. Timing Diagram

When C_x charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the HC4538A to a low state (#19), and completing the time−out cycle.

POWER−DOWN CONSIDERATIONS

Large values of C_x may cause problems when powering down the HC4538A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn−off time of the V_{CC} power supply must not be faster than $t = V_{CC} \bullet C_x/(30\ mA)$. For example, if V_{CC} = 5.0 V and C_x = 15 μF, the V_{CC} supply must turn off no faster than $t = (5.0\ V) \bullet (15\ \mu F)/30\ mA = 2.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{CC} to zero volts occurs, the HC4538A may sustain damage. To avoid this possibility, use an external damping diode, D_x, connected as shown in Figure 12. Best results can be achieved if diode D_X is chosen to be a germanium or Schottky type diode able to withstand large current surges.

RESET AND POWER ON RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the HC4538A to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_x is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_x is allowed to quickly charge up to V_{CC} (#23) to await the next trigger signal.

On power up of the HC4538A the power−on reset circuit will be high causing a reset condition. This will prevent the trigger−control circuit from accepting a trigger input during this state. The HC4538A's Q outputs are low and the $\overline{Q}$ not outputs are high.

RETRIGGER OPERATION

When used in the retriggerable mode (Figure 13), the HC4538A may be retriggered during timing out of the output pulse at any time after the trigger−control circuit flip−flop has been reset (#24), and the voltage across C_x is above the lower reference voltage. As long as the C_x voltage is below the lower reference voltage, the reset of the flip−flop is high, disabling any trigger pulse. This prevents M3 from turning on during this period resulting in an output pulse width that is predictable.

The amount of undershoot voltage on R_xC_x during the trigger mode is a function of loop delay, M3 conductivity, and V_{DD}. Minimum retrigger time, trr (Figure 7), is a function of 1) time to discharge R_xC_x from V_{DD} to lower reference voltage ($T_{discharge}$); 2) loop delay (T_{delay}); 3) time to charge R_xC_x from the undershoot voltage back to the lower reference voltage (T_{charge}).

Figure 14 shows the device configured in the non−retriggerable mode.

For additional information, please see Application Note (AN1558/D) titled *Characterization of Retrigger Time in the HC4538A Dual Precision Monostable Multivibrator.*

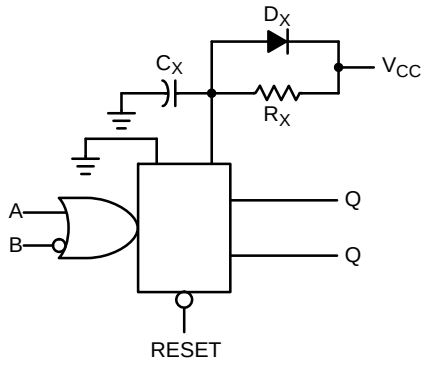


Figure 12. Discharge Protection During Power Down

TYPICAL APPLICATIONS

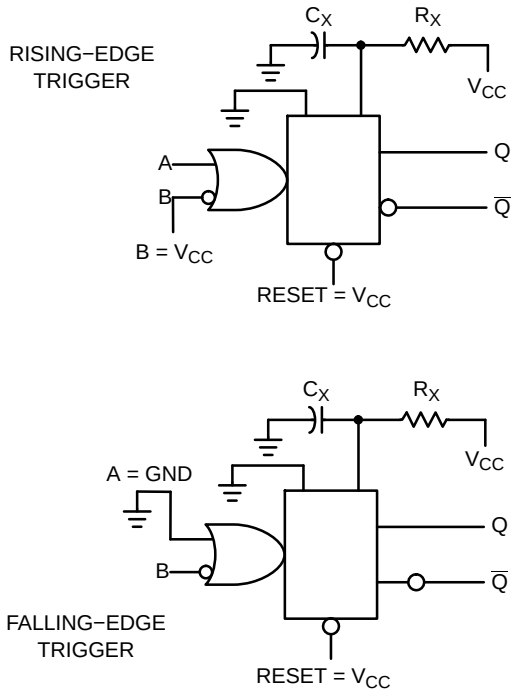


Figure 13. Retriggerable Monostable Circuitry

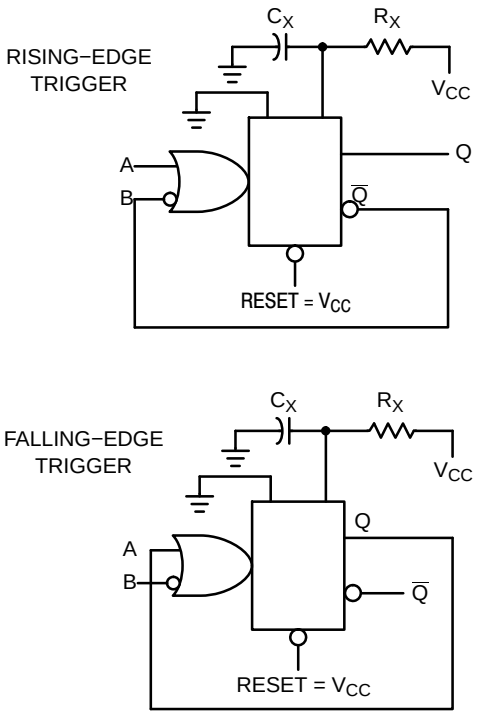


Figure 14. Non−retriggerable Monostable Circuitry

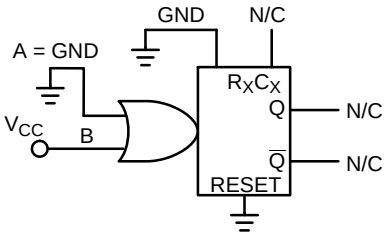
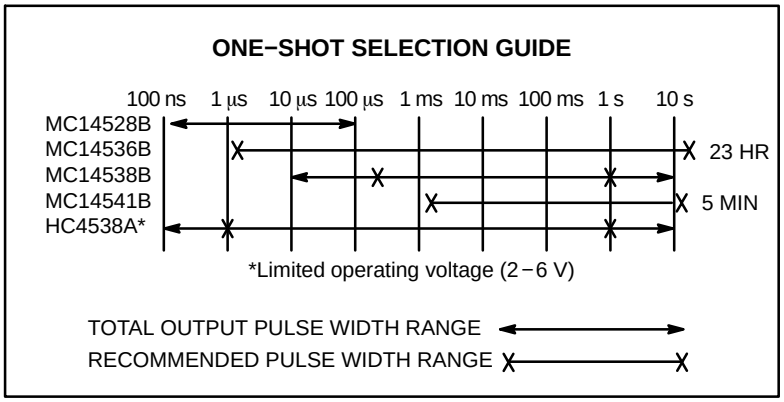
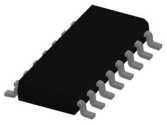


Figure 15. Connection of Unused Section

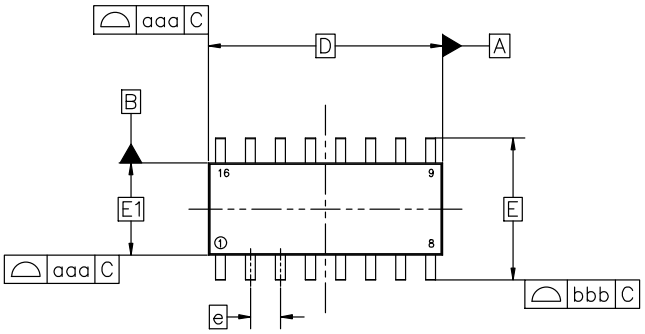




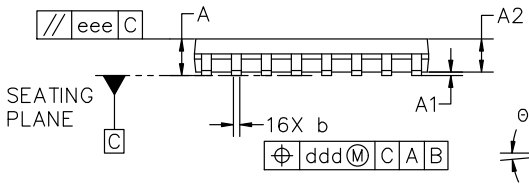
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

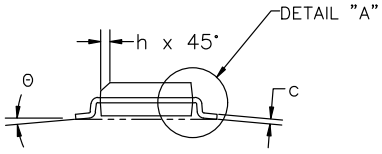
NOTES:
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2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



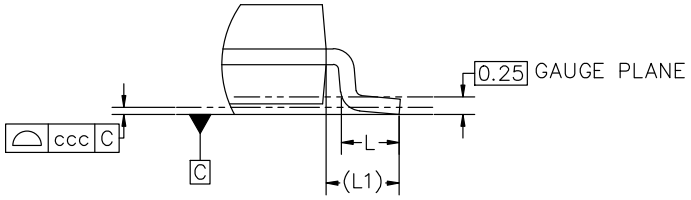
TOP VIEW



SIDE VIEW

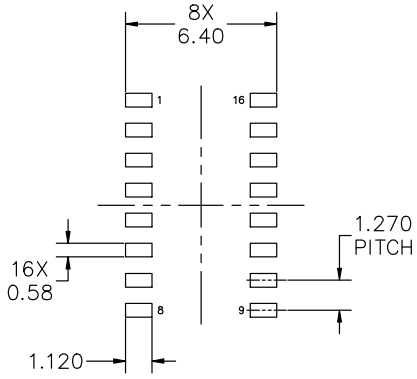


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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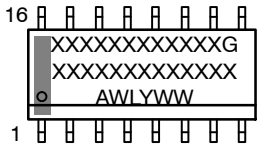
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SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

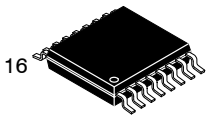
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1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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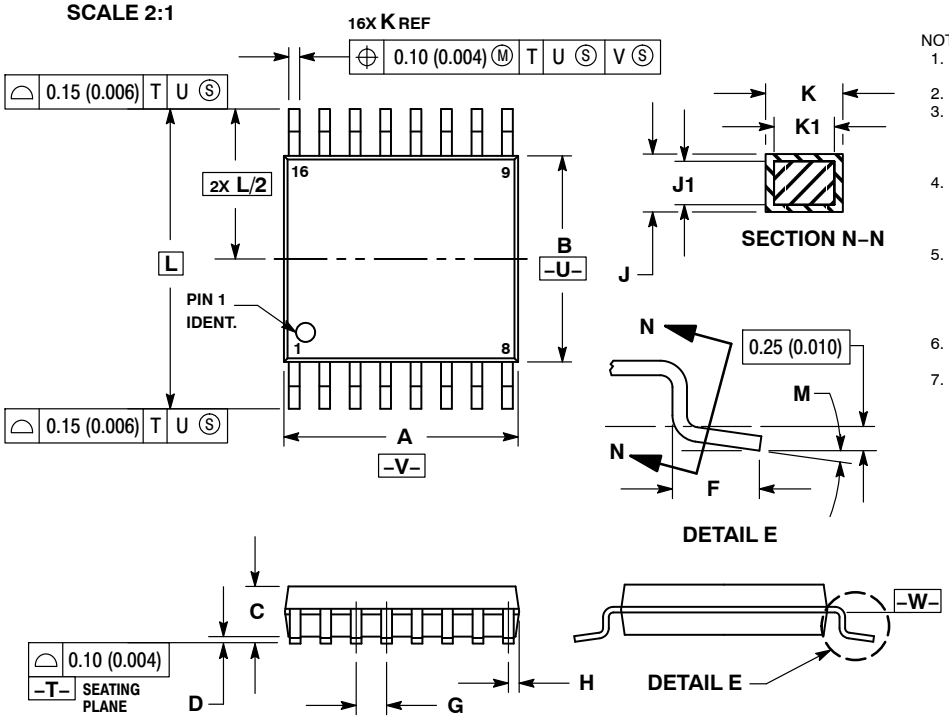
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SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

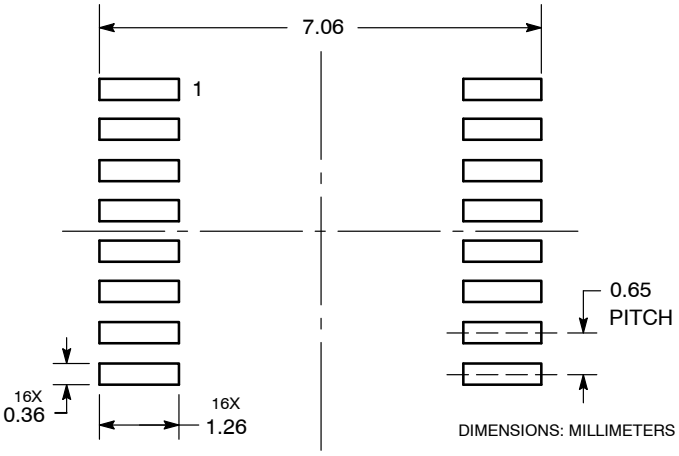
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NOTES:
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4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

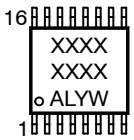
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B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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