552-02

Low Skew 2-Input MUX and 1 to 8 Clock Buffer

Description

The 552-02 is a low skew, single-input to eight-output clock buffer. The device offers a dual input with pin select for switching between two clock sources. For a low skew 1 to 4 buffer, see the 553.

Renesas makes many non-PLL and PLL-based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact Renesas for all of your clocking needs.

Features

- Low skew outputs: 50ps maximum
- Packaged in 16-pin TSSOP, Pb-free
- Low power CMOS technology
- Operating voltages of 2.5V to 5V
- Output Enable pin tri-states outputs
- 5V tolerant input clocks
- Input/Output clock frequency up to 200MHz
- Input clock multiplexer simplifies clock selection
- Industrial temperature

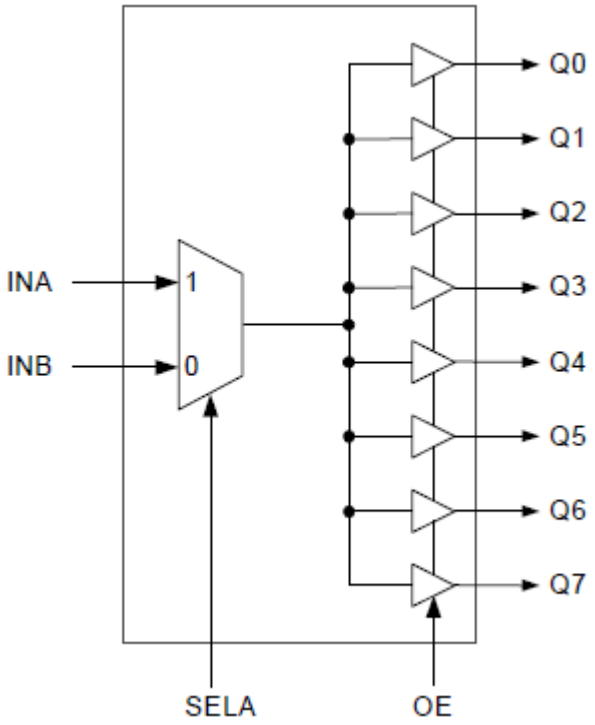


Figure 1. Block Diagram

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1. Pin Information

1.1 Pin Assignments

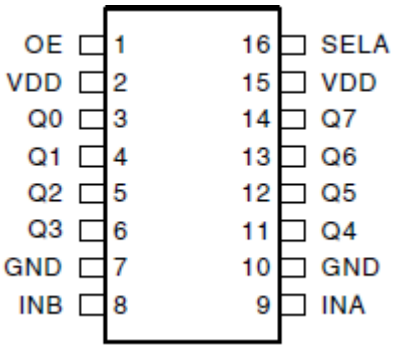


Figure 2. 16-TSSOP Pin Assignments – Top View

1.2 Input Source Select

SELA	Input
0	INB
1	INA

1.3 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	OE	Input	Output Enable. Tri-states outputs when low. Internal pull-up resistor.
2	VDD	Power	Connect to +2.5V, +3.3V or +5.0V. Must be the same as pin 15.
3	Q0	Output	Clock Output 0.
4	Q1	Output	Clock Output 1.
5	Q2	Output	Clock Output 2.
6	Q3	Output	Clock Output 3.
7	GND	Power	Connect to ground.
8	INB	Input	Clock Input B. 5.0V tolerant.
9	INA	Input	Clock Input A. 5.0V tolerant.
10	GND	Power	Connect to ground.
11	Q4	Output	Clock Output 4.
12	Q5	Output	Clock Output 5.
13	Q6	Output	Clock Output 6.
14	Q7	Output	Clock Output 7.
15	VDD	Power	Connect to +2.5V, +3.3V or +5.0V. Must be the same as pin 2.
16	SELA	Input	Selects either INA or INB. Internal pull-up resistor.

2. External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01µF should be connected between V_{DD} on pin 2 and GND on pin 7, and between V_{DD} on pin 15 and GND on pin 10, as close to the device as possible. A 33Ω series terminating resistor should be used on each clock output if the trace is longer than 1-inch.

To achieve the low output skews that the 552-02 is capable of, careful attention must be paid to board layout. Essentially, all 8 outputs must have identical terminations, identical loads, and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15ps of skew.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage, V_{DD}	-	-	7	V
SELA, OE and all Outputs	-	-0.5	V_{DD} + 0.5	V
INA and INB	-	0.5	5.5	V
Ambient Operating Temperature	T_{JMAX}	-40	+85	°C
Storage Temperature	T_{ST}	-65	+150	°C
Junction Temperature	V_{ESDHBM}	-	175	°C
Soldering Temperature	V_{ESDCDM}	-	260	°C

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature	-40	+85	°C
Power Supply Voltage (measured in respect GND)	+2.375	+5.25	V

3.3 DC Electrical Specifications

VDD = 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise specified.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Voltage	V_{DD}	-	2.375	-	2.625	V
Input High Voltage, INA, INB [1]	V_{IH}	-	$V_{DD}/2 + 0.5$	-	5.5	V
Input Low Voltage, INA, INB [1]	V_{IL}	-	-	-	$V_{DD}/2 - 0.5$	V
Input High Voltage, OE, SELA	V_{IH}	-	1.8	-	V_{DD}	V
Input Low Voltage, OE, SELA	V_{IL}	-	-	-	0.7	V
Output High Voltage	V_{OH}	I_{OH} = -16mA	2	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 16mA	-	-	0.4	V
Operating Supply Current	I_{DD}	No load, 135MHz	-	35	-	mA
Short Circuit Current	I_{OS}	Each output	-	60	-	mA

1. Nominal switching threshold is $V_{DD}/2$.

VDD = 3.3V ±5%; T_A = -40°C to +85°C, unless otherwise specified.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Voltage	V_{DD}	-	3.135	-	3.465	V
Input High Voltage, INA, INB [1]	V_{IH}	-	$V_{DD}/2 + 0.7$	-	5.5	V
Input Low Voltage, INA, INB [1]	V_{IL}	-	-	-	$V_{DD}/2 - 0.7$	V
Input High Voltage, OE, SELA	V_{IH}	-	2	-	V_{DD}	V
Input Low Voltage, OE, SELA	V_{IL}	-	-	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25mA	2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 25mA	-	-	0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12mA	V_{DD} - 0.4	-	-	V
Operating Supply Current	I_{DD}	No load, 135MHz	-	50	-	mA
Short Circuit Current	I_{OS}	Each output	-	80	-	mA

1. Nominal switching threshold is $V_{DD}/2$.

VDD = 5.0V ±5%; T_A = -40°C to +85°C, unless otherwise specified.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Voltage	V_{DD}	-	4.75	-	5.25	V
Input High Voltage, INA, INB [1]	V_{IH}	-	$V_{DD}/2 + 1$	-	5.5	V
Input Low Voltage, INA, INB [1]	V_{IL}	-	-	-	$V_{DD}/2 - 1$	V
Input High Voltage, OE, SELA	V_{IH}	-	2	-	V_{DD}	V
Input Low Voltage, OE, SELA	V_{IL}	-	-	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -35mA	2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 35mA	-	-	0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12mA	V_{DD} - 0.4	-	-	V
Operating Supply Current	I_{DD}	No load, 135MHz	-	85	-	mA
Short Circuit Current	I_{OS}	Each output	-	100	-	mA

1. Nominal switching threshold is $V_{DD}/2$.

3.4 AC Electrical Specifications

VDD = 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise specified.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Frequency	-	-	0	-	200	MHz
Output Rise Time	t_{OR}	0.8V to 2.0V, C_L = 15pF	-	1.0	1.5	ns
Output Fall Time	t_{OF}	2.0V to 0.8V, C_L = 15pF	-	1.0	1.5	ns
Propagation Delay [1]	-	-	-	3.5	-	ns
Output to Output Skew [2]	-	Rising edges at V_{DD}/2	-	0	50	ps
Input A to Input B Skew [3]	-	-	-	0	50	ps

1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.
3. Propagation delay matching through the part.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

VDD = 3.3V ±5%; T_A = -40°C to +85°C, unless otherwise specified.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Frequency	-	-	0	-	200	MHz
Output Rise Time	t_{OR}	0.8V to 2.0V, C_L = 15pF	-	0.6	1.0	ns
Output Fall Time	t_{OF}	2.0V to 0.8V, C_L = 15pF	-	0.6	1.0	ns
Propagation Delay [1]	-	-	2.0	3.0	5.5	ns
Output to Output Skew [2]	-	Rising edges at V_{DD}/2	-	0	50	ps
Input A to Input B Skew [3]	-	-	-	0	50	ps
Part-to-Part Skew		-	-	-	3.5	ns

1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.
3. Propagation delay matching through the part.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

VDD = 5.0V ±5%; T_A = -40°C to +85°C, unless otherwise specified.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Frequency	-	-	0	-	200	MHz
Output Rise Time	t_{OR}	0.8V to 2.0V, C_L = 15pF	-	0.3	0.7	ns
Output Fall Time	t_{OF}	2.0V to 0.8V, C_L = 15pF	-	0.3	0.7	ns
Propagation Delay [1]	-	-	-	2.8	-	ns
Output to Output Skew [2]	-	Rising edges at V_{DD}/2	-	0	50	ps
Input A to Input B Skew [3]	-	-	-	0	50	ps

1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.
3. Propagation delay matching through the part.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

4. Package Outline Drawings

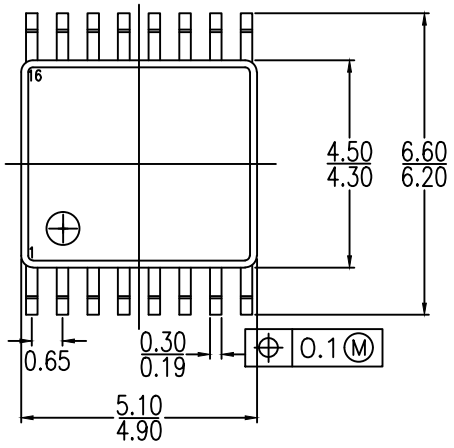
The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

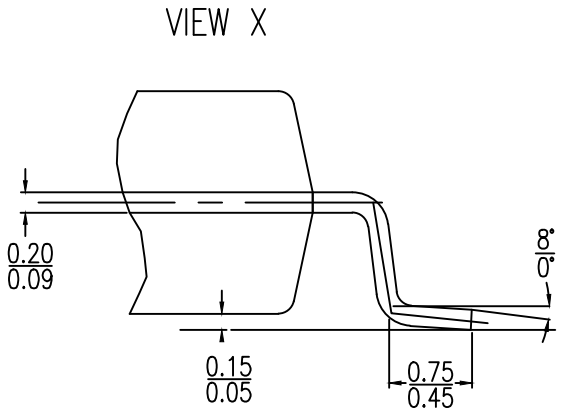
5. Ordering Information

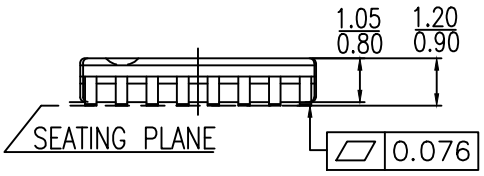
Part Number	Marking	Package Description	Carrier Type	Temperature Range
552G-02I	552G-02I	16-TSSOP, 4.4mm Body, 0.65 Pitch	Tubes	-40°C to +85°C
552G-02IT	552G-02I	16-TSSOP, 4.4mm Body, 0.65 Pitch	Tape and Reel	-40°C to +85°C
552G-02ILN	552G02IN	16-TSSOP, 4.4mm Body, 0.65 Pitch	Tubes	-40°C to +85°C
552G-02ILNT	552G02IN	16-TSSOP, 4.4mm Body, 0.65 Pitch	Tape and Reel	-40°C to +85°C

6. Revision History

Revision	Date	Description
1.09	Feb 25, 2025	Reformatted to Renesas template.
-	Feb 17, 2006	Formerly Revision H version of IDT branded datasheet.

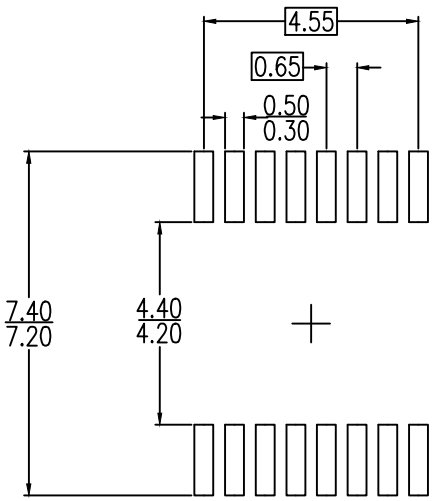






NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS

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LAND PATTERN DIMENSIONS

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1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
Jan 26, 2018	Rev 00	Revised from PSC-4056-02 PGG16

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