ESP-C3-12F-Kit Specification

Version V1.1

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Document development/revision/abolishment resume

Version	Date	Developed/revised content	Make	Verify
V1.0	2021.05.10	First developed	Yingying Chen	Hong Xu
V1.1	2021.05.27	Fix Size	Hong Xu	Hong Xu

CONTENT

1. Product overview

The ESP-C3-12F-Kit development board is a core development board designed by ESP-C3-12F for the ESP-C3-12F module. The development board continues the classic design of the NodeMCU development board, leading all I/O to the With pin headers, developers can connect peripherals according to their needs. When using the breadboard for development and debugging, the standard headers on both sides can make the operation easier and more convenient.

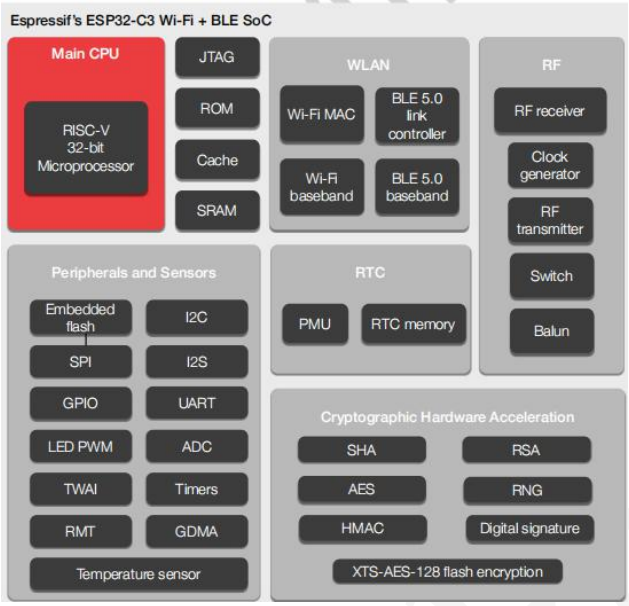
ESP-C3-12F Wi-Fi module is developed by Shenzhen Ai-Thinker Technology Co., Ltd. The module's core processor chip ESP32-C3 is a highly integrated low-power Wi-Fi and Bluetooth system-on-chip (SoC), designed for the Internet of Things (IoT), mobile devices, wearable electronic devices, smart homes, etc. Designed for various applications.

The ESP32-C3 chip has industry-leading low-power performance and radio frequency performance, and supports Wi-Fi IEEE802.11b/g/n protocol and BLE 5.0. The chip is equipped with a RISC-V 32-bit single-core processor with an operating frequency of up to 160 MHz. Support secondary development without using other microcontrollers or processors. The chip has built-in 400 KB SRAM, 384 KB ROM, 8KB RTC SRAM, built-in 4MB Flash also supports external Flash. The chip supports a variety of low power consumption working states, which can meet the power consumption requirements of various application scenarios. The chip's unique features such as fine clock gating function, dynamic voltage clock frequency adjustment function, and RF output power adjustable function can achieve the best balance between communication distance, communication rate and power consumption.

The ESP-C3-12F module provides a wealth of peripheral interfaces, including UART, PWM, SPI, I2S, I2C, ADC, temperature sensor and up to 15 GPIOs.

The ESP-C3-12F module has a variety of unique hardware security mechanisms. The hardware encryption accelerator supports AES, SHA and RSA algorithms. Among them, RNG, HMAC and digital signature (Digital Signature) modules provide more security features. Other security features include Flash encryption and secure boot (se-cure boot) signature verification. The perfect security mechanism enables the chip to be perfectly applied to various encryption products.

The ESP-C3-12F module supports low-power Bluetooth: Bluetooth5, Bluetooth mesh. Bluetooth rate support: 125Kbps, 500Kbps, 1Mbps, 2Mbps. Support broadcast extension, multi-broadcasting, channel selection.



Features

- Support Wi-Fi 802.11b/g/n, 1T1R mode data rate up to 150Mbps
- Support BLE5.0, does not support classic Bluetooth, rate support: 125Kbps, 500Kbps, 1Mbps, 2Mbps
- RISC-V 32-bit single-core processor, supports a clock frequency of up to 160 MHz, has 400 KB SRAM, 384 KB ROM, 8KB RTC SRAM
- Support UART/PWM/GPIO/ADC/I2C/I2S interface, support temperature sensor, pulse counter
- The development board has RGB three-in-one lamp beads, which is convenient for the second development of customers
- Support multiple sleep modes, deep sleep current is less than 5uA
- Serial port rate up to 5Mbps
- Support STA/AP/STA+AP mode and promiscuous mode
- Support Smart Config (APP)/AirKiss (WeChat) of Android and IOS, one-click network configuration
- Support serial port local upgrade and remote firmware upgrade (FOTA)
- General AT commands can be used quickly
- Support secondary development, integrated Windows and Linux development environment
- About Flash configuration ESP-C3-12F uses the built-in 4MByte Flash of the chip by default, and supports the external Flash version of the chip.

1.1 Main parameters

List 1 main parameters description

Model	ESP-C3-12F-Kit
Packaging	DIP-30
Size(module)	24.0*16.0*3.1(±0.2)MM
Antenna	PCB antenna/IPEX port
Spectrum range	2400 ~ 2483.5MHz
Working temperature	-40 ℃ ~ 85 ℃
Storage environment	-40 ℃ ~ 125 ℃ , < 90%RH
Power supply	Voltage 5V，current >500mA
Interface	UART/GPIO/ADC/PWM/I2C/I2S
IO port	IO0,IO1,IO2,IO3,IO4,IO5,IO8,IO9,IO10,IO18,IO19,IO20,IO21
Serial port rate	Support 110 ~ 4608000 bps ， default 115200 bps
Bluetooth	BLE 5.0
Safety	WEP/WPA-PSK/WPA2-PSK
SPI Flash	Default 4MByte，support 2MByte version
Onboard RGB interface	IO5 connects to RGB blue lamp beads; IO3 connects to RGB red lamp beads; IO4 connects to RGB green lamp beads

2.Electrical parameters

The ESP-C3-12F-Kit development board is an electrostatic sensitive device, and special precautions need to be taken when handling it

2.1Electrical characteristics

Parameters		Conditions	Min	Typical	Max	Unit
Voltage		VDD	3.0	3.3	5.0	V
I/O	V_{IL}/V_{IH}	-	-0.3/0.75VDD	-	0.25VDD/VDD+0.3	V
	V_{OL}/V_{OH}	-	N/0.8VIO	-	0.1VIO/N	V
	I_{MAX}	-	-	-	12	mA

2.2WIFI RF performance

Description	Typical	Unit
Working frequency	2400 - 2483.5	MHz
Output Power		
11n mode HT40, PA output power is	15±2	dBm
11n mode HT20, PA output power is	15±2	dBm
In 11g mode, PA output power is	16±2	dBm
In 11b mode, PA output power	18±2	dBm
Receiving sensitivity		
CCK, 1 Mbps	-96±2	dBm
CCK, 11 Mbps	-88±2	dBm

6 Mbps (1/2 BPSK)	-92±2	dBm
54 Mbps (3/4 64-QAM)	-75±2	dBm
HT20 (MCS7)	-73±2	dBm
HT40 (MCS7)	-70±2	dBm

2.3 BLE RF performance

Description	Typical	Unit
Output Power		
Transmit power	0±2	dBm
Receiving sensitivity Bluetooth low energy 1M		
Sensitivity @30.8%PER	-96±2	dBm

2.4 Power consumption

The following power consumption data is based on a 3.3V power supply, an ambient temperature of 25°C, and measured using an internal voltage regulator.

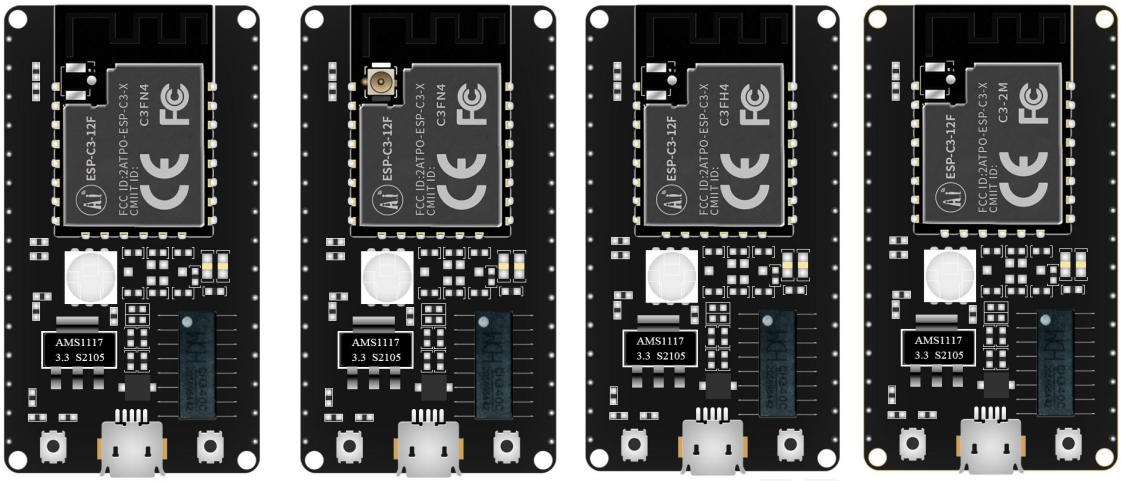
- All measurements are done at the antenna interface without SAW filter.
- All emission data is based on 90% duty cycle, measured in continuous emission mode.

Mode	Mix	Typical	Max	Unit
Transmit 802.11b, CCK 1Mbps, POUT=+20dBm	-	350	-	mA
Transmit 802.11g, OFDM 54Mbps, POUT =+18dBm	-	290	-	mA
Transmit 802.11n, MCS7, POUT =+17dBm	-	280	-	mA
Receive 802.11b, the packet length is 1024 bytes	-	90	-	mA
Receive 802.11g, the packet length is 1024 bytes	-	90	-	mA
Receive 802.11n, the packet length is 1024 bytes	-	93	-	mA

Modem-Sleep①	-	20	-	mA
Light-Sleep②	-	130	-	μA
Deep-Sleep③	-	5	-	μA
Power Off	-	1	-	μA

3.Exterior

The appearance of four different packages of ESP-C3-12F-Kit development board



(a) (b) (c) (d)

(The picture and silk screen are for reference only, the actual product shall prevail)

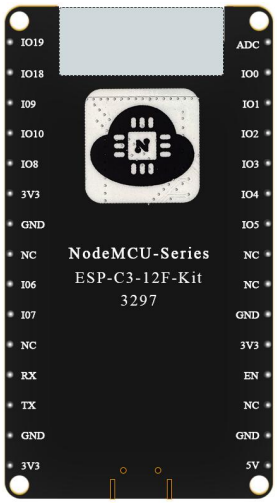
Different package selection description：

Figure (a) Type package (normal version): Compatible with PCB onboard antenna and IPEX external antenna, built-in 4M flash；

Figure (b) Type package (normal version): Compatible with PCB onboard antenna and IPEX external antenna, built-in 4M flash;

Figure (c) Type package (high temperature version): Compatible with PCB onboard antenna and IPEX external antenna, built-in 4M flash；

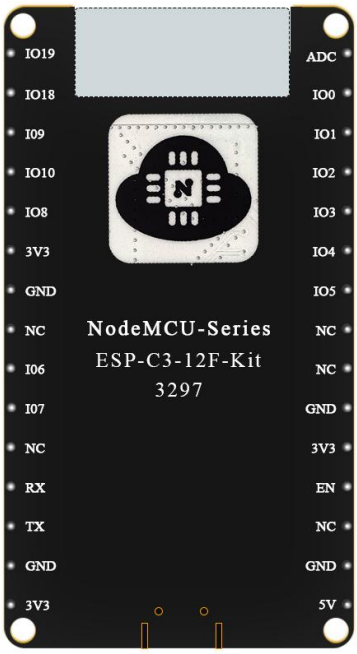
Figure (d) Type package: compatible with PCB onboard antenna and IPEX external antenna, external 2M flash；



(The picture and silk screen are for reference only, the actual product shall prevail)

4.Pin definition

The ESP-C3-12F-Kit development board module has a total of 30 interfaces, as shown in the pin diagram, the pin function definition table is the interface definition table



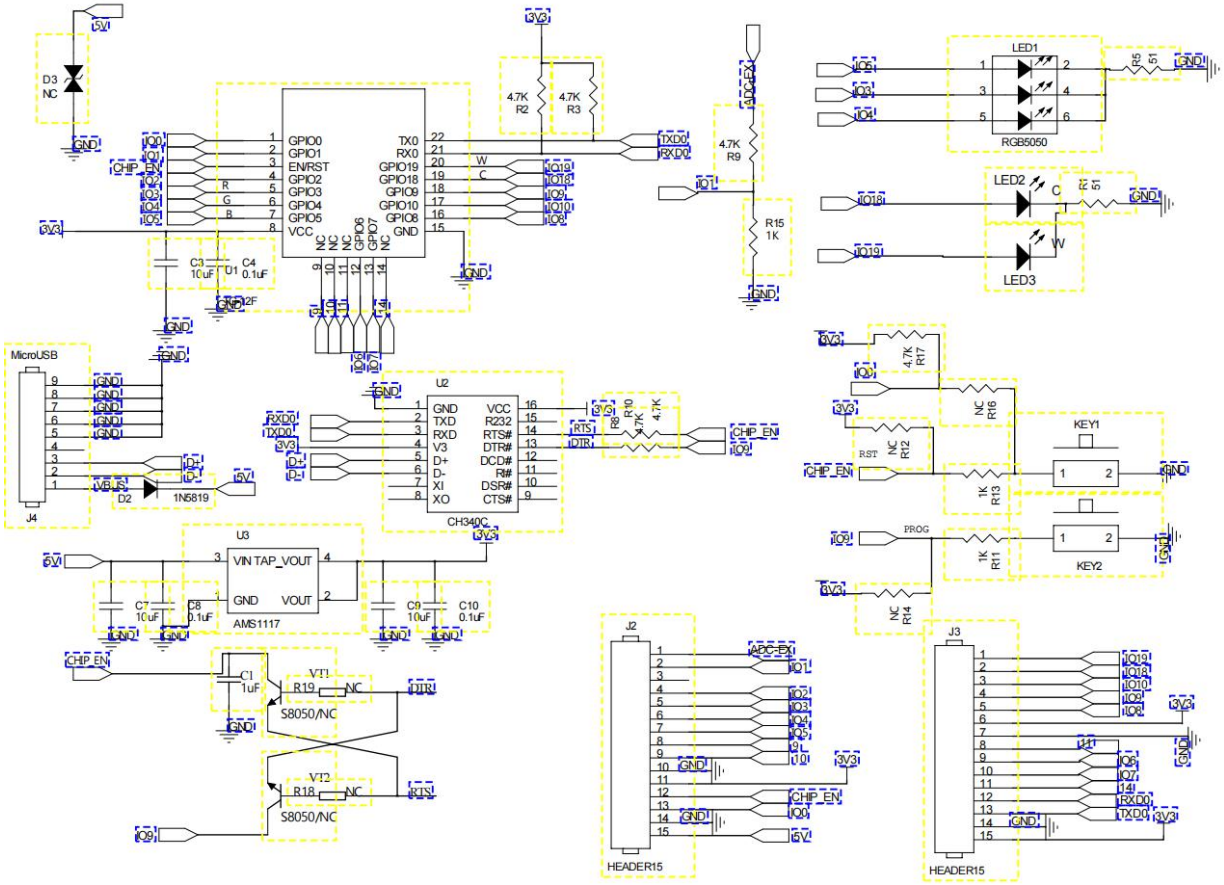
ESP-C3-12F-Kit pin diagram

Pin function definition table

No.	Name	Function description
1	ADC	ADC_CHECK(ADC1_CH0)
2	IO0	IO0 / ADC1_CH0 / XTAL_32K_N
3	IO1	IO1 / ADC1_CH1 / XTAL_32K_N
4	IO2	IO2 / ADC1_CH2 / FSPIQ
5	IO3	IO03 / ADC1_CH3
6	IO4	IO04 / ADC1_CH4 / FSPIHD / MTMS
7	IO5	IO05 / ADC2_CH0 / FSPIWP / MTDI
8	NC	NC
9	NC	NC
10	GND	GND
11	3V3	Digital 3.3V power output

12	EN	High level: chip enable;Low level: the chip is turned off; Note that the EN pin should not be left floating;
13	NC	NC
14	GND	GND
15	5V	5V power input
16	3V3	Digital 3.3V power output
17	GND	GND
18	TX	TX0 / IO21
19	RX	RX0 / IO20
20	NC	NC
21	IO7	IO7 / FSPID / MTDO
22	IO6	IO6 / FSPICLK / MTCK
23	NC	NC
24	GND	GND
25	3V3	Digital 3.3V power output
26	IO8	IO8
27	IO10	IO10 / FSPICSO
28	IO9	IO9
29	IO18	IO18
30	IO19	IO19

5.Schematic diagram



6.Design guide

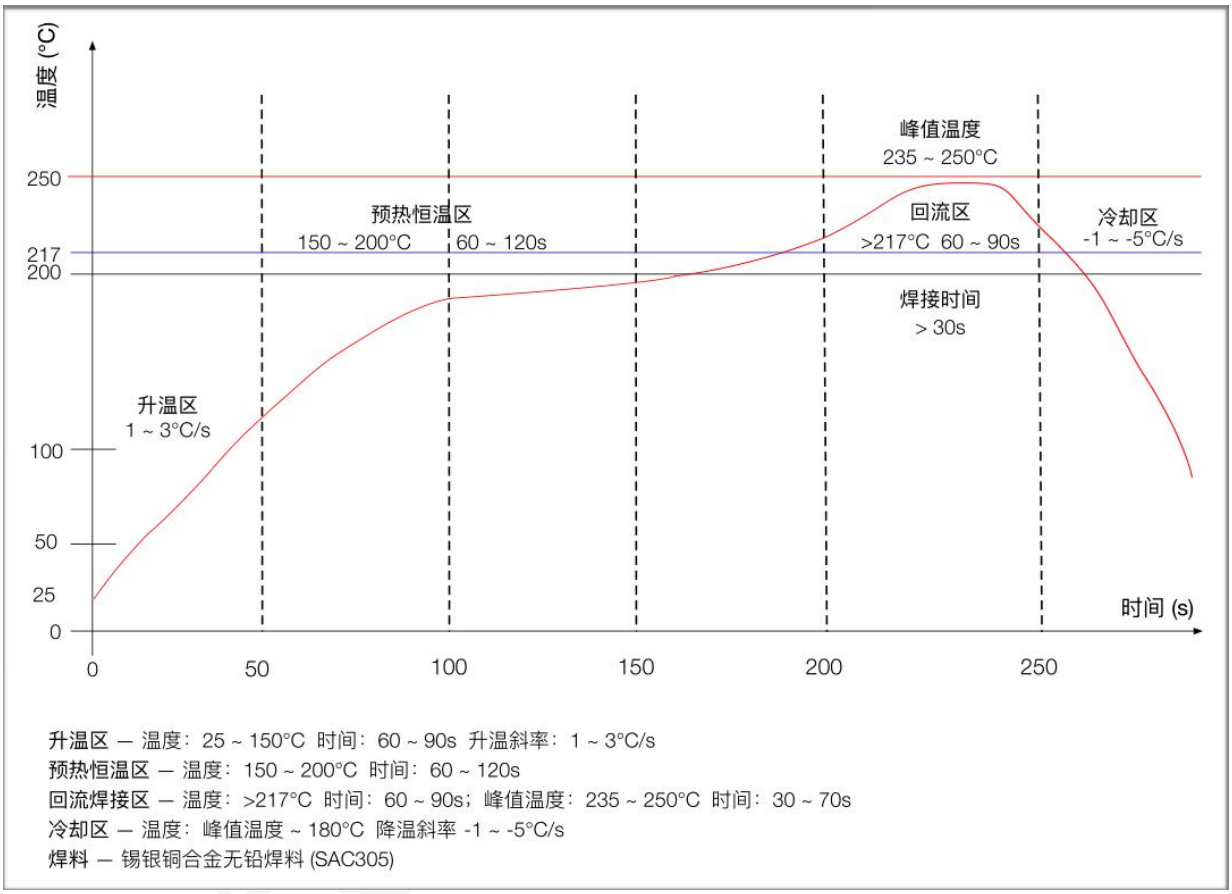
6.1 Power supply

- Recommended 5V voltage, peak current above 500mA
- It is recommended to use LDO for power supply; if using DC-DC, it is recommended that the ripple be controlled within 30mV
- It is recommended to reserve the position of the dynamic response capacitor for the DC-DC power supply circuit, which can optimize the output ripple when the load changes greatly.
- It is recommended to add ESD devices to the 5V power interface

6.2 Antenna layout requirements

It is forbidden to place metal parts around the module antenna, away from high-frequency components.

7.Reflow soldering curve



8.Package

The packaging of the ESP-C3-12F-Kit development board is an electrostatic bag with pearl cotton inserted.

9.Contact us

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