

BW20-12F Specification

Version V1.0.1

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Document resume

Version	Date	Develop/revise content	Edition	Approve
V1.0.0	2024.06.13	First Edition	Xihuan Lu	Ning Guang
V1.0.1	2024.12.31	Add special instructions for PSRAM version PA8 pin,update screen printing representative information for shielding cover,and remove Arduino development item	Xihuan Lu	Ning Guang

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1. Product overview

BW20-12F is a dual-band Wi-Fi + BLE SoC module developed by Ai-Thinker based on RTL8711 series chips, which supports dual-frequency (2.4 GHz or 5 GHz)802.11a/b/g/n WLAN protocol and Bluetooth 5.0 protocol. The BW 20-12F integrates dual-core MCU, a ARM V8.1 (Cortex-M4F compatible) high-performance MCU with a maximum frequency of 330 MHz; a ARM V8M (Cortex-M0 compatible) low-power MCU.

The BW20-12F module has rich peripheral interfaces, including UART / GPIO / ADC / PWM / IIC / SPI / SDIO / IR / SWD / USB etc. It can be widely used in the Internet of Things (IoT), mobile devices, wearable electronic devices, smart home and other fields.

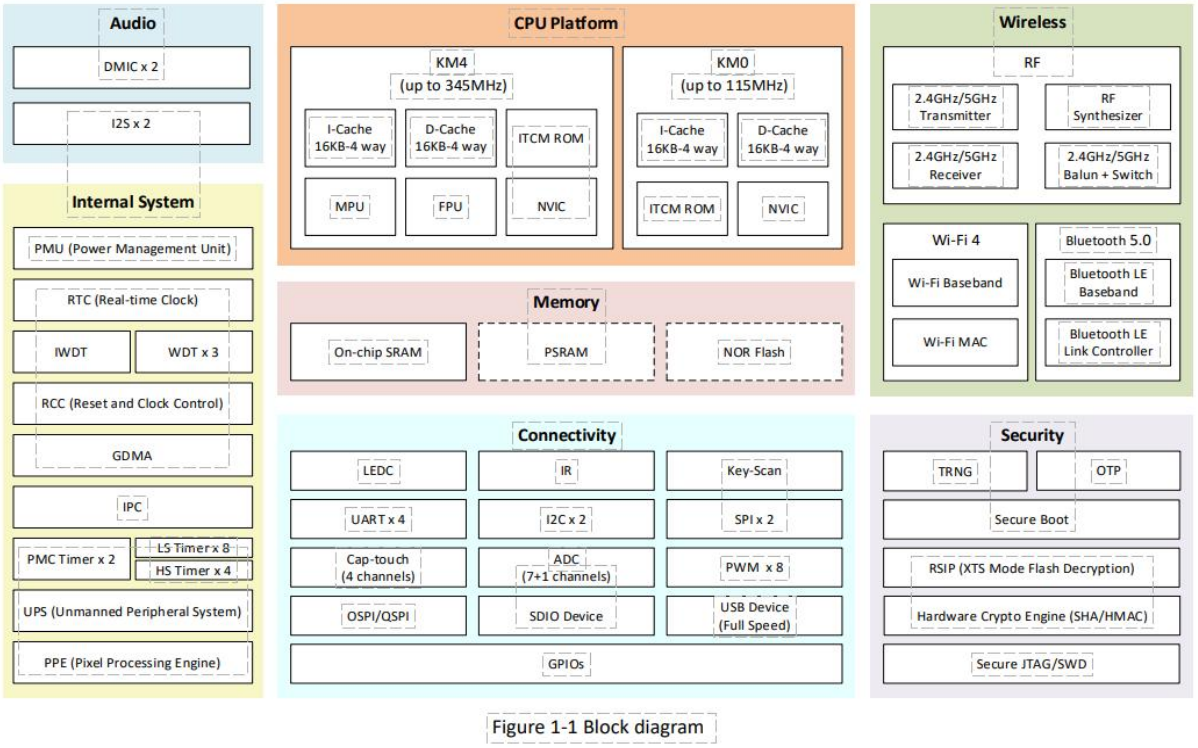


Figure 1-1 Block diagram

Figure 1 Chip Block Diagram

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1.1. Characteristic

- Support for the 802.11a/b/g/n protocol
- Support for dual-frequency 2.4GHz or 5GHz
- Supports the HT20 / HT40 mode
- Support for Bluetooth 5.0
- Support for BLE Long Range
- The Bluetooth supports a high-power mode LE data length extension
- Support for link layer privacy
- Support for the hardware encryption engine Integrated dual-core MCU, up to 330 MHz
- Abundant interfaces, with 17 flexible IO ports
- Wi-Fi and Bluetooth share the same antenna
- Support secondary development, support programming in Linux and Windows environments

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2. Main parameters

Table 1 Description of the main parameters

Model	BW20-12F
Package	SMD-22
Size	24*16*3.2(±0.2)MM
Antenna	on-board PCB antenna、IPEX connector（1st generation）
Frequency range	2400~2483.5MHz or 5180~5825MHz
Operating temperature	-40 ℃~85 ℃
Storage temperature	-40 ℃~125 ℃,<90%RH
Power supply	Voltage supply 3.0V~3.6V,typical value 3.3V. Current supply>500mA
Support interface	UART/GPIO/ADC/PWM/IIC/SPI/SDIO/IR/SWD/USB
Available IO	Default 17
UART rate	Default 115200bps
Bluetooth	BLE 5.0
SPI flash	Default 4MByte,Maximum support is 16MByte

2.1. Static electricity requirement

BW 20-12F module is electrostatic sensitive equipment, which requires special ESD precautions, and usually ESD protective devices should be added in use. Proper ESD handling and packaging must be used during the transportation, operation, and use of the BW 20-12F module. Do not touch the module by hand or use non-antistatic iron to damage the module.



Figure 2 ESD Anti-static diagram

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2.2. Electrical characteristics

Table 2 Electrical characteristics table

Parameters		Condition	Min.	Typical value	Max.	Unit
Voltage supply		3V3	3.0	3.3	3.6	V
I/O	VIL	-	-	-	0.3*VDD	V
	VIH	-	0.65*VDD	-	-	V
	VOL	-	-	0.15*VDD	-	V
	VOH	-	-	0.85*VDD	-	V

2.3. Wi-Fi RF performance

Table 3 Wi-Fi RF performance

Description	Typical value			Unit
Frequency range	2400~2483.5 and 5180~5825			MHz
Output power				
Mode	**Min. value**	**Typical value**	**Max.**	**Unit**
11a mode，PA output power	-	18	-	dBm
11b mode，PA output power	-	19	-	dBm
11g mode，PA output power	-	18	-	dBm
11n mode，PA output power	-	17	-	dBm
Receiving sensitivity				
Mode	**Min.value**	**Typical value**	**Max.**	**Unit**
11b，1Mbps	-	-99	-	dBm
11b，11Mbps	-	-90	-	dBm
11a/g，6Mbps	-	-94	-	dBm
11a/g，54Mbps	-	-76	-	dBm
HT20（MCS0）	-	-93	-	dBm
HT20（MCS7）	-	-74	-	dBm
HT40（MCS0）	-	-91	-	dBm
HT40（MCS7）	-	-71	-	dBm

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2.4. BLE RF performance

Table 4 BLE RF performance

Description	Typical value			Unit
Frequency range	2400 ~ 2484MHz			MHz
Output power				
Rate mode	**Min.value**	**Typical value**	**Max.value**	**Unit**
1Mbps	-	15	-	dBm
2Mbps	-	15	-	dBm
Receiving sensitivity				
Rate mode	**Min.value**	**Typical value**	**Max.value**	**Unit**
1Mbps @30.8%PER	-	-99	-	dBm
2Mbps @30.8%PER	-	-97	-	dBm

2.5. Power Consumption

The following power consumption data is based on a 3.3V power supply and an ambient temperature of 25°C.

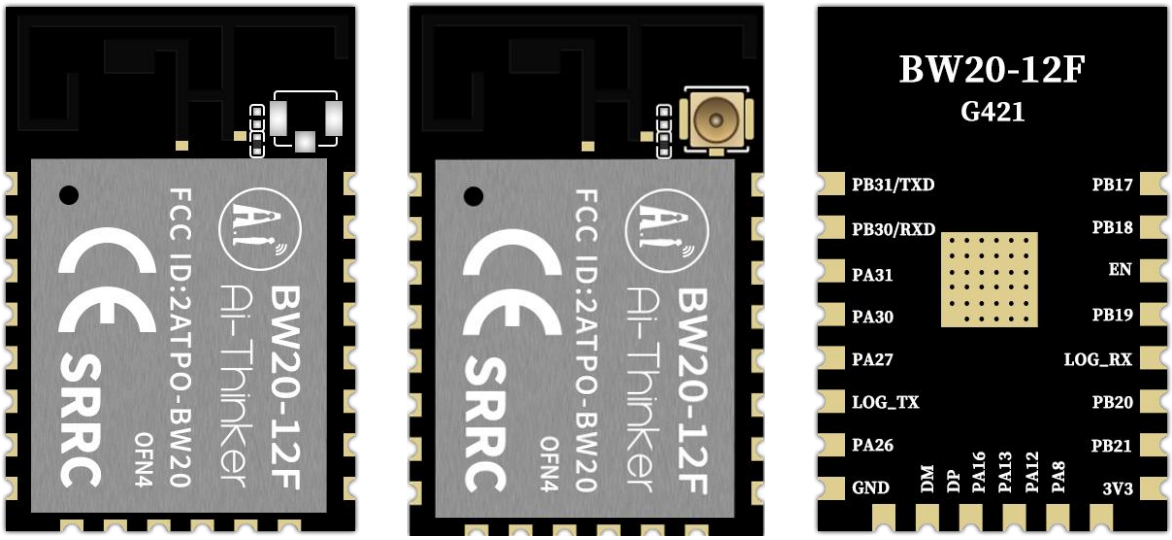
- POUT power for all transmission modes is measured at the antenna interface.
- All emission data are measured in continuous emission mode.

Table 5 Power consumption table

Mode	Min.value	Typical	Max.va	Unit
Transmitting 802.11b,11Mbps,POUT=+22dBm	-	355	-	mA
Transmitting 802.11g, 54Mbps, POUT	-	95	-	mA
Transmitting 802.11n, MCS7, POUT	-	93	-	mA
Receive 802.11b	-	40	-	mA
Receive 802.11g	-	40	-	mA
Receive 802.11n	-	40	-	mA

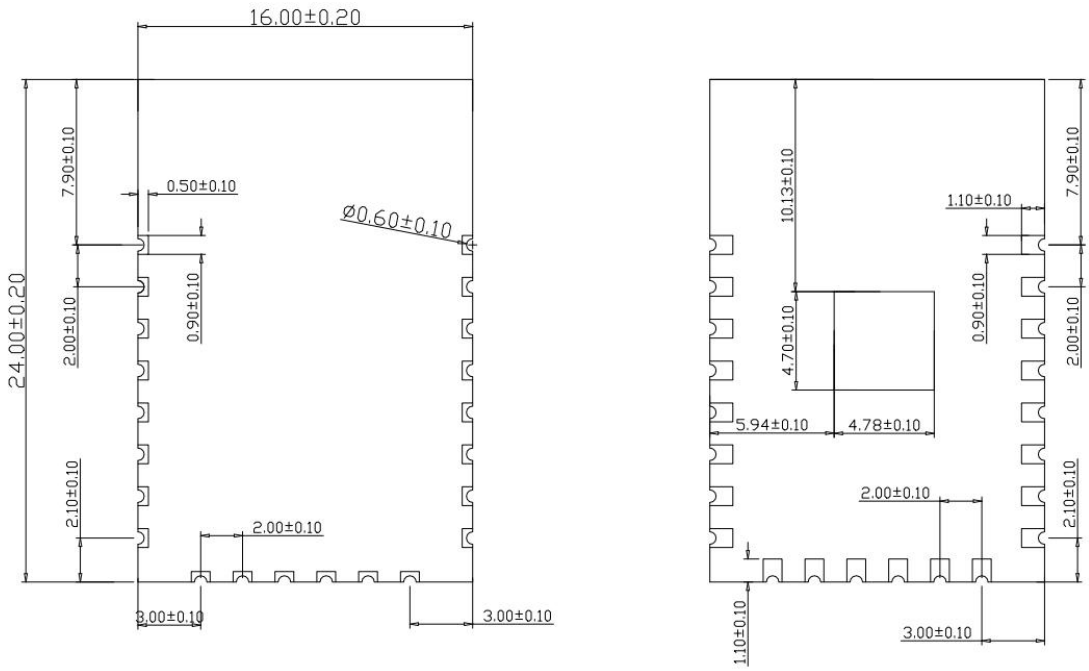
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3. Appearance dimensions



Front Front Back

Figure 3 Appearance diagram (Rendering figure is for reference only,subject to physical objects)



Front Back

Figure 4 Size diagram

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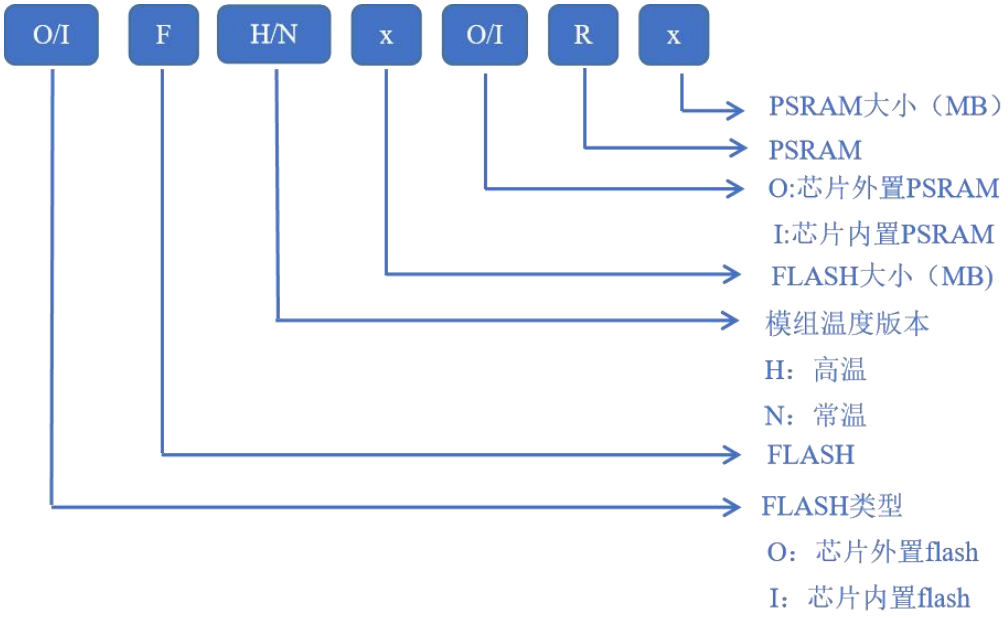
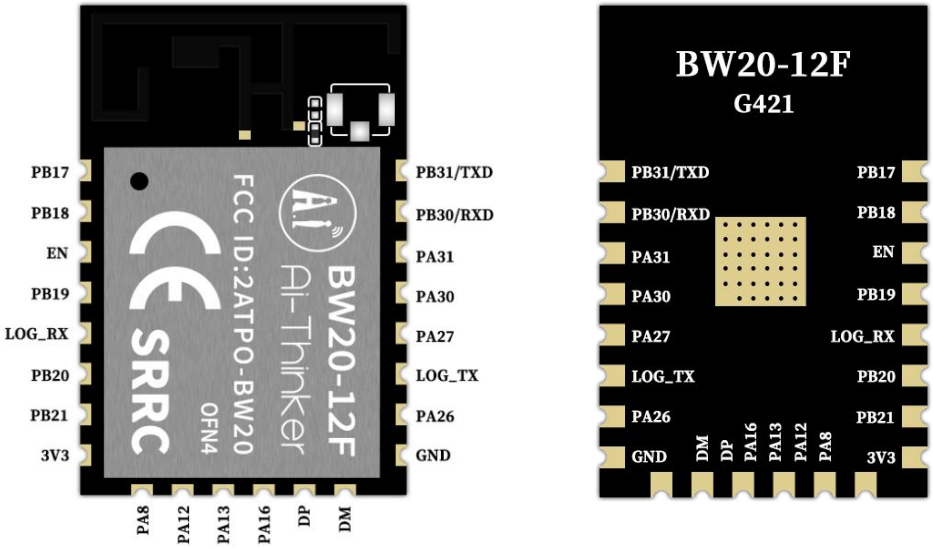


Figure 5 The screen cover information

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4. Pin definition

BW20-12F is connected a total of 22 pins, as in the pin schematic diagram, and the definition of the pin function is shown in the following table.



Front Back

Figure 6 Pin diagram

Table 5 Pin function definition table

No.	Name	Function description
1	PB17	TOUCH2_ADC2/SPI1_CS/SD_D3
2	PB18	TOUCH1_ADC1/SPI1_CLK/SD_CMD
3	EN	Chips enable pin and pull up effectively
4	PB19	TOUCH0_ADC0/SPI1_MOSI/SD_CLK
5	LOG_RX	UART_LOG_RXD，Firmware download RX pin
6	PB20	SPI1_MISO/SWD_CLK/SD_D0
7	PB21	SPI1_CS/SWD_DAT/SD_D1
8	3V3	3.3V power supply（VDD），the external power supply output current is recommended in above 500mA
9	PA8	PSRAM_DQ5/TIM8_TRIG/LDOM_OUT;When the built-in PSRAM version is used as the PSRAM power supply pin, PA8 is not available
10	PA12	SPI0_CS/SD_D2/TIM9_TRIG

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11	PA13	The default is not available and the IO is occupied by Flash inside the module. Please contact Ai-Thinker if need to use. SD_D2/external Flash this pin is NC
12	PA16	The default is not available and the IO is occupied by Flash inside the module. Please contact Ai-Thinker if need to use. SPI0_MISO/SD_CLK/external Flash this pin is NC
13	DP	PA29/SPI1_CLK/SD_CLK/FSDP
14	DM	PA28/SPI0_MISO/SD_CMD/FSDM
15	GND	Ground
16	PA26	SPI0_CLK/SD_D2
17	LOG_TX	UART _ LOG _ TXD, TX pin for download firmware, do not external pull down will enter Flash download mode
18	PA27	SPI0_MOSI/SD_D3
19	PA30	SPI1_MOSI/SWD_CLK/SD_D0，default function is SWD DATA，IC can be configured as PA31
20	PA31	SPI1_MISO/SWD_DAT/SD_D1，fefault function is SWD DATA，IC can be configured as PA31
21	PB30/RXD	UART 1 _ RXD, do not external pull down, external pull down will enter Load OTP settings
22	PB31/TXD	UART 1 _ TXD, do not external pull down, external pull down will enter the chip test mode

Note: 1. When LOG_TX is low level at the moment of power-on, the module enters the burning mode; when it is high level at the moment of power-on, the module starts normally and defaults is pull-up.
2. PA13 and PA16 are internally occupied in the external Flash version. At this time, these two IOs are unavailable and the pins are left floating.
3. PB30 / RXD Do not external pull down, external pull down will enter the Load OTP settings.
4. PB31 / TXD do not external down, external down will enter the chip test mode.
5. PA8:PA8 is available in the regular version (without PSRAM version), When using the PSRAM version.PA8 is the PSRAM power supply pin and is not available.

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5. Schematic diagram

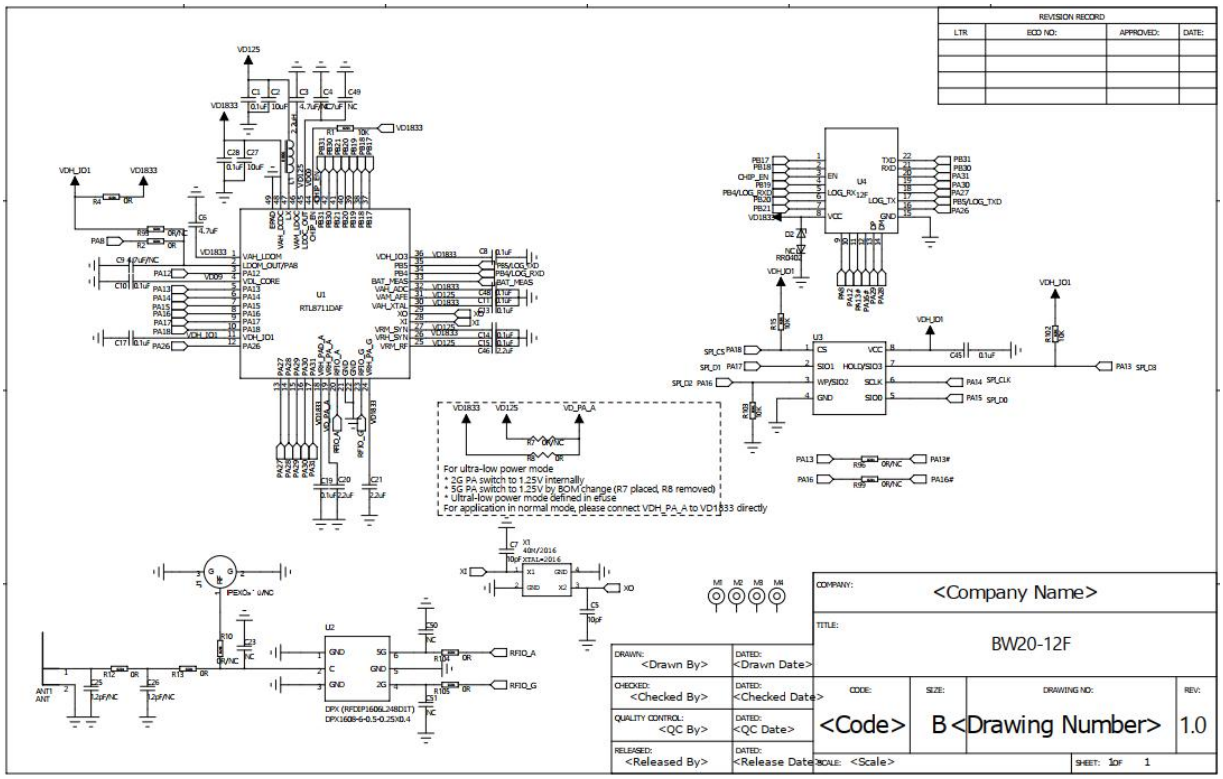


Figure 7 Schematic diagram

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6. Design guide

6.1. Circuit guidance of application

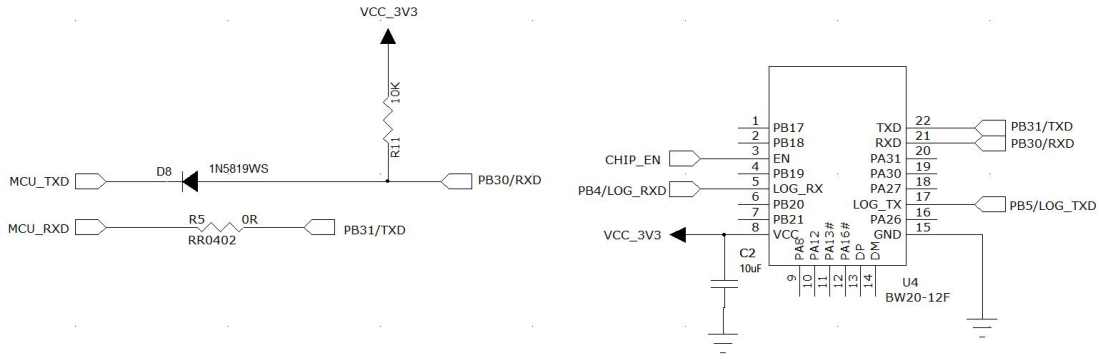


Figure 8 Circuit guidance of application

Note：

- LOG _ TX is the starting control pin in normal operating mode at high level and burning firmware mode at low level. Internal chip default high level.

6.2. Recommend PCB package size

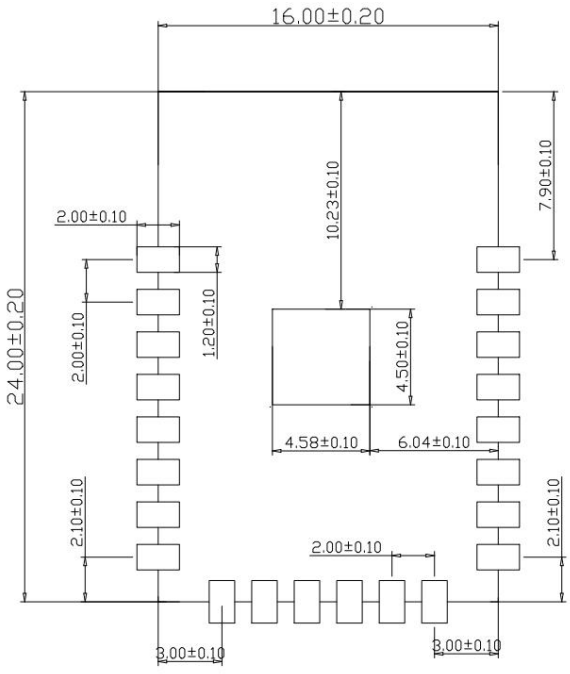


Figure 9 Recommend PCB package size（TOP view）

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6.3. Antenna layout requirements

- In the installation position on the motherboard, the following two ways are recommended:

Scheme 1: put the module on the edge of the motherboard, and the antenna area extends of the edge of the motherboard.

Scheme two: put the module on the edge of the motherboard, which hollowed an area in the antenna position.

- In order to meet the performance of on-board antenna, metal parts are prohibited around the antenna, away from high-frequency devices.

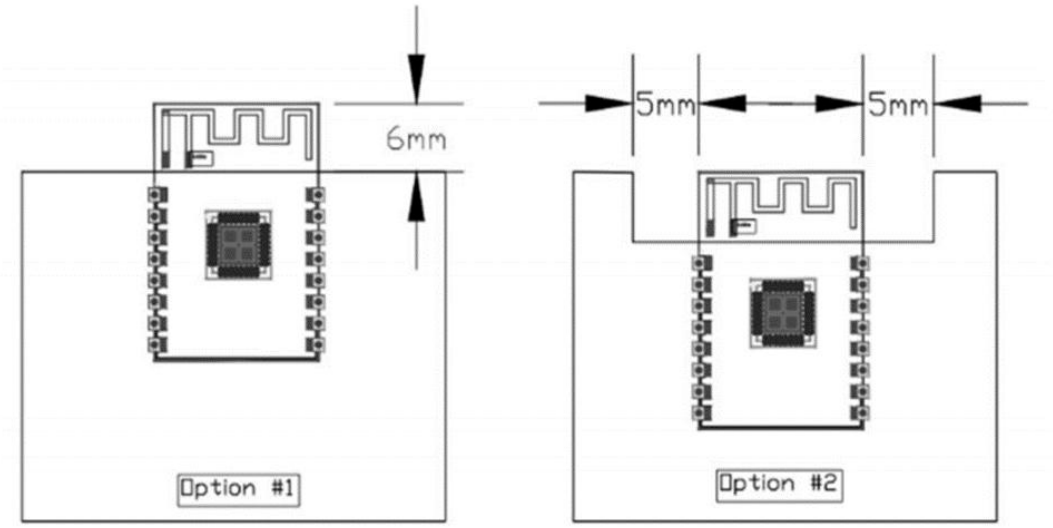


Figure 10 Schematic diagram of the antenna layout

6.4. Power supply

- Recommended 3.3V voltage, peak current above 500 mA.
- It is recommended to use LDO; if DC-DC, ripple control within 30 mV.
- The DC-DC power supply circuit suggests to reserve the position of the dynamic response capacitor, which can optimize the output ripple when the load change is large.
- 3.3V power interface, it is recommended to add ESD devices.
- If the power supply is boosted from 1.5V to 3.0V for more than 15 ms, add the voltage reset IC or use the wide voltage version Flash.
- During the repeated up and down process, if the voltage cannot be less than 0.3V, the voltage reset IC must be increased.

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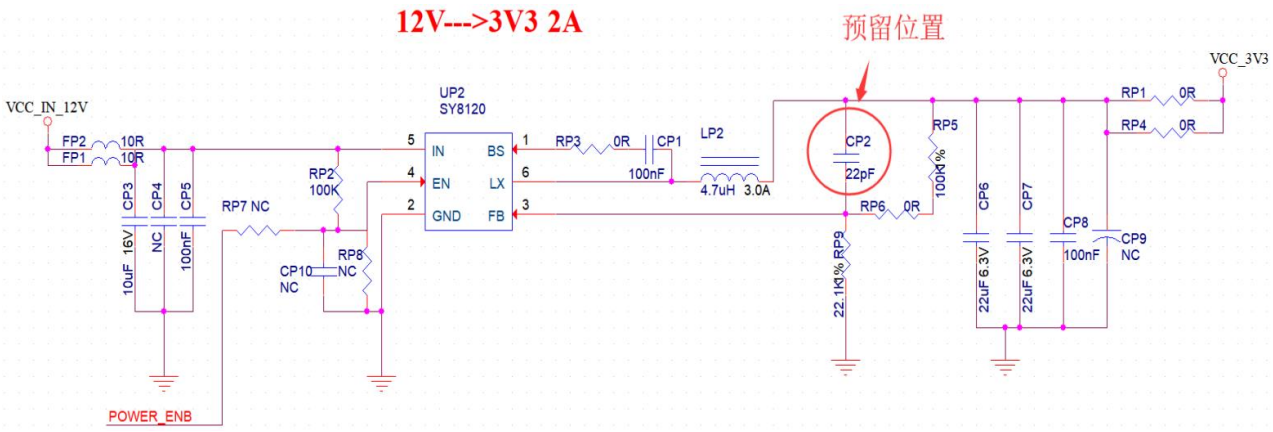


Figure 11 The DC-DC step-down circuit diagram

6.5. GPIO

- There are some IO ports on the periphery of the module. If you need to use it, it is recommended to connect a 10-100 ohm resistor in series with the IO port. This inhibits overshoot and makes both sides level more stable. It is helpful for EMI and ESD.
- For special I/O ports to be pulled up and down, refer to the usage instructions in the specifications, which may affect the module startup configuration.
- The IO port of the module is 3.3V. If the IO level of the main control and the module do not match, a level conversion circuit needs to be added.
- If the I/O port is directly connected to a peripheral port or terminals, for example, a pin row, reserve an ESD device near the terminal of the I/O cable.

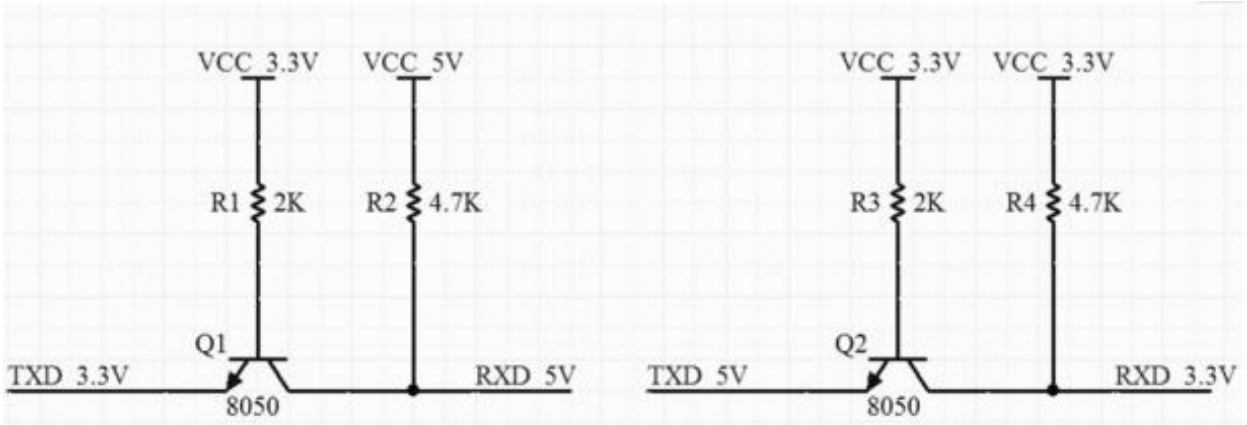


Figure 12 The level conversion circuit

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7. Storage conditions

Products sealed in moisture-proof bags should be stored in a non-condensing atmosphere of <40 ° C /90%RH.

The module has a moisture sensitivity rating of MSL 3.

After the vacuum bag is opened, it must be used within 168 hours at 25±5℃/60%RH, otherwise it needs to be baked before it can be put on line again.

8. Reflow welding curve diagram

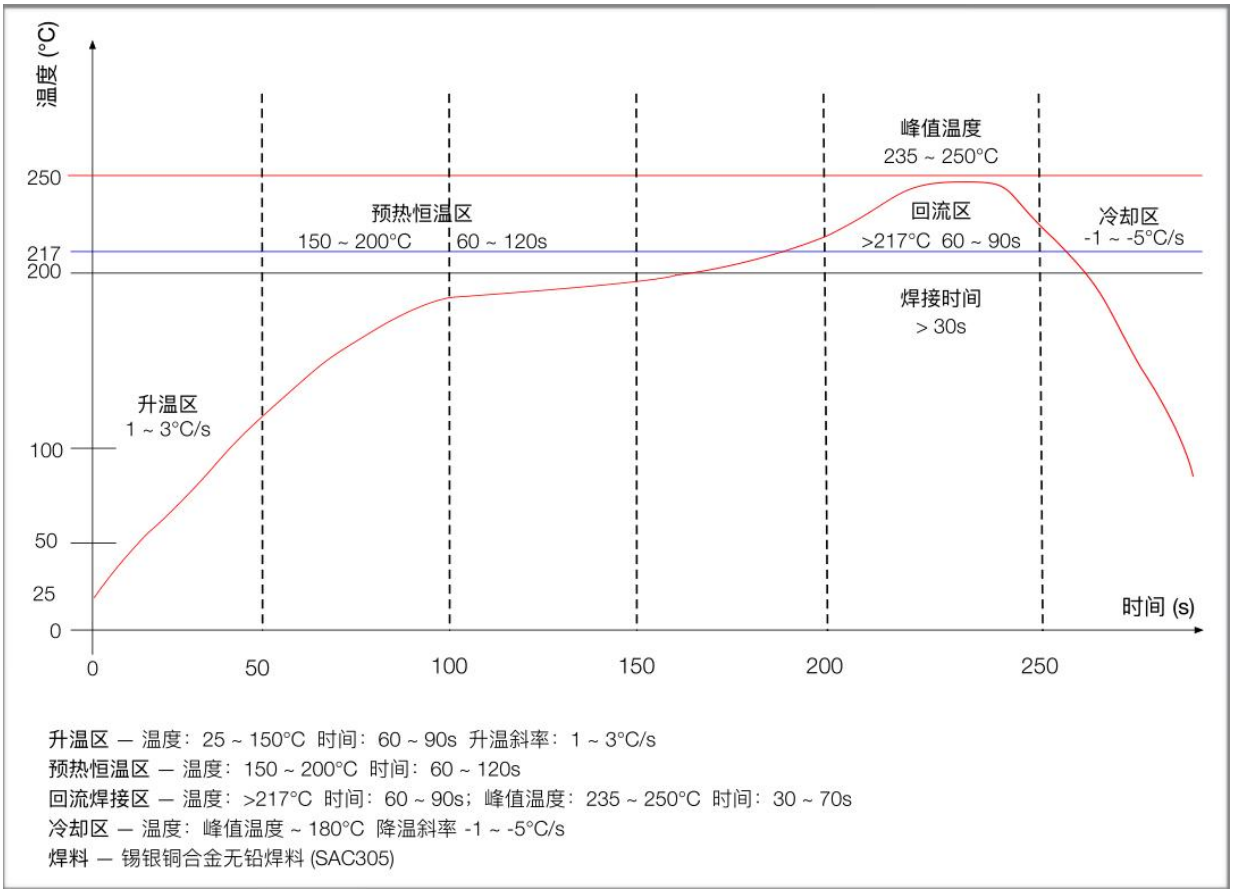


Figure 13 Reflow welding diagram

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9. Product Packaging Information

BW20-12F module module was packaged in a tape, 800pcs/reel.As shown in the below image:



Figure 14 Package and packing diagram

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