7 Series FPGAs Data Sheet: Overview

DS180 (v2.6.1) September 8, 2020 **Product Specification**

General Description

Xilinx® 7 series FPGAs comprise four FPGA families that address the complete range of system requirements, ranging from low cost, small form factor, cost-sensitive, high-volume applications to ultra high-end connectivity bandwidth, logic capacity, and signal processing capability for the most demanding high-performance applications. The 7 series FPGAs include:

- Spartan®-7 Family: Optimized for low cost, lowest power, and high I/O performance. Available in low-cost, very small form-factor packaging for smallest PCB footprint.
- Artix®-7 Family: Optimized for low power applications requiring serial transceivers and high DSP and logic throughput. Provides the lowest total bill of materials cost for high-throughput, cost-sensitive applications.
- Kintex®-7 Family: Optimized for best price-performance with a 2X improvement compared to previous generation, enabling a new class of FPGAs.
- Virtex®-7 Family: Optimized for highest system performance and capacity with a 2X improvement in system performance. Highest capability devices enabled by stacked silicon interconnect (SSI) technology.

Built on a state-of-the-art, high-performance, low-power (HPL), 28 nm, high-k metal gate (HKMG) process technology, 7 series FPGAs enable an unparalleled increase in system performance with 2.9 Tb/s of I/O bandwidth, 2 million logic cell capacity, and 5.3 TMAC/s DSP, while consuming 50% less power than previous generation devices to offer a fully programmable alternative to ASSPs and ASICs.

Summary of 7 Series FPGA Features

- Advanced high-performance FPGA logic based on real 6-input look-up table (LUT) technology configurable as distributed memory.
- 36 Kb dual-port block RAM with built-in FIFO logic for on-chip data buffering.
- High-performance SelectIO™ technology with support for DDR3 interfaces up to 1,866 Mb/s.
- High-speed serial connectivity with built-in multi-gigabit transceivers from 600 Mb/s to max. rates of 6.6 Gb/s up to 28.05 Gb/s, offering a special low-power mode, optimized for chip-to-chip interfaces.
- A user configurable analog interface (XADC), incorporating dual 12-bit 1MSPS analog-to-digital converters with on-chip thermal and supply sensors.
- DSP slices with 25 x 18 multiplier, 48-bit accumulator, and pre-adder for high-performance filtering, including optimized symmetric coefficient filtering.
- Powerful clock management tiles (CMT), combining phase-locked loop (PLL) and mixed-mode clock manager (MMCM) blocks for high precision and low jitter.
- Quickly deploy embedded processing with MicroBlaze™ processor.
- Integrated block for PCI Express® (PCIe), for up to x8 Gen3 Endpoint and Root Port designs.
- Wide variety of configuration options, including support for commodity memories, 256-bit AES encryption with HMAC/SHA-256 authentication, and built-in SEU detection and correction.
- Low-cost, wire-bond, bare-die flip-chip, and high signal integrity flip-chip packaging offering easy migration between family members in the same package. All packages available in Pb-free and selected packages in Pb option.
- Designed for high performance and lowest power with 28 nm, HKMG, HPL process, 1.0V core voltage process technology and 0.9V core voltage option for even lower power.

Table 1: **7 Series Families Comparison**

Max. Capability	Spartan-7	Artix-7	Kintex-7	Virtex-7
Logic Cells	102K	215K	478K	1,955K
Block RAM(1)	4.2 Mb	13 Mb	34 Mb	68 Mb
DSP Slices	160	740	1,920	3,600
DSP Performance(2)	176 GMAC/s	929 GMAC/s	2,845 GMAC/s	5,335 GMAC/s
MicroBlaze CPU(3)	260 DMIPs	303 DMIPs	438 DMIPs	441 DMIPs
Transceivers	–	16	32	96
Transceiver Speed	–	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s
Serial Bandwidth	–	211 Gb/s	800 Gb/s	2,784 Gb/s
PCIe Interface	–	x4 Gen2	x8 Gen2	x8 Gen3
Memory Interface	800 Mb/s	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
I/O Pins	400	500	500	1,200
I/O Voltage	1.2V–3.3V	1.2V–3.3V	1.2V–3.3V	1.2V–3.3V
Package Options	Low-Cost, Wire-Bond	Low-Cost, Wire-Bond, Bare-Die Flip-Chip	Bare-Die Flip-Chip and High-Performance Flip-Chip	Highest Performance Flip-Chip

Notes:
1. Additional memory available in the form of distributed RAM.
2. Peak DSP performance numbers are based on symmetrical filter implementation.
3. Peak MicroBlaze CPU performance numbers based on microcontroller preset.

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Spartan-7 FPGA Feature Summary

Table 2: **Spartan-7 FPGA Feature Summary by Device**

Device	Logic Cells	CLB		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe	GT	XADC Blocks	Total I/O Banks[5]	Max User I/O
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7S6	6,000	938	70	10	10	5	180	2	0	0	0	2	100
XC7S15	12,800	2,000	150	20	20	10	360	2	0	0	0	2	100
XC7S25	23,360	3,650	313	80	90	45	1,620	3	0	0	1	3	150
XC7S50	52,160	8,150	600	120	150	75	2,700	5	0	0	1	5	250
XC7S75	76,800	12,000	832	140	180	90	3,240	8	0	0	1	8	400
XC7S100	102,400	16,000	1,100	160	240	120	4,320	8	0	0	1	8	400

Notes:

1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Does not include configuration Bank 0.

Table 3: **Spartan-7 FPGA Device-Package Combinations and Maximum I/Os**

Package	CPGA196	CSGA225	CSGA324	FTGB196	FGGA484	FGGA676
Size (mm)	8 x 8	13 x 13	15 x 15	15 x 15	23 x 23	27 x 27
Ball Pitch (mm)	0.5	0.8	0.8	1.0	1.0	1.0
Device	HR I/O[1]	HR I/O[1]	HR I/O[1]	HR I/O[1]	HR I/O[1]	HR I/O[1]
XC7S6	100	100		100		
XC7S15	100	100		100		
XC7S25		150	150	100		
XC7S50			210	100	250	
XC7S75					338	400
XC7S100					338	400

Notes:

1. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Artix-7 FPGA Feature Summary

Table 4: **Artix-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTPs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7A12T	12,800	2,000	171	40	40	20	720	3	1	2	1	3	150
XC7A15T	16,640	2,600	200	45	50	25	900	5	1	4	1	5	250
XC7A25T	23,360	3,650	313	80	90	45	1,620	3	1	4	1	3	150
XC7A35T	33,280	5,200	400	90	100	50	1,800	5	1	4	1	5	250
XC7A50T	52,160	8,150	600	120	150	75	2,700	5	1	4	1	5	250
XC7A75T	75,520	11,800	892	180	210	105	3,780	6	1	8	1	6	300
XC7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	8	1	6	300
XC7A200T	215,360	33,650	2,888	740	730	365	13,140	10	1	16	1	10	500

Notes:
1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Artix-7 FPGA Interface Blocks for PCI Express support up to x4 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTP transceivers.

Table 5: **Artix-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	CPG236		CPG238		CSG324		CSG325		FTG256		SBG484		FGG484[2]		FBG484[2]		FGG676[3]		FBG676[3]		FFG1156	
Size (mm)	10 x 10		10 x 10		15 x 15		15 x 15		17 x 17		19 x 19		23 x 23		23 x 23		27 x 27		27 x 27		35 x 35	
Ball Pitch (mm)	0.5		0.5		0.8		0.8		1.0		0.8		1.0		1.0		1.0		1.0		1.0	
Device	GTP[4]	I/O HR[5]	GTP[4]	I/O HR[5]	GTP[4]	I/O HR[5]	GTP[4]	I/O HR[5]	GTP[4]	I/O HR[5]	GTP	I/O HR[5]	GTP[4]	I/O HR[5]	GTP	I/O HR[5]	GTP[4]	I/O HR[5]	GTP	I/O HR[5]	GTP	I/O HR[5]
XC7A12T			2	112			2	150														
XC7A15T	2	106			0	210	4	150	0	170			4	250								
XC7A25T			2	112			4	150														
XC7A35T	2	106			0	210	4	150	0	170			4	250								
XC7A50T	2	106			0	210	4	150	0	170			4	250								
XC7A75T					0	210			0	170			4	285			8	300				
XC7A100T					0	210			0	170			4	285			8	300				
XC7A200T											4	285			4	285			8	400	16	500

Notes:
1. All packages listed are Pb-free (SBG, FBG, FFG with exemption 15). Some packages are available in Pb option.
2. Devices in FGG484 and FBG484 are footprint compatible.
3. Devices in FGG676 and FBG676 are footprint compatible.
4. GTP transceivers in CP, CS, FT, and FG packages support data rates up to 6.25 Gb/s.
5. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Kintex-7 FPGA Feature Summary

Table 6: **Kintex-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTXs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7K70T	65,600	10,250	838	240	270	135	4,860	6	1	8	1	6	300
XC7K160T	162,240	25,350	2,188	600	650	325	11,700	8	1	8	1	8	400
XC7K325T	326,080	50,950	4,000	840	890	445	16,020	10	1	16	1	10	500
XC7K355T	356,160	55,650	5,088	1,440	1,430	715	25,740	6	1	24	1	6	300
XC7K410T	406,720	63,550	5,663	1,540	1,590	795	28,620	10	1	16	1	10	500
XC7K420T	416,960	65,150	5,938	1,680	1,670	835	30,060	8	1	32	1	8	400
XC7K480T	477,760	74,650	6,788	1,920	1,910	955	34,380	8	1	32	1	8	400

Notes:
1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Kintex-7 FPGA Interface Blocks for PCI Express support up to x8 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTX transceivers.

Table 7: **Kintex-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	FBG484			FBG676[2]			FFG676[2]			FBG900[3]			FFG900[3]			FFG901			FFG1156		
Size (mm)	23 x 23			27 x 27			27 x 27			31 x 31			31 x 31			31 x 31			35 x 35		
Ball Pitch (mm)	1.0			1.0			1.0			1.0			1.0			1.0			1.0		
Device	GTX[4]	I/O		GTX[4]	I/O		GTX	I/O		GTX[4]	I/O		GTX	I/O		GTX	I/O		GTX	I/O	
		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]
XC7K70T	4	185	100	8	200	100															
XC7K160T	4	185	100	8	250	150	8	250	150												
XC7K325T				8	250	150	8	250	150	16	350	150	16	350	150						
XC7K355T																24	300	0			
XC7K410T				8	250	150	8	250	150	16	350	150	16	350	150						
XC7K420T																28	380	0	32	400	0
XC7K480T																28	380	0	32	400	0

Notes:
1. All packages listed are Pb-free (FBG, FFG with exemption 15). Some packages are available in Pb option.
2. Devices in FBG676 and FFG676 are footprint compatible.
3. Devices in FBG900 and FFG900 are footprint compatible.
4. GTX transceivers in FB packages support the following maximum data rates: 10.3Gb/s in FBG484; 6.6Gb/s in FBG676 and FBG900. Refer to *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS182) for details.
5. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
6. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Virtex-7 FPGA Feature Summary

Table 8: **Virtex-7 FPGA Feature Summary**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTX	GTH	GTZ	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]	SLRs[8]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)									
XC7V585T	582,720	91,050	6,938	1,260	1,590	795	28,620	18	3	36	0	0	1	17	850	N/A
XC7V2000T	1,954,560	305,400	21,550	2,160	2,584	1,292	46,512	24	4	36	0	0	1	24	1,200	4
XC7VX330T	326,400	51,000	4,388	1,120	1,500	750	27,000	14	2	0	28	0	1	14	700	N/A
XC7VX415T	412,160	64,400	6,525	2,160	1,760	880	31,680	12	2	0	48	0	1	12	600	N/A
XC7VX485T	485,760	75,900	8,175	2,800	2,060	1,030	37,080	14	4	56	0	0	1	14	700	N/A
XC7VX550T	554,240	86,600	8,725	2,880	2,360	1,180	42,480	20	2	0	80	0	1	16	600	N/A
XC7VX690T	693,120	108,300	10,888	3,600	2,940	1,470	52,920	20	3	0	80	0	1	20	1,000	N/A
XC7VX980T	979,200	153,000	13,838	3,600	3,000	1,500	54,000	18	3	0	72	0	1	18	900	N/A
XC7VX1140T	1,139,200	178,000	17,700	3,360	3,760	1,880	67,680	24	4	0	96	0	1	22	1,100	4
XC7VH580T	580,480	90,700	8,850	1,680	1,880	940	33,840	12	2	0	48	8	1	12	600	2
XC7VH870T	876,160	136,900	13,275	2,520	2,820	1,410	50,760	18	3	0	72	16	1	6	300	3

Notes:
1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Virtex-7 T FPGA Interface Blocks for PCI Express support up to x8 Gen 2. Virtex-7 XT and Virtex-7 HT Interface Blocks for PCI Express support up to x8 Gen 3, with the exception of the XC7VX485T device, which supports x8 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTX, GTH, or GTZ transceivers.
8. Super logic regions (SLRs) are the constituent parts of FPGAs that use SSI technology. Virtex-7 HT devices use SSI technology to connect SLRs with 28.05 Gb/s transceivers.

Table 9: **Virtex-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	FFG1157				FFG1761[2]				FHG1761[2]				FLG1925		
Size (mm)	35 x 35				42.5 x 42.5				45 x 45				45 x 45		
Ball Pitch	1.0				1.0				1.0				1.0		
Device	GTX	GTH	I/O		GTX	GTH	I/O		GTX	GTH	I/O		GTX	I/O	
			HR[3]	HP[4]			HR[3]	HP[4]			HR[3]	HP[4]		HR[3]	HP[4]
XC7V585T	20	0	0	600	36	0	100	750							
XC7V2000T									36	0	0	850	16	0	1,200
XC7VX330T	0	20	0	600	0	28	50	650							
XC7VX415T	0	20	0	600											
XC7VX485T	20	0	0	600	28	0	0	700							
XC7VX550T															
XC7VX690T	0	20	0	600	0	36	0	850							
XC7VX980T															
XC7VX1140T															

Notes:
1. All packages listed are Pb-free (FFG, FHG, FLG with exemption 15). Some packages are available in Pb option.
2. Devices in FFG1761 and FHG1761 are footprint compatible.
3. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
4. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Table 10: **Virtex-7 FPGA Device-Package Combinations and Maximum I/Os - Continued**

Package[1]	FFG1158			FFG1926[2]			FLG1926[2]			FFG1927			FFG1928[3]			FLG1928[3]			FFG1930[4]			FLG1930[4]		
Size (mm)	35 x 35			45 x 45			45 x 45			45 x 45			45 x 45			45 x 45			45 x 45			45 x 45		
Ball Pitch	1.0			1.0			1.0			1.0			1.0			1.0			1.0			1.0		
Device	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O
			HP[5]			HP[5]			HP[5]			HP[5]			HP[5]			HP[5]			HP[5]			HP[5]
XC7V585T																								
XC7V2000T																								
XC7VX330T																								
XC7VX415T	0	48	350							0	48	600												
XC7VX485T	48	0	350							56	0	600							24	0	700			
XC7VX550T	0	48	350							0	80	600												
XC7VX690T	0	48	350	0	64	720				0	80	600							0	24	1,000			
XC7VX980T				0	64	720							0	72	480				0	24	900			
XC7VX1140T							0	64	720							0	96	480				0	24	1,100

Notes:
1. All packages listed are Pb-free (FFG, FLG with exemption 15). Some packages are available in Pb option.
2. Devices in FFG1926 and FLG1926 are footprint compatible.
3. Devices in FFG1928 and FLG1928 are footprint compatible.
4. Devices in FFG1930 and FLG1930 are footprint compatible.
5. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Table 11: **Virtex-7 HT FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	FLG1155			FLG1931			FLG1932		
Size (mm)	35 x 35			45 x 45			45 x 45		
Ball Pitch	1.0			1.0			1.0		
Device	GTH	GTZ	I/O HP[2]	GTH	GTZ	I/O HP[2]	GTH	GTZ	I/O HP[2]
XC7VH580T	24	8	400	48	8	600			
XC7VH870T							72	16	300

Notes:
1. All packages listed are Pb-free with exemption 15. Some packages are available in Pb option.
2. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Stacked Silicon Interconnect (SSI) Technology

There are many challenges associated with creating high capacity FPGAs that Xilinx addresses with the SSI technology. SSI technology enables multiple super logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single FPGA with more than ten thousand inter-SLR connections, providing ultra-high bandwidth connectivity with low latency and low power consumption. There are two types of SLRs used in Virtex-7 FPGAs: a logic intensive SLR used in the Virtex-7 T devices and a DSP/block RAM/transceiver-rich SLR used in the Virtex-7 XT and HT devices. SSI technology enables the production of higher capability FPGAs than traditional manufacturing methods, enabling the highest capacity and highest performance FPGAs ever created to reach production more quickly and with less risk than would otherwise be possible. Thousands of super long line (SLL) routing resources and ultra-high performance clock lines that cross between the SLRs ensure that designs span seamlessly across these high-density programmable logic devices.

CLBs, Slices, and LUTs

Some key features of the CLB architecture include:

- Real 6-input look-up tables (LUTs)
- Memory capability within the LUT
- Register and shift register functionality

The LUTs in 7 series FPGAs can be configured as either one 6-input LUT (64-bit ROMs) with one output, or as two 5-input LUTs (32-bit ROMs) with separate outputs but common addresses or logic inputs. Each LUT output can optionally be registered in a flip-flop. Four such LUTs and their eight flip-flops as well as multiplexers and arithmetic carry logic form a slice, and two slices form a configurable logic block (CLB). Four of the eight flip-flops per slice (one per LUT) can optionally be configured as latches.

Between 25–50% of all slices can also use their LUTs as distributed 64-bit RAM or as 32-bit shift registers (SRL32) or as two SRL16s. Modern synthesis tools take advantage of these highly efficient logic, arithmetic, and memory features.

Clock Management

Some of the key highlights of the clock management architecture include:

- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering

Each 7 series FPGA has up to 24 clock management tiles (CMTs), each consisting of one mixed-mode clock manager (MMCM) and one phase-locked loop (PLL).

Mixed-Mode Clock Manager and Phase-Locked Loop

The MMCM and PLL share many characteristics. Both can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of both components is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers: D, M, and O. The pre-divider D (programmable by configuration and afterwards via DRP) reduces the input frequency and feeds one input of the traditional PLL phase/frequency comparator. The feedback divider M (programmable by configuration and afterwards via DRP) acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each can be selected to drive one of the output dividers (six for the PLL, O0 to O5, and seven for the MMCM, O0 to O6), each programmable by configuration to divide by any integer from 1 to 128.

The MMCM and PLL have three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-bandwidth mode has the best jitter attenuation but not the smallest phase offset. High-bandwidth mode has the best phase offset, but not the best jitter attenuation. Optimized mode allows the tools to find the best setting.

MMCM Additional Programmable Features

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of $^1/_8$ and can thus increase frequency synthesis capabilities by a factor of 8.

The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1600 MHz, the phase-shift timing increment is 11.2 ps.

Clock Distribution

Each 7 series FPGA provides six different types of clock lines (BUFG, BUFR, BUFIO, BUFH, BUFMR, and the high-performance clock) to address the different clocking requirements of high fanout, short propagation delay, and extremely low skew.

Global Clock Lines

In each 7 series FPGA (except XC7S6 and XC7S15), 32 global clock lines have the highest fanout and can reach every flip-flop clock, clock enable, and set/reset, as well as many logic inputs. There are 12 global clock lines within any clock region driven by the horizontal clock buffers (BUFH). Each BUFH can be independently enabled/disabled, allowing for clocks to be turned off within a region, thereby offering fine-grain control over which clock regions consume power. Global clock lines can be driven by global clock buffers, which can also perform glitchless clock multiplexing and clock enable functions. Global clocks are often driven from the CMT, which can completely eliminate the basic clock distribution delay.

Regional Clocks

Regional clocks can drive all clock destinations in their region. A region is defined as an area that is 50 I/O and 50 CLB high and half the chip wide. 7 series FPGAs have between two and twenty-four regions. There are four regional clock tracks in every region. Each regional clock buffer can be driven from any of four clock-capable input pins, and its frequency can optionally be divided by any integer from 1 to 8.

I/O Clocks

I/O clocks are especially fast and serve only I/O logic and serializer/deserializer (SerDes) circuits, as described in the I/O Logic section. The 7 series devices have a direct connection from the MMCM to the I/O for low-jitter, high-performance interfaces.

Block RAM

Some of the key features of the block RAM include:

- Dual-port 36 Kb block RAM with port widths of up to 72
- Programmable FIFO logic
- Built-in optional error correction circuitry

Every 7 series FPGA has between 5 and 1,880 dual-port block RAMs, each storing 36 Kb. Each block RAM has two completely independent ports that share nothing but the stored data.

Synchronous Operation

Each memory access, read or write, is controlled by the clock. All inputs, data, address, clock enables, and write enables are registered. Nothing happens without a clock. The input address is always clocked, retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency.

During a write operation, the data output can reflect either the previously stored data, the newly written data, or can remain unchanged.

Programmable Data Width

Each port can be configured as 32K × 1, 16K × 2, 8K × 4, 4K × 9 (or 8), 2K × 18 (or 16), 1K × 36 (or 32), or 512 × 72 (or 64). The two ports can have different aspect ratios without any constraints.

Each block RAM can be divided into two completely independent 18 Kb block RAMs that can each be configured to any aspect ratio from 16K × 1 to 512 × 36. Everything described previously for the full 36 Kb block RAM also applies to each of the smaller 18 Kb block RAMs.

Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18 Kb RAM) or 36 bits (36 Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72.

Both sides of the dual-port 36 Kb RAM can be of variable width.

Two adjacent 36 Kb block RAMs can be configured as one cascaded 64K × 1 dual-port RAM without any additional logic.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, almost full, and almost empty. The almost full and almost empty flags are freely programmable. Similar to the block RAM, the FIFO width and depth are programmable, but the write and read ports always have identical width.

First word fall-through mode presents the first-written word on the data output even before the first read operation. After the first word has been read, there is no difference between this mode and the standard mode.

Digital Signal Processing — DSP Slice

Some highlights of the DSP functionality include:

- 25 × 18 two's complement multiplier/accumulator high-resolution (48 bit) signal processor
- Power saving pre-adder to optimize symmetrical filter applications
- Advanced features: optional pipelining, optional ALU, and dedicated buses for cascading

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All 7 series FPGAs have many dedicated, full custom, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 25 × 18 bit two's complement multiplier and a 48-bit accumulator, both capable of operating up to 741 MHz. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The DSP also includes a 48-bit-wide Pattern Detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

Input/Output

Some highlights of the input/output functionality include:

- High-performance SelectIO technology with support for 1,866 Mb/s DDR3
- High-frequency decoupling capacitors within the package for enhanced signal integrity
- Digitally Controlled Impedance that can be 3-stated for lowest power, high-speed I/O operation

The number of I/O pins varies depending on device and package size. Each I/O is configurable and can comply with a large number of I/O standards. With the exception of the supply pins and a few dedicated configuration pins, all other package pins have the same I/O capabilities, constrained only by certain banking rules. The I/O in 7 series FPGAs are classed as high range (HR) or high performance (HP). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.2V to 1.8V.

HR and HP I/O pins in 7 series FPGAs are organized in banks, with 50 pins per bank. Each bank has one common V_{CCO} output supply, which also powers certain input buffers. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). There are two V_{REF} pins per bank (except configuration bank 0). A single bank can have only one V_{REF} voltage value.

Xilinx 7 series FPGAs use a variety of package types to suit the needs of the user, including small form factor wire-bond packages for lowest cost; conventional, high performance flip-chip packages; and bare-die flip-chip packages that balance smaller form factor with high performance. In the flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Controlled ESR discrete decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All 7 series devices support differential standards beyond LVDS: RSDS, BLVDS, differential SSTL, and differential HSTL.

Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended SSTL and differential SSTL. The SSTL I/O standard can support data rates of up to 1,866 Mb/s for DDR3 interfacing applications.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input and some outputs can be individually delayed by up to 32 increments of 78 ps, 52 ps, or 39 ps each. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O structure. Each I/O pin possesses an 8-bit IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 3, 4, 5, 6, 7, or 8 bits. By cascading two IOSERDES from two adjacent pins (default from differential I/O), wider width conversions of 10 and 14 bits can also be supported. The ISERDES has a special oversampling mode capable of asynchronous data recovery for applications like a 1.25 Gb/s LVDS I/O-based SGMII interface.

Low-Power Gigabit Transceivers

Some highlights of the Low-Power Gigabit Transceivers include:

- High-performance transceivers capable of up to 6.6 Gb/s (GTP), 12.5 Gb/s (GTX), 13.1 Gb/s (GTH), or 28.05 Gb/s (GTZ) line rates depending on the family, enabling the first single device for 400G implementations.
- Low-power mode optimized for chip-to-chip interfaces.
- Advanced Transmit pre and post emphasis, receiver linear equalization (CTLE), and decision feedback equalization (DFE) for long reach or backplane applications. Auto-adaption at receiver equalization and on-chip Eye Scan for easy serial link tuning.

Ultra-fast serial data transmission to optical modules, between ICs on the same PCB, over the backplane, or over longer distances is becoming increasingly popular and important to enable customer line cards to scale to 100 Gb/s and onwards to 400 Gb/s. It requires specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues at these high data rates.

The transceiver count in the 7 series FPGAs ranges from up to 16 transceiver circuits in the Artix-7 family, up to 32 transceiver circuits in the Kintex-7 family, and up to 96 transceiver circuits in the Virtex-7 family. Each serial transceiver is a combined transmitter and receiver. The various 7 series serial transceivers use either a combination of ring oscillators and

LC tank or, in the case of the GTZ, a single LC tank architecture to allow the ideal blend of flexibility and performance while enabling IP portability across the family members. The different 7 series family members offer different top-end data rates. The GTP operates up to 6.6 Gb/s, the GTX operates up to 12.5 Gb/s, the GTH operates up to 13.1 Gb/s, and the GTZ operates up to 28.05 Gb/s. Lower data rates can be achieved using FPGA logic-based oversampling. The serial transmitter and receiver are independent circuits that use an advanced PLL architecture to multiply the reference frequency input by certain programmable numbers up to 100 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80. Additionally, the GTZ transmitter supports up to 160 bit data widths. This allows the designer to trade-off datapath width for timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits. Additionally, the GTZ receiver supports up to 160 bit data widths. This allows the FPGA designer to trade-off internal datapath width versus logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable linear and decision feedback equalizers (to compensate for PC board and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally guarantees sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the FPGA logic using the RXUSRCLK clock. For short channels, the transceivers offers a special low power mode (LPM) to reduce power consumption by approximately 30%.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCI Express and SATA/SAS applications.

Integrated Interface Blocks for PCI Express Designs

Highlights of the integrated blocks for PCI Express include:

- Compliant to the PCI Express Base Specification 2.1 or 3.0 (depending of family) with Endpoint and Root Port capability
- Supports Gen1 (2.5 Gb/s), Gen2 (5 Gb/s), and Gen3 (8 Gb/s) depending on device family
- Advanced configuration options, Advanced Error Reporting (AER), and End-to-End CRC (ECRC) Advanced Error Reporting and ECRC features
- Multiple-function and single root I/O virtualization (SR-IOV) support enabled through soft-logic wrappers or embedded in the integrated block depending on family

All Artix-7, Kintex-7, and Virtex-7 devices include at least one integrated block for PCI Express technology that can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 2.1 or 3.0. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom FPGA-to-FPGA communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA.

This block is highly configurable to system design requirements and can operate 1, 2, 4, or 8 lanes at the 2.5 Gb/s, 5.0 Gb/s, and 8.0 Gb/s data rates. For high-performance applications, advanced buffering techniques of the block offer a flexible

maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCI Express, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: lane width, maximum payload size, FPGA logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Xilinx offers two wrappers for the integrated block: AXI4-Stream and AXI4 (memory mapped). Note that legacy TRN/Local Link is not available in 7 series devices for the integrated block for PCI Express. AXI4-Stream is designed for existing customers of the integrated block and enables easy migration to AXI4-Stream from TRN. AXI4 (memory mapped) is designed for Xilinx Platform Studio/EDK design flow and MicroBlaze™ processor based designs.

More information and documentation on solutions for PCI Express designs can be found at: http://www.xilinx.com/products/technology/pci-express.html.

Configuration

There are many advanced configuration features, including:

- High-speed SPI and BPI (parallel NOR) configuration
- Built-in MultiBoot and safe-update capability
- 256-bit AES encryption with HMAC/SHA-256 authentication
- Built-in SEU detection and correction
- Partial reconfiguration

Xilinx 7 series FPGAs store their customized configuration in SRAM-type internal latches. There are up to 450 Mb configuration bits, depending on device size and user-design implementation options. The configuration storage is volatile and must be reloaded whenever the FPGA is powered up. This storage can also be reloaded at any time by pulling the PROGRAM_B pin Low. Several methods and data formats for loading configuration are available, determined by the three mode pins.

The SPI interface (x1, x2, and x4 modes) and the BPI interface (parallel-NOR x8 and x16) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, and x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on. Some configuration options such as BPI are not supported in all device-package combinations. Refer to UG470, *7 Series FPGAs Configuration User Guide* for details.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide are also supported by the FPGA that are especially useful for processor-driven configuration.

The FPGA has the ability to reconfigure itself with a different image using SPI or BPI flash, eliminating the need for an external controller. The FPGA can reload its original design in case there are any errors in the data transmission, ensuring an operational FPGA at the end of the process. This is especially useful for updates to a design after the end product has been shipped. Customers can ship their products with an early version of the design, thus getting their products to market faster. This feature allows customers to keep their end users current with the most up-to-date designs while the product is already in the field.

The dynamic reconfiguration port (DRP) gives the system designer easy access to the configuration and status registers of the MMCM, PLL, XADC, transceivers, and integrated block for PCI Express. The DRP behaves like a set of memory-mapped registers, accessing and modifying block-specific configuration bits as well as status and control registers.

Encryption, Readback, and Partial Reconfiguration

In all 7 series FPGAs (except XC7S6 and XC7S15), the FPGA bitstream, which contains sensitive customer IP, can be protected with 256-bit AES encryption and HMAC/SHA-256 authentication to prevent unauthorized copying of the design. The FPGA performs decryption on the fly during configuration using an internally stored 256-bit key. This key can reside in battery-backed RAM or in nonvolatile eFUSE bits.

Most configuration data can be read back without affecting the system's operation. Typically, configuration is an all-or-nothing operation, but Xilinx 7 series FPGAs support partial reconfiguration. This is an extremely powerful and flexible feature that allows the user to change portions of the FPGA while other portions remain static. Users can time-slice these portions to fit more IP into smaller devices, saving cost and power. Where applicable in certain designs, partial reconfiguration can greatly improve the versatility of the FPGA.

XADC (Analog-to-Digital Converter)

Highlights of the XADC architecture include:

- Dual 12-bit 1 MSPS analog-to-digital converters (ADCs)
- Up to 17 flexible and user-configurable analog inputs
- On-chip or external reference option
- On-chip temperature (±4°C max error) and power supply (±1% max error) sensors
- Continuous JTAG access to ADC measurements

All Xilinx 7 series FPGAs (except XC7S6 and XC7S15) integrate a new flexible analog interface called XADC. When combined with the programmable logic capability of the 7 series FPGAs, the XADC can address a broad range of data acquisition and monitoring requirements. For more information, go to: http://www.xilinx.com/ams.

The XADC contains two 12-bit 1 MSPS ADCs with separate track and hold amplifiers, an on-chip analog multiplexer (up to 17 external analog input channels supported), and on-chip thermal and supply sensors. The two ADCs can be configured to simultaneously sample two external-input analog channels. The track and hold amplifiers support a range of analog input signal types, including unipolar, bipolar, and differential. The analog inputs can support signal bandwidths of at least 500 KHz at sample rates of 1MSPS. It is possible to support higher analog bandwidths using external analog multiplexer mode with the dedicated analog input (see UG480, 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide).

The XADC optionally uses an on-chip reference circuit (±1%), thereby eliminating the need for any external active components for basic on-chip monitoring of temperature and power supply rails. To achieve the full 12-bit performance of the ADCs, an external 1.25V reference IC is recommended.

If the XADC is not instantiated in a design, then by default it digitizes the output of all on-chip sensors. The most recent measurement results (together with maximum and minimum readings) are stored in dedicated registers for access at any time via the JTAG interface. User-defined alarm thresholds can automatically indicate over-temperature events and unacceptable power supply variation. A user-specified limit (for example, 100°C) can be used to initiate an automatic powerdown.

7 Series FPGA Ordering Information

Table 12 shows the speed and temperature grades available in the different device families. Some devices might not be available in every speed and temperature grade.

Table 12: **7 Series Speed Grade and Temperature Ranges**

Device Family	Devices	Speed Grade, Temperature Range, and Operating Voltage			
		Commercial (C) 0°C to +85°C	Extended (E) 0°C to +100°C	Industrial (I) –40°C to +100°C	Expanded (Q) –40°C to +125°C
Spartan-7	All	-2C (1.0V)		-2I (1.0V)	
		-1C (1.0V)		-1I (1.0V)	-1Q (1.0V)
				-1LI (0.95V)	
Artix-7	All		-3E (1.0V)		
		-2C (1.0V)		-2I (1.0V)	
			-2LE (1.0V or 0.9V)		
		-1C (1.0V)		-1I (1.0V)	
				-1LI (0.95V)	
Kintex-7	XC7K70T		-3E (1.0V)		
		-2C (1.0V)		-2I (1.0V)	
			-2LE (1.0V or 0.9V)		
		-1C (1.0V)		-1I (1.0V)	
	XC7K160T XC7K325T XC7K355T XC7K410T XC7K420T XC7K480T		-3E (1.0V)		
		-2C (1.0V)		-2I (1.0V)	
			-2LE (1.0V or 0.9V)	-2LI (0.95V)	
		-1C (1.0V)		-1I (1.0V)	
Virtex-7 T	XC7V585T		-3E (1.0V)		
		-2C (1.0V)		-2I (1.0V)	
			-2LE (1.0V)		
		-1C (1.0V)		-1I (1.0V)	
	XC7V2000T	-2C (1.0V)			
			-2GE (1.0V)		
			-2LE (1.0V)		
		-1C (1.0V)		-1I (1.0V)	
Virtex-7 XT	XC7VX330T XC7VX415T XC7VX485T XC7VX550T XC7VX690T		-3E (1.0V)		
		-2C (1.0V)		-2I (1.0V)	
			-2LE (1.0V)		
		-1C (1.0V)		-1I (1.0V)	
	XC7VX980T	-2C (1.0V)			
			-2LE (1.0V)		
		-1C (1.0V)		-1I (1.0V)	
	XC7VX1140T	-2C (1.0V)			
			-2GE (1.0V)		
			-2LE (1.0V)		
		-1C (1.0V)		-1I (1.0V)	
Virtex-7 HT	All	-2C (1.0V)			
			-2GE (1.0V)		
			-2LE (1.0V)		
		-1C (1.0V)			

The Spartan-7 FPGA ordering information is shown in Figure 1. Refer to the Package Marking section of UG475, *7 Series FPGAs Packaging and Pinout* for a more detailed explanation of the device markings.

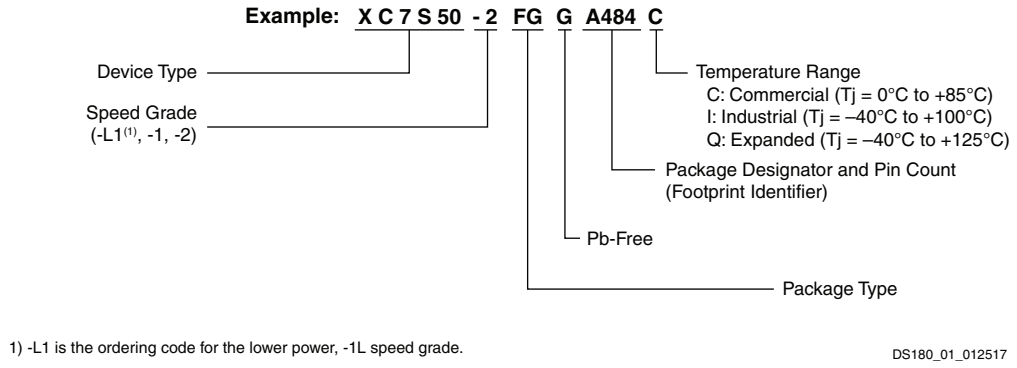


Figure 1: **Spartan-7 FPGA Ordering Information**

The Artix-7, Kintex-7, and Virtex-7 FPGA ordering information, shown in Figure 2, applies to all packages including Pb-Free. Refer to the Package Marking section of UG475, *7 Series FPGAs Packaging and Pinout* for a more detailed explanation of the device markings.

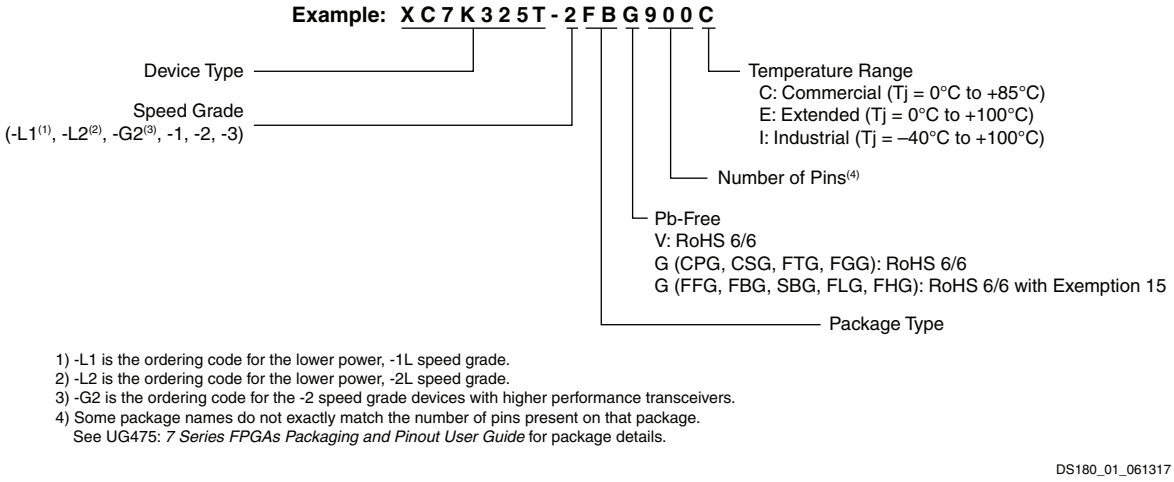


Figure 2: **Artix-7, Kintex-7, and Virtex-7 FPGA Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/21/10	1.0	Initial Xilinx release.
07/30/10	1.1	Added SHA-256 to authentication information. Updated Table 5, Table 7, Virtex-7 FPGA Device-Package Combinations and Maximum I/Os table (Virtex-7 T devices), and Table 9 with ball pitch information and voltage bank information. Updated DSP and Logic Slice information in Table 8. Updated Low-Power Gigabit Transceivers.
09/24/10	1.2	In General Description, updated 4.7 TMACS DSP to 5.0 TMACS DSP. In Table 1, added Note 1; updated Peak DSP Performance for Kintex-7 and Virtex-7 families. In Table 4, updated CMT information for XC7A175T and XC7A355T. In Table 6, replaced XC7K120T with XC7K160T and replaced XC7K230T with XC7K325T—and updated corresponding information. Also added XC7K355T, XC7K420T, and XC7K480T. In Table 7,replaced XC7K230T with XC7K325T. In Table 8, updated XC7V450T Logic Cell, CLB, block RAM, and PCI information; updated XC7VX415T and XC7VX690T PCI information; updated XC7V1500T, and XC7V2000T block RAM information; and replaced XC7VX605T with XC7VX575T, replaced XC7VX895T with XC7VX850T, and replaced XC7VX910T with XC7VX865T—and updated corresponding information. Updated Digital Signal Processing — DSP Slice with operating speed of 640 MHz. Removed specific transceiver type from Out-of-Band Signaling. In Virtex-7 FPGA Device-Package Combinations and Maximum I/Os table (Virtex-7 T devices), replaced XC7VX605T with XC7VX575T and added table notes 2 and 3. In Table 9, removed the FFG784 package for the XC7VX485T device; replaced XC7VX605T with XC7VX575T; replaced XC7VX895T with XC7VX850T; and replaced XC7VX910T with XC7VX865T.
10/20/10	1.3	In Table 7, replaced XC7K120T with XC7K160T. Updated Digital Signal Processing — DSP Slice.
11/17/10	1.4	Updated maximum I/O bandwidth to 3.1 Tb/s in General Description. Updated Peak Transceiver Speed for Virtex-7 FPGAs in Summary of 7 Series FPGA Features and in Table 1. Updated Peak DSP Performance values in Table 1 and Digital Signal Processing — DSP Slice. In Table 7, updated XC7K70T I/O information. In Table 8, added XC7VH290T, XC7VH580T, and XC7VH870T devices and updated total I/O banks information for the XC7V585T, XC7V855T, XC7V1500T, and XC7VX865T devices. In Table 9, updated XC7VX415T, XC7VX485T, XC7VX690T, XC7VX850T, and XC7VX865T device information. Added Table 11. Updated Low-Power Gigabit Transceivers information, including the addition of the GTZ transceivers.
02/22/11	1.5	Updated Summary of 7 Series FPGA Features and the Low-Power Gigabit Transceivers highlights and section. In Table 1, updated Kintex-7 FPGA, Artix-7 FPGA information. In Table 4, updated XC7A175T. Also, updated XC7A355T. Added three Artix-7 FPGA packages to Table 5: SBG325, SBG484, and FBG485, changed package from FGG784 to FBG784, and updated package information for XC7A175T and XC7A355T devices. In Table 6, updated XC7K160T and added three devices: XC7K355T, XC7K420T, and XC7K480T. In Table 7, updated XC7K70T package information and added three devices: XC7K355T, XC7K420T, and XC7K480T. In Table 8, added note 1 (EasyPath FPGAs) and updated note 7 to include GTZ transceivers. In Virtex-7 FPGA Device-Package Combinations and Maximum I/Os table (Virtex-7 T devices), added two Virtex-7 FPGA packages: FHG1157 and FHG1761, and updated XC7V1500T (no FFG1157) and XC7V2000T (no FFG1761) package information and removed the associated notes. Added CLBs, Slices, and LUTs. Updated Input/Output. Added EasyPath-7 FPGAs.
03/28/11	1.6	Updated General Description, Summary of 7 Series FPGA Features, Table 1, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9 (combined Virtex-7 T and XT devices in one table), and Table 11. Updated the Low-Power Gigabit Transceivers highlights and section. Updated Block RAM, Integrated Interface Blocks for PCI Express Designs, Configuration, Encryption, Readback, and Partial Reconfiguration, XADC (Analog-to-Digital Converter), 7 Series FPGA Ordering Information, and EasyPath-7 FPGAs.
07/06/11	1.7	Updated General Description, Summary of 7 Series FPGA Features, Table 1, Table 4, Table 6, Table 8, Table 9 and Table 11. Added Table 10. Added Stacked Silicon Interconnect (SSI) Technology. Updated Transmitter, Configuration, and XADC (Analog-to-Digital Converter). Updated Figure 1.
09/13/11	1.8	Updated General Description, Table 1, Table 4, Table 5, Table 8, CLBs, Slices, and LUTs, Configuration, and 7 Series FPGA Ordering Information.
01/15/12	1.9	Updated General Description, Table 1, Table 4, Table 5, Table 6, Table 7, Table 8, Table 10, Table 11, Block RAM, Digital Signal Processing — DSP Slice, Low-Power Gigabit Transceivers, Integrated Interface Blocks for PCI Express Designs, Configuration, EasyPath-7 FPGAs, and 7 Series FPGA Ordering Information.

Date	Version	Description of Revisions
03/02/12	1.10	Updated General Description, Table 5, and Table 12.
05/02/12	1.11	Updated Table 7, Table 9, Table 10, Low-Power Gigabit Transceivers, and 7 Series FPGA Ordering Information. Added 7 Series FPGA Ordering Information.
10/15/12	1.12	Updated overview with Artix-7 SL and SLT devices. Updated Table 1, Table 4, Table 5, Table 8, Table 9, Table 10, Table 11, and Table 12. Added Table 3. Updated Regional Clocks, Block RAM, Integrated Interface Blocks for PCI Express Designs, Configuration, and 7 Series FPGA Ordering Information.
11/30/12	1.13	Updated notes in Table 4 and Table 12. Updated XADC (Analog-to-Digital Converter).
07/29/13	1.14	Removed SL and SLT devices. Updated General Description, Table 4, Table 5, notes in Table 6 and Table 8, Regional Clocks, Input/Output, Low-Power Gigabit Transceivers, Integrated Interface Blocks for PCI Express Designs, Configuration, and 7 Series FPGA Ordering Information. Removed previous Table 3.
02/18/14	1.15	Changed document classification to Product Specification from Preliminary Product Specification. Updated HR I/O information for XC7A35T and XC7A50T in Table 5. Updated XC7VH870T I/O information in Table 8. Updated Table 11.
10/08/14	1.16	Added XC7A15T to Table 4 and Table 5. Removed HCG1931 and HCG1932 from Table 11. Updated Input/Output Delay; Block RAM; Configuration; I/O Clocks; and Updated Table 12 and Figure 1.
12/17/14	1.16.1	Typographical edit.
05/27/15	1.17	Updated Table 5, Table 7, Table 9, Table 10, Table 11, and Figure 1.
09/27/16	2.0	Added Spartan-7 devices throughout document, including Table 1, Table 2, Table 3, and Table 12. Added two Artix-7 devices XC7A12T and XC7A25T throughout document, including Table 4, Table 5, and Table 12. Updated General Description; Figure 1, Table 7, Regional Clocks, Block RAM, Integrated Interface Blocks for PCI Express Designs, Configuration, Encryption, Readback, and Partial Reconfiguration, and XADC (Analog-to-Digital Converter).
10/20/16	2.1	Updated Table 5.
12/15/16	2.2	Updated Table 3.
03/17/17	2.3	Updated Table 1, Table 5, Table 7, Table 9, Table 10, Table 12, and I/O Electrical Characteristics.
03/28/17	2.4	Updated Table 7.
08/01/17	2.5	Updated Table 5 and Figure 2.
02/27/18	2.6	Added MicroBlaze CPU information to the Summary of 7 Series FPGA Features and Table 1.
09/08/20	2.6.1	Editorial updates.

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