

NAU88C22 Demo Board User Manual

The PCB name: EVB-NAU88C22YG_V1.0

Ordering P/N: NL-NAU88C22

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1 OVERVIEW

The NAU88C22 is a low power, high quality CODEC for portable and general purpose audio applications. In addition to precision 24-bit stereo ADCs and DACs, this device integrates a broad range of additional functions to simplify implementation of complete audio system solutions. The NAU88C22 includes drivers for speaker, headphone, and differential or stereo line outputs, and integrates preamps for stereo differential microphones, significantly reducing external component requirements. Also, a fractional PLL is available to accurately generate any audio sample rate for the CODEC using any commonly available system clock from 8MHz through 33MHz.

2.1 Top View

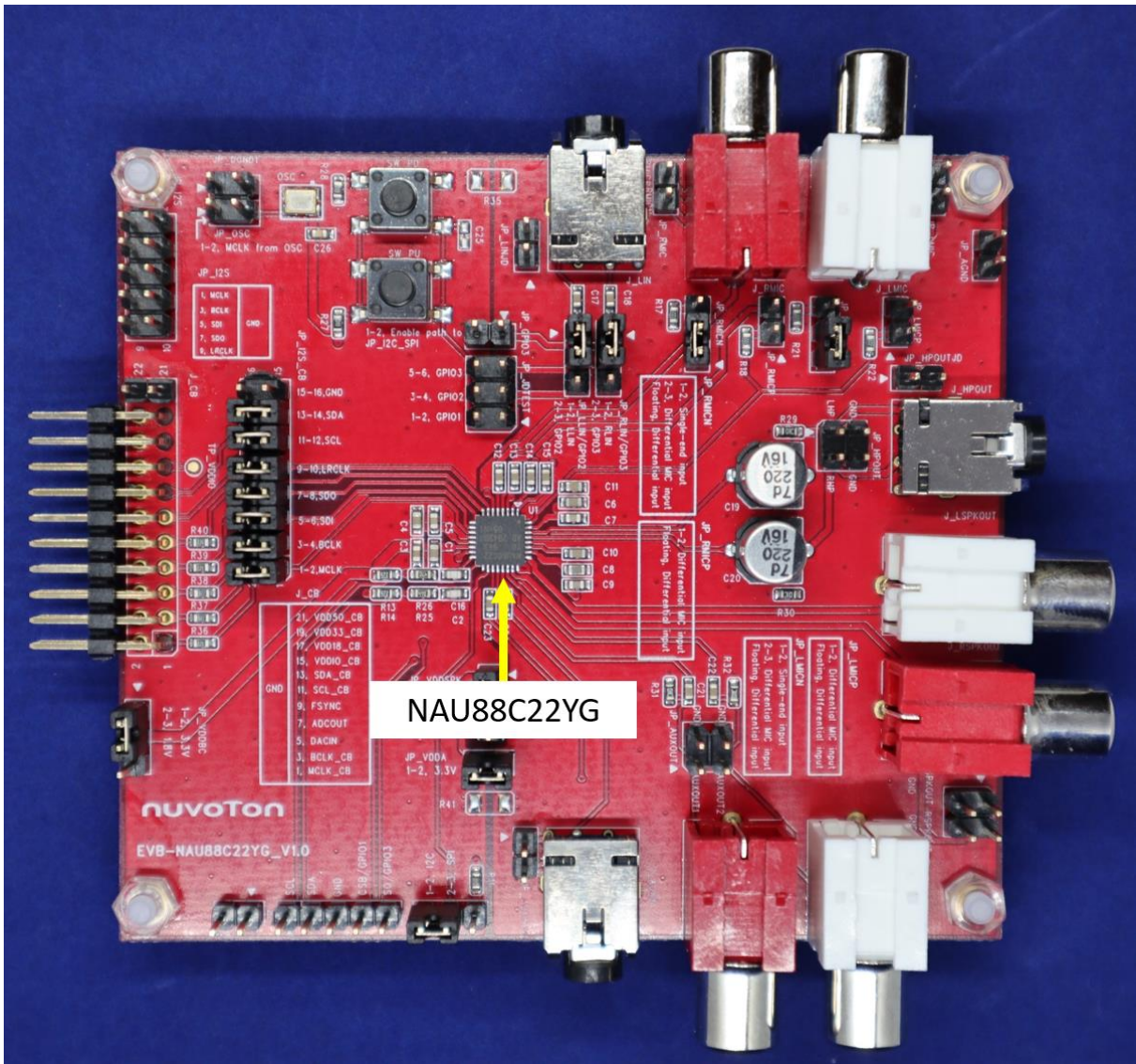


Figure 2.1-1 Top View

Name	Description
NAU88C22YG	Audio CODEC

Table 2.1-1 Main Components

2.2 Input / Output

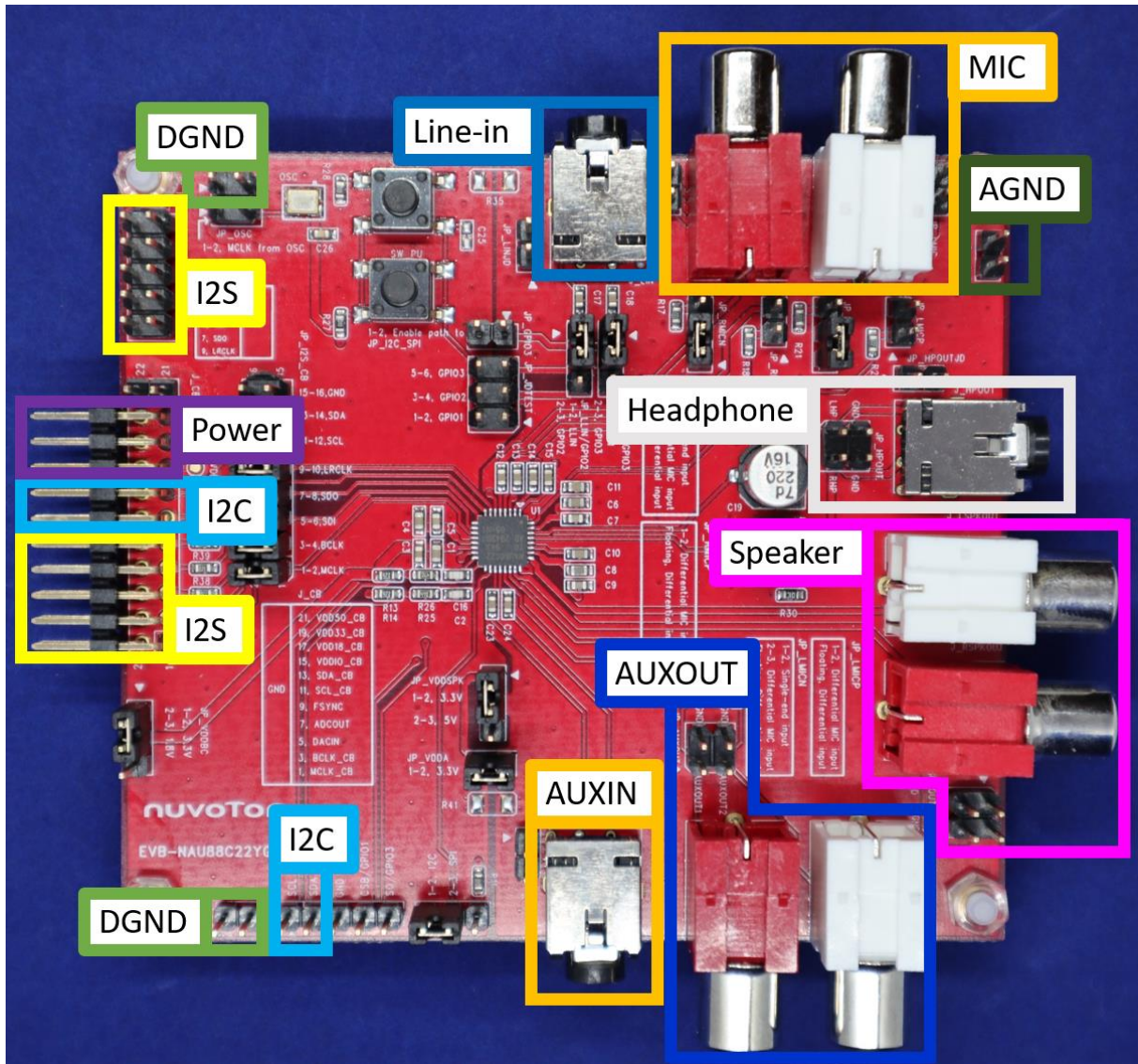


Figure 2.2-1 Input / Output

Name	Description																											
J_CB	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Pin 1</td> <td rowspan="5" style="width: 20%; text-align: center; vertical-align: middle;">I2S Interface</td> <td style="width: 35%;">MCLK, Master Clock</td> <td style="width: 15%;">Pin 11</td> <td rowspan="2" style="width: 15%; text-align: center; vertical-align: middle;">I2C Interface</td> <td style="width: 20%;">SDA</td> </tr> <tr> <td>Pin 3</td> <td>BCLK, Bit Clock</td> <td>Pin 13</td> <td>SCL</td> </tr> <tr> <td>Pin 5</td> <td>DACIN</td> <td>Pin15</td> <td rowspan="4" style="text-align: center; vertical-align: middle;">Power. Provide power to Demo board.</td> <td>VDDIO</td> </tr> <tr> <td>Pin 7</td> <td>ADCOUT</td> <td>Pin 17</td> <td>VDD1.8</td> </tr> <tr> <td>Pin 9</td> <td>FS ,Frame Sync</td> <td>Pin 19</td> <td>VDD3.3</td> </tr> <tr> <td></td> <td></td> <td>Pin 21</td> <td>VDD5</td> </tr> </table>	Pin 1	I2S Interface	MCLK, Master Clock	Pin 11	I2C Interface	SDA	Pin 3	BCLK, Bit Clock	Pin 13	SCL	Pin 5	DACIN	Pin15	Power. Provide power to Demo board.	VDDIO	Pin 7	ADCOUT	Pin 17	VDD1.8	Pin 9	FS ,Frame Sync	Pin 19	VDD3.3			Pin 21	VDD5
Pin 1	I2S Interface	MCLK, Master Clock		Pin 11	I2C Interface		SDA																					
Pin 3		BCLK, Bit Clock		Pin 13		SCL																						
Pin 5		DACIN		Pin15	Power. Provide power to Demo board.	VDDIO																						
Pin 7		ADCOUT		Pin 17		VDD1.8																						
Pin 9		FS ,Frame Sync	Pin 19	VDD3.3																								
		Pin 21	VDD5																									
JP_I2S	<p>These pins can also be I2S interface</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Pin 1</td> <td style="width: 85%;">MCLK, Master Clock</td> </tr> <tr> <td>Pin 3</td> <td>BCLK, Bit Clock</td> </tr> <tr> <td>Pin 5</td> <td>DACIN</td> </tr> <tr> <td>Pin 7</td> <td>ADCOUT</td> </tr> <tr> <td>Pin 9</td> <td>FS ,Frame Sync</td> </tr> </table>	Pin 1	MCLK, Master Clock	Pin 3	BCLK, Bit Clock	Pin 5	DACIN	Pin 7	ADCOUT	Pin 9	FS ,Frame Sync																	
Pin 1	MCLK, Master Clock																											
Pin 3	BCLK, Bit Clock																											
Pin 5	DACIN																											
Pin 7	ADCOUT																											
Pin 9	FS ,Frame Sync																											
JP_I2C_SPI	<p>Pin1 and Pin2 are I2C interface. In addition, this connector can be an SPI interface.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Pin 1</td> <td style="width: 85%;">SDL</td> </tr> <tr> <td>Pin 2</td> <td>SCA</td> </tr> <tr> <td>Pin 3</td> <td>GND</td> </tr> <tr> <td>Pin 4</td> <td>CSB/GPIO1</td> </tr> <tr> <td>Pin 5</td> <td>RLIN/GPIO3</td> </tr> </table>	Pin 1	SDL	Pin 2	SCA	Pin 3	GND	Pin 4	CSB/GPIO1	Pin 5	RLIN/GPIO3																	
Pin 1	SDL																											
Pin 2	SCA																											
Pin 3	GND																											
Pin 4	CSB/GPIO1																											
Pin 5	RLIN/GPIO3																											
MIC	Microphone input.																											
Headphone	Headphone output.																											
Speaker	Speaker out.																											
AUXIN	Auxiliary input.																											
AUXOUT	Auxiliary output.																											

Table 2.2-1 Input / Output

2.3 Jumpers

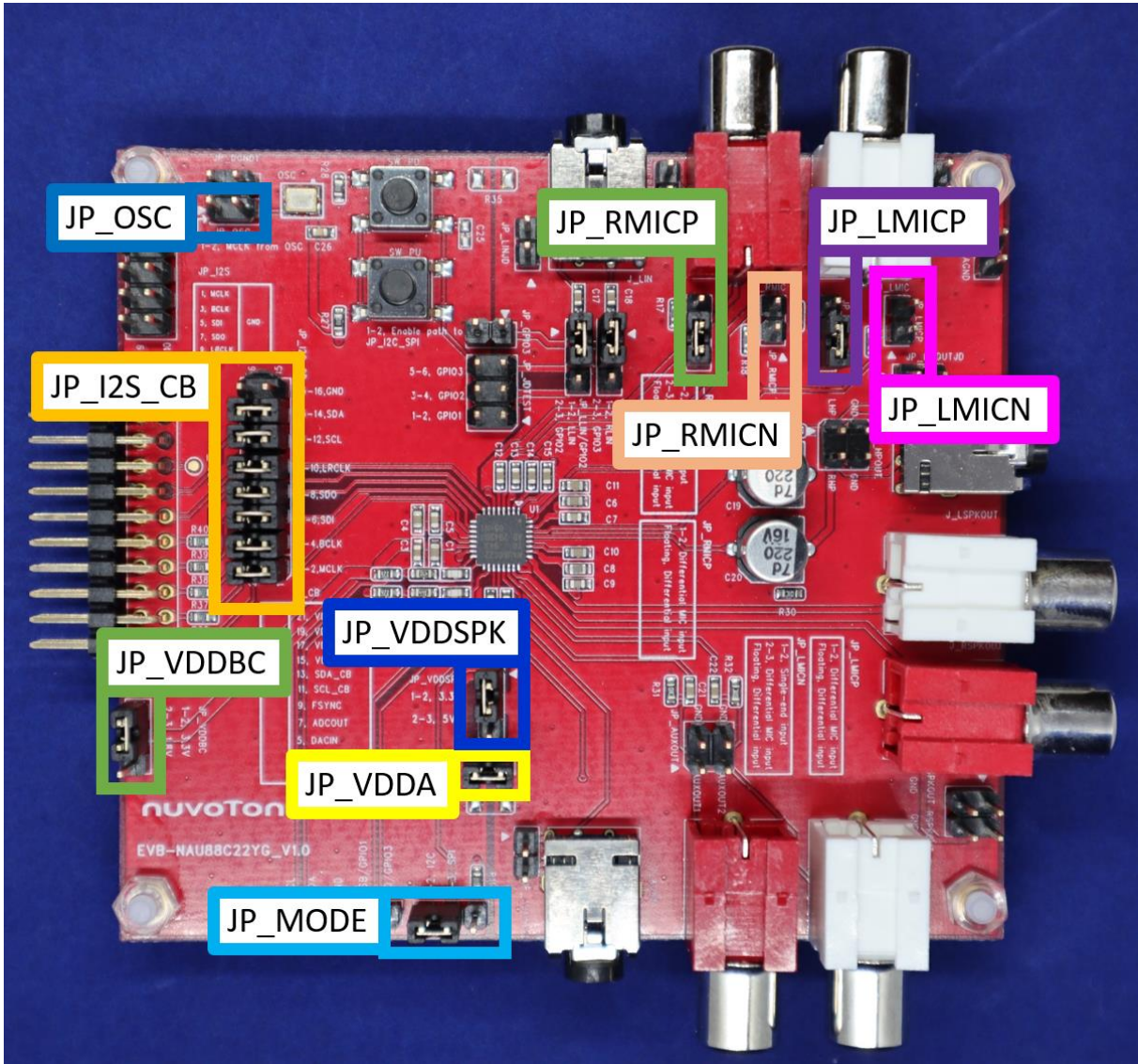
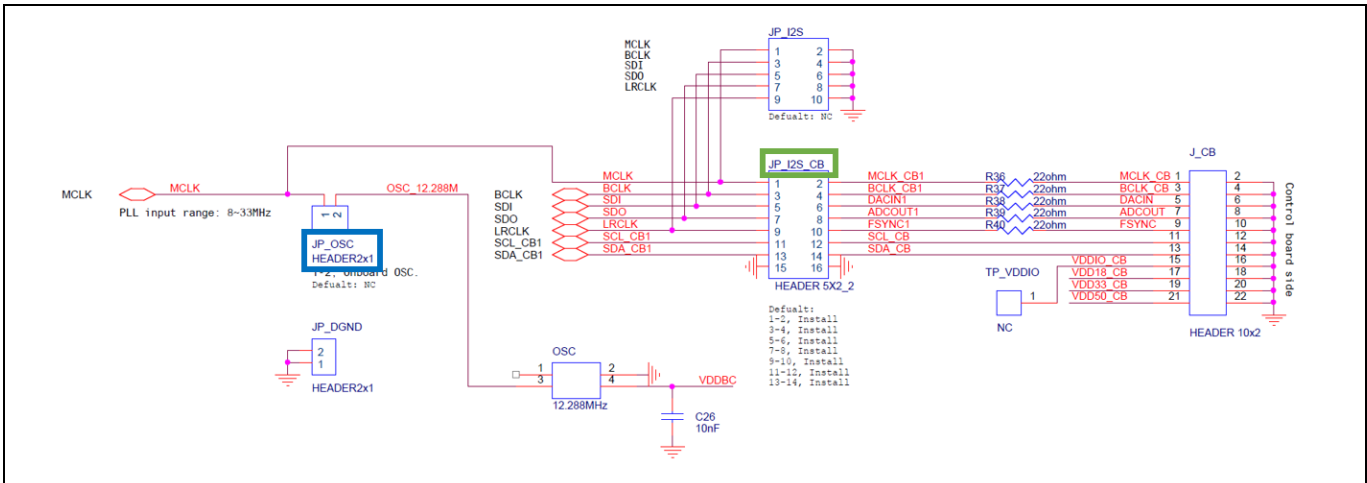


Figure 2.3-1 Jumpers

Name	Pin definition	Description						
JP_VDDBC	VDDDB and VDDC voltage selection	<table border="1"> <tr> <td>Short</td> <td>1-2 (default)</td> <td>2-3</td> </tr> <tr> <td>VDDBC</td> <td>VDDBC uses voltage of 3.3V</td> <td>VDDBC uses voltage of 3.3V</td> </tr> </table>	Short	1-2 (default)	2-3	VDDBC	VDDBC uses voltage of 3.3V	VDDBC uses voltage of 3.3V
Short	1-2 (default)	2-3						
VDDBC	VDDBC uses voltage of 3.3V	VDDBC uses voltage of 3.3V						
JP_VDDSPK	Speaker power supply voltage selection	<table border="1"> <tr> <td>Short</td> <td>1-2 (default)</td> <td>2-3</td> </tr> <tr> <td>VDDSPK</td> <td>VDDSPK uses voltage of 3.3V</td> <td>VDDSPK uses voltage of 5V</td> </tr> </table>	Short	1-2 (default)	2-3	VDDSPK	VDDSPK uses voltage of 3.3V	VDDSPK uses voltage of 5V
Short	1-2 (default)	2-3						
VDDSPK	VDDSPK uses voltage of 3.3V	VDDSPK uses voltage of 5V						
JP_VDDA	VDDA power source selection	<table border="1"> <tr> <td></td> <td>Short (default)</td> <td>Open</td> </tr> <tr> <td>VDDA</td> <td>Using power from JP_I2S_CB</td> <td>Can use external power to connect to pin2</td> </tr> </table>		Short (default)	Open	VDDA	Using power from JP_I2S_CB	Can use external power to connect to pin2
	Short (default)	Open						
VDDA	Using power from JP_I2S_CB	Can use external power to connect to pin2						



JP_I2S_CB	I2C and I2S signal selection		Short (default)	Open
		Pin 1-2 MCLK	Using signal from J_CB	Can use external signal to connect to pin1
		Pin 3-4 BCLK		Can use external signal to connect to pin3
		Pin 5-6 SDI		Can use external signal to connect to pin5
		Pin 7-8 SDO		Can use external signal to connect to pin7
		Pin 9-10 LRCLK		Can use external signal to connect to pin9
		Pin 11-12 SCL		Can use external signal to connect to pin11
		Pin 13-14 SDA		Can use external signal to connect to pin13
Pin 15-16 GNG				

JP_OSC	Onboard OSC selection		Short	Open (default)
		VDDA	<p>MCLK signal source is Onboard OSC</p> <p>Note : If you want to use Onboard OSC, you need to make sure that J_CB has no signal input, or open JP_I2S_CB pin1-2</p>	MCLK signal source is JP_I2S_CB

JP_LMICP	Left Mic channel source selection														
JP_LMICN		<table border="1" data-bbox="667 737 1385 846"> <tr> <td></td> <td>Short</td> <td>Open (default)</td> </tr> <tr> <td>JP_LMICP</td> <td>MIC input</td> <td>Differential input</td> </tr> </table> <table border="1" data-bbox="581 873 1471 1014"> <tr> <td></td> <td>Short 1-2 (default)</td> <td>Short 2-3</td> <td>Open</td> </tr> <tr> <td>JP_LMICN</td> <td>Sing-end input</td> <td>MIC input</td> <td>Differential input</td> </tr> </table>		Short	Open (default)	JP_LMICP	MIC input	Differential input		Short 1-2 (default)	Short 2-3	Open	JP_LMICN	Sing-end input	MIC input
	Short	Open (default)													
JP_LMICP	MIC input	Differential input													
	Short 1-2 (default)	Short 2-3	Open												
JP_LMICN	Sing-end input	MIC input	Differential input												
JP_RMICP	Right Mic channel source selection														
JP_RMICN		<table border="1" data-bbox="667 1537 1385 1646"> <tr> <td></td> <td>Short</td> <td>Open (default)</td> </tr> <tr> <td>JP_LMICP</td> <td>MIC input</td> <td>Differential input</td> </tr> </table> <table border="1" data-bbox="581 1673 1471 1814"> <tr> <td></td> <td>Short 1-2 (default)</td> <td>Short 2-3</td> <td>Open</td> </tr> <tr> <td>JP_LMICN</td> <td>Sing-end input</td> <td>MIC input</td> <td>Differential input</td> </tr> </table>		Short	Open (default)	JP_LMICP	MIC input	Differential input		Short 1-2 (default)	Short 2-3	Open	JP_LMICN	Sing-end input	MIC input
	Short	Open (default)													
JP_LMICP	MIC input	Differential input													
	Short 1-2 (default)	Short 2-3	Open												
JP_LMICN	Sing-end input	MIC input	Differential input												

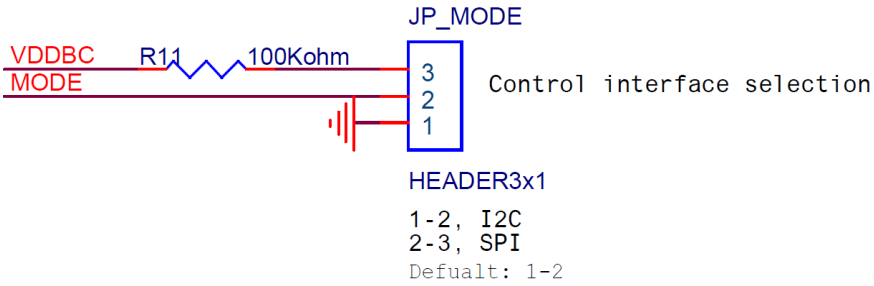
JP_MODE	Control interface selection	 <p>JP_MODE Control interface selection</p> <p>HEADER3x1 1-2, I2C 2-3, SPI Default: 1-2</p> <table border="1" data-bbox="662 577 1393 714"> <thead> <tr> <th></th> <th>Short (default)</th> <th>Open</th> </tr> </thead> <tbody> <tr> <td>VDDA</td> <td>Using power from JP_I2S_CB</td> <td>Can use external power to connect to pin2</td> </tr> </tbody> </table>		Short (default)	Open	VDDA	Using power from JP_I2S_CB	Can use external power to connect to pin2
	Short (default)	Open						
VDDA	Using power from JP_I2S_CB	Can use external power to connect to pin2						

Table 2.3-1 Jumpers

2.4 Schematic

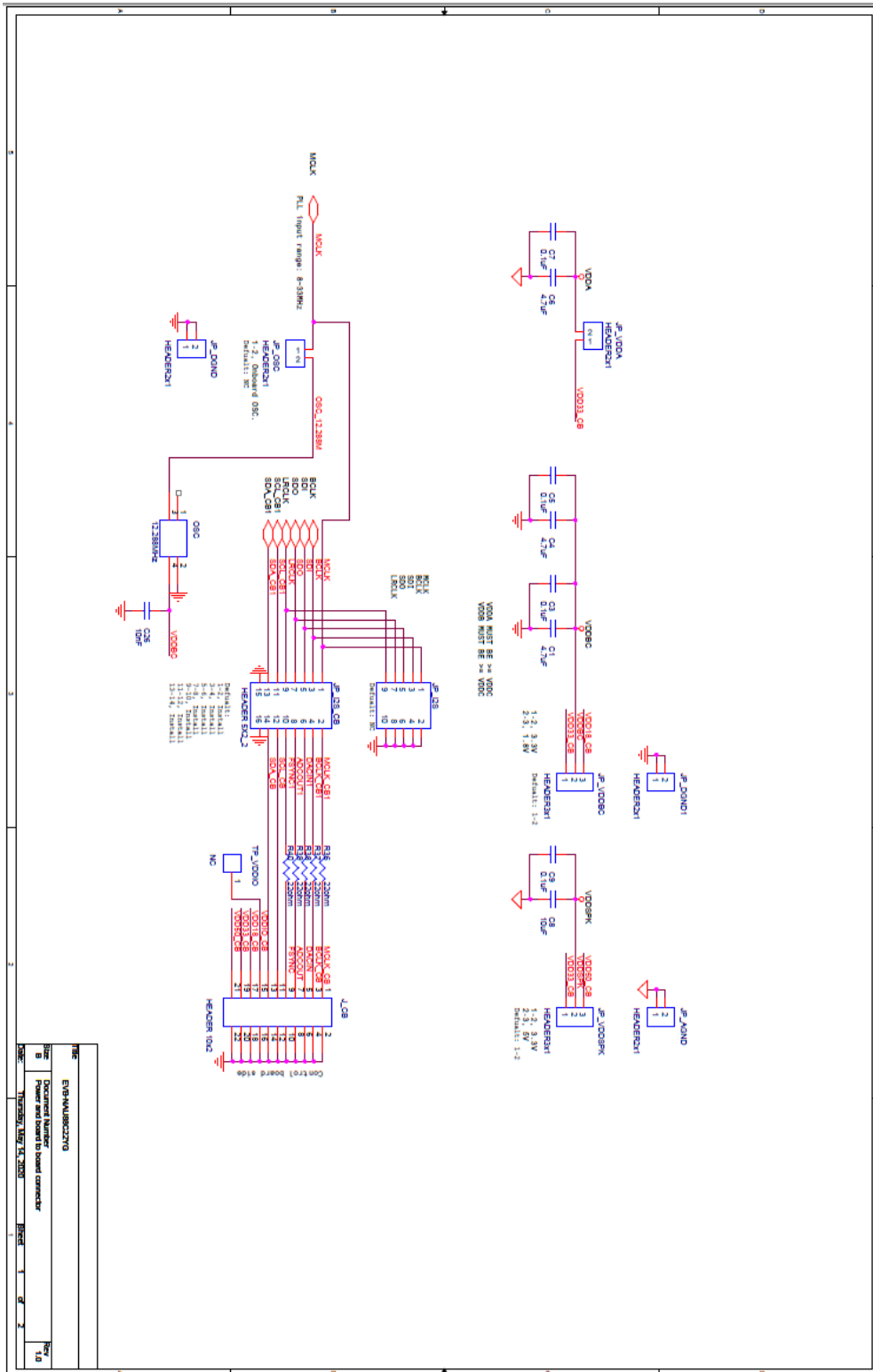


Figure 2.4-1 Schematic (page 1)

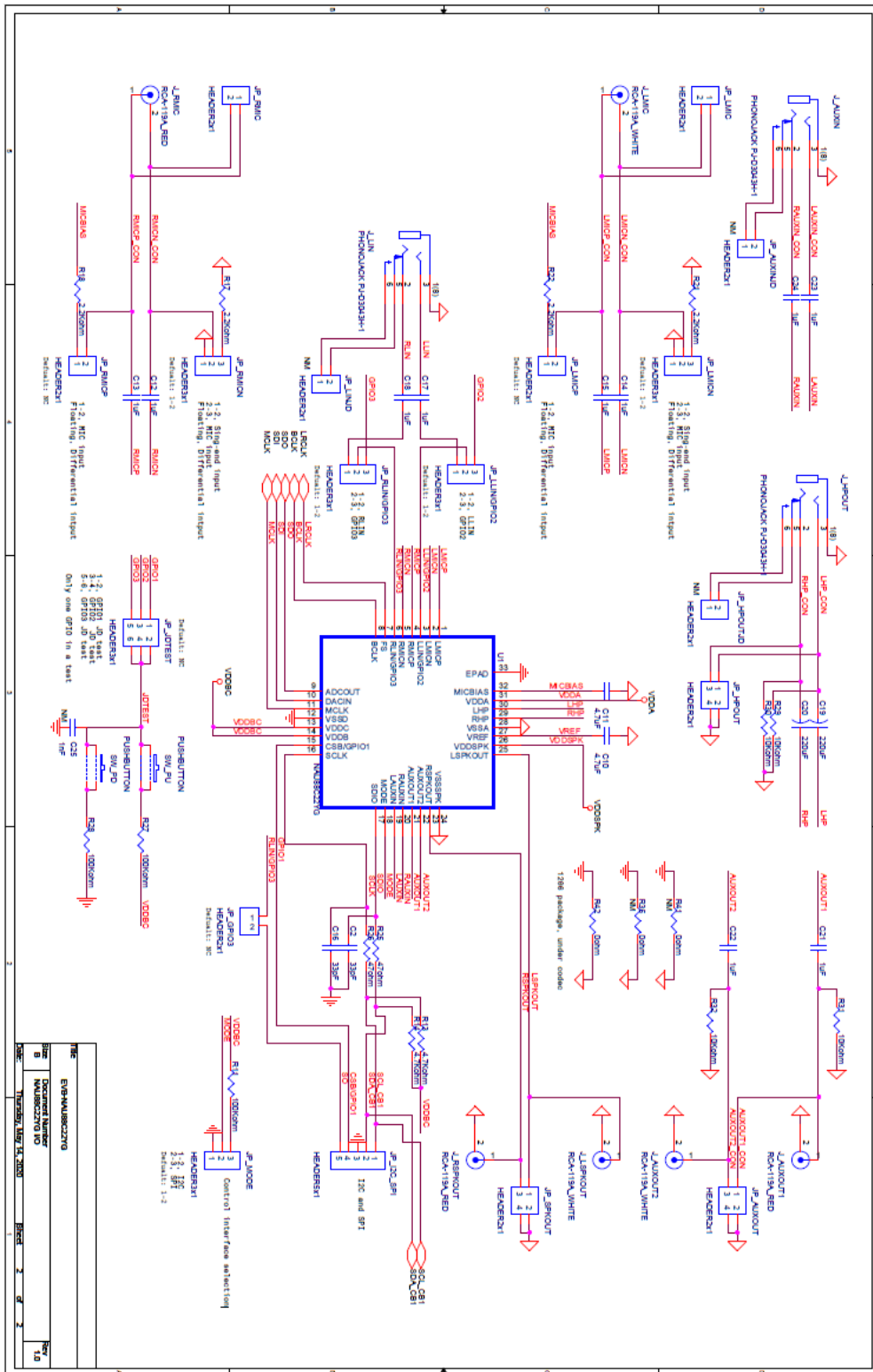


Figure 2.4-2 Schematic (page 2)

2.5 Bare Board

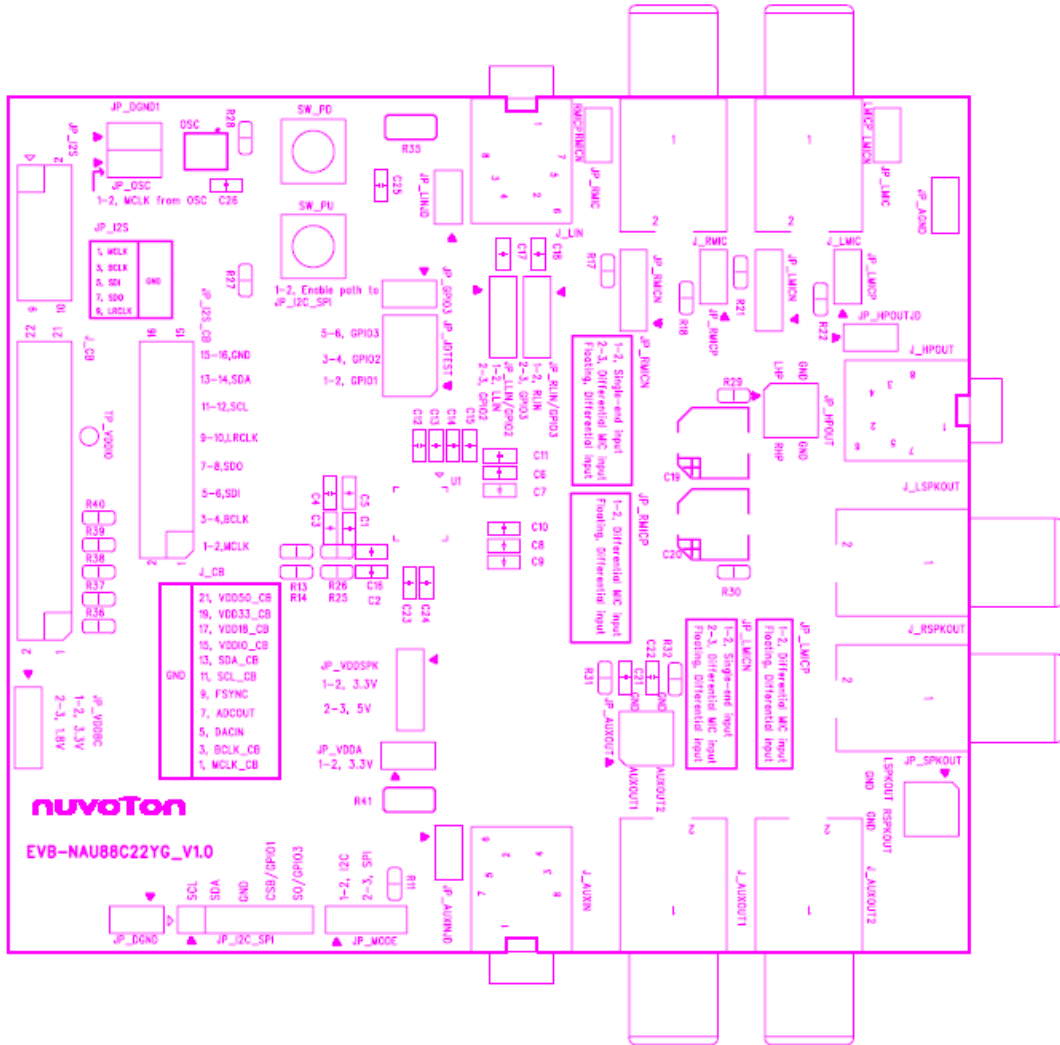


Figure 2.5-1 Top View of Bare Board

3 CONNECTED TO AUDIO CONTROL BOARD

If there is Nuvoton's Audio Control Board, NAU88C22 Demo Board can be used with Audio Control Board (USB_I2C_I2S_Control_Board_V1.1). When the Audio Control Board is connected to the NAU88C22 Demo Board, the PC or USB host can use the GUI to control the NAU88C22 Demo Board and know the status of the NAU88C22 Demo Board.

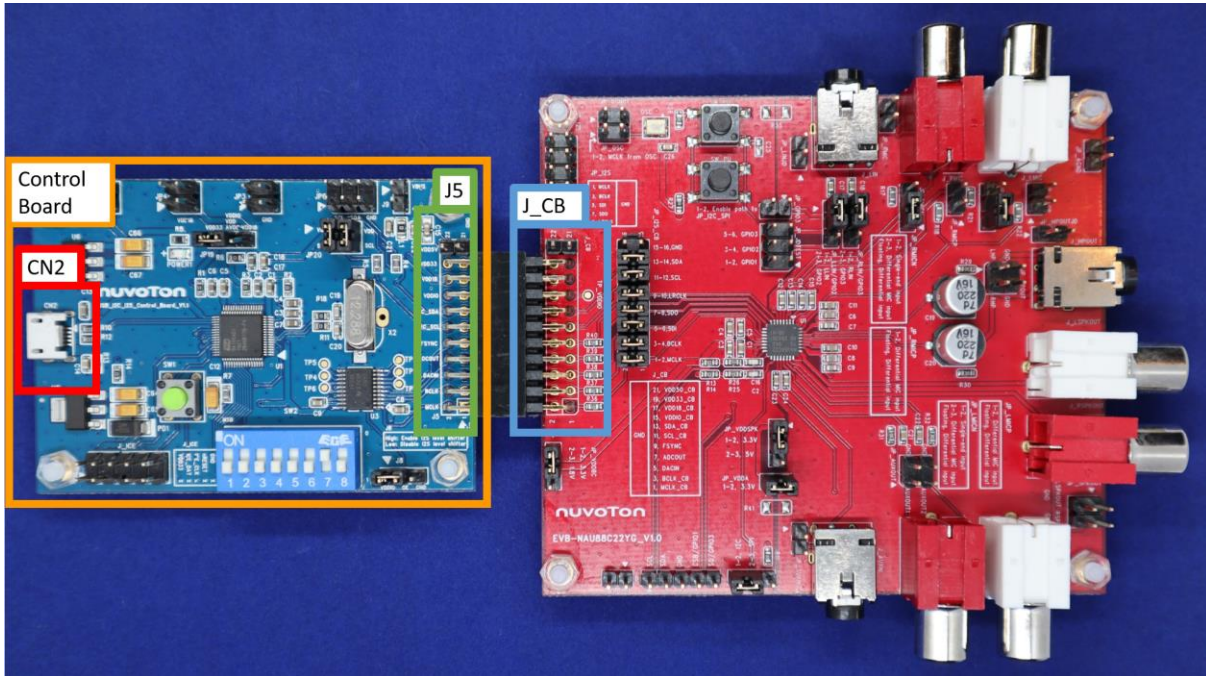


Figure 3-1 Connection Audio Control Board

Signal path:

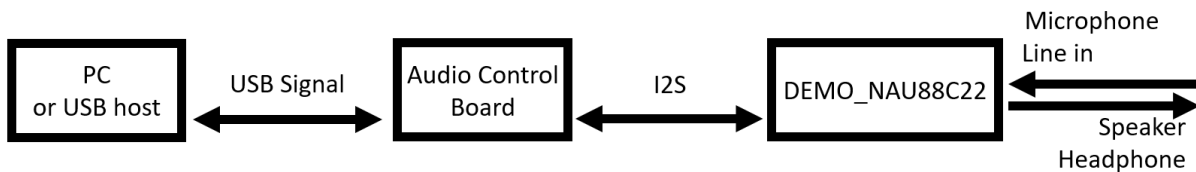


Figure 3-2 Signal Path

Board setting SOP:

Reference Figure 3-1

Step1: Connect J_CB of the NAU88C22 Demo Board to J5 of the Audio Control Board.

Step2: Connect CN2 of the Audio Control Board to PC or USB host via USB cable.

4 APPLICATION

4-1 SPI

3-wire

- a. JP_MODE 2-3 short

4-wire

- a. JP_MODE 2-3 short
- b. JP_GPIO3 1-2 short (for 4-wire SPI)
- c. JP_RLIN/GPIO3 NC (for 4-wire SPI)

4-2 RMICP and RMICN

Differential input

- a. JP_RMICN NC
- b. JP_RMICP NC

Single-end input

- a. JP_RMICN 1-2 short
- b. JP_RMICP NC

MIC input

- a. JP_RMICN 2-3 short
- b. JP_RMICP 1-2 short

4-3 LMICP and LMICN

Differential input

- a. JP_LMICN NC
- b. JP_LMICP NC

Single-end input

- a. JP_LMICN 1-2 short
- b. JP_LMICP NC

MIC input

- a. JP_LMICN 2-3 short
- b. JP_LMICP 1-2 short

4-4 Line level input

- a. JP_LLIN/GPIO2 1-2 short
- b. JP_RLIN/GPIO3 1-2 short

4-5 MCLKMCLK from control board

- a. JP_OSC NC
- b. JP_I2S_CB 1-2 short

External MCLK

- a. JP_OSC NC and the pin1 is the input for external clock source
- b. JP_DGND is the GND for the external clock source

Onboard OSC(12.288MHz)

- a. JP_OSC 1-2 short
- b. JP_I2S_CB 1-2 NC

5 REVISION HISTORY

Date	Revision	Description
2021.05.25	1.0	1 st version release

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