XIAMEN PRECISE DISPLAY

SPECIFICATIONS FOR
LIQUID CRYSTAL DISPLAY

PART NUMBER:	PGM12864A-NSW-BBW-01
DATE:	2017.04.28

1.0 MECHANICAL SPECS

1. Overall Module Size	93.0mm(W) x70.0mm(H) x max15.0mm(D) for LED backlight version
2. Dot Size	0.48mm(W) x 0.48mm(H)
3. Dot Pitch	0.52mm(W) x 0.52mm(H)
4. Duty	1/64
5. Controller IC	NT7107, NT7108 (Or equivalent AIP31107E, AIP31108E)
6. LC Fluid Options	STN-Blue
7. Polarizer Options	Negative/Transmissive
8. Viewing Angle	6:00 o'clock
9. Backlight Options	LED backlight white
10. Temperature Range Options	Wide Temp. Range（Operating: -20ºC ~ 70ºC, Storage:-30ºC ~ 80ºC）

2.0 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Typ	Max	Unit
Operating temperature (Standard)	Top	0	-	50	ºC
Storage temperature (Standard)	Tst	-10	-	60	ºC
Operating temperature (Wide temperature)	Top	-20	-	70	ºC
Storage temperature (Wide temperature)	Tst	-30	-	80	ºC
Input voltage	Vin	Vss		Vdd	V
Supply voltage for logic	Vdd- Vss	2.7	-	5.5	V
Supply voltage for LCD drive	Vdd- Vo	8.0	8.7	9.5	V

3.0 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	Vdd	fosc=270kHz	4.5	5.0	5.5	V
Power Supply Current	Idd	Vdd=5.0V, fosc=270kHz	-	2.5	5.0	mA
Recommended LCD Voltage	Vdd - Vo	0ºC	-	8.9	9.5	V
		25ºC	8.5	8.7	9.0	
		50ºC	8.0	8.5	-	
LED Power Supply Voltage	Vfled	R=68Ω	-	5.0	5.5	V
LED Power Supply Current	Ifled	R=68Ω	-	-	40	mA

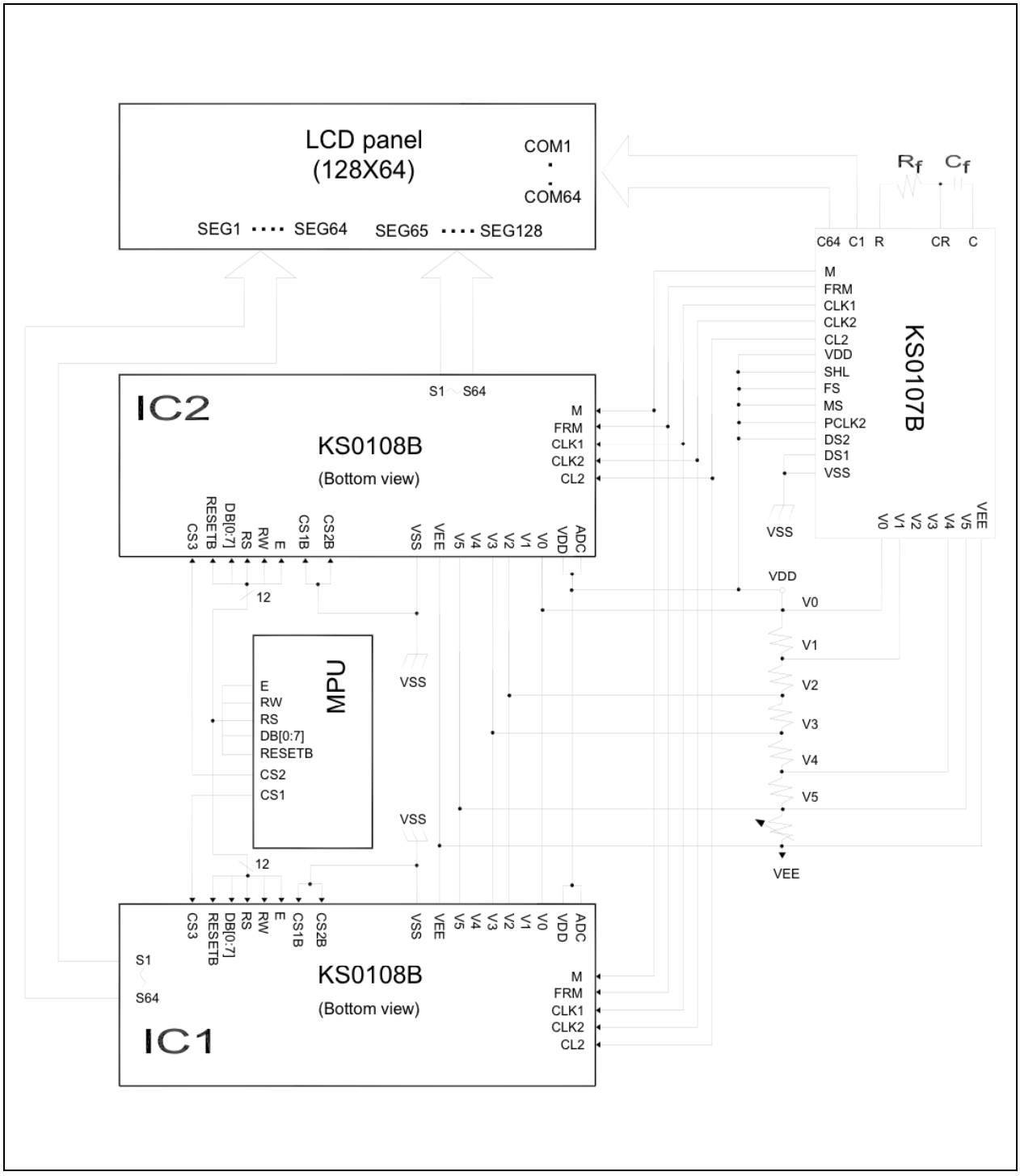
4.0 OPTICAL CHARACTERISTICS (Ta=25ºC, Vdd= 5.0V±0.25V, TN LC fluid)

Item	Symbol	Condition	Min	Typ	Max	Unit
Viewing angle (horizontal)	θ	Cr ≥ 4.0	-25	-	-	deg
Viewing angle (vertical)	ϕ	Cr ≥ 4.0	-30	-	30	deg
Contrast Ratio	Cr	ϕ=0°, θ=0°	-	2	-	
Response time (rise)	Tr	ϕ=0°, θ=0°	-	120	150	ms
Response time (fall)	Tf	ϕ=0°, θ=0°	-	120	150	ms

4.1 OPTICAL CHARACTERISTICS (Ta=25ºC, Vdd= 5.0V±0.25V, STN LC fluid)

Item	Symbol	Condition	Min	Typ	Max	Unit
Viewing angle (horizontal)	θ	Cr ≥ 2.0	-60	-	35	deg
Viewing angle (vertical)	ϕ	Cr ≥ 2.0	-40	-	40	deg
Contrast Ratio	Cr	ϕ=0°, θ=0°	-	6	-	
Response time (rise)	Tr	ϕ=0°, θ=0°	-	150	250	ms
Response time (fall)	Tf	ϕ=0°, θ=0°	-	150	250	ms

5.0 BLOCK DIAGRAM

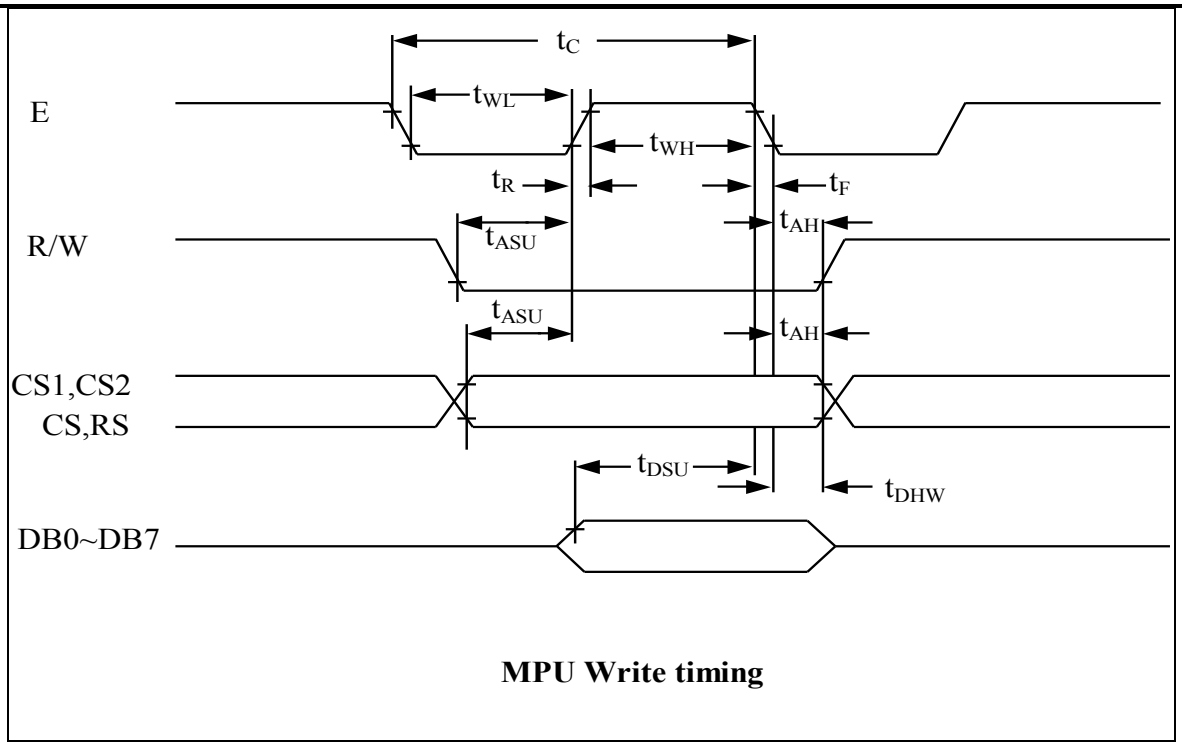


6.0 PIN ASSIGNMENT

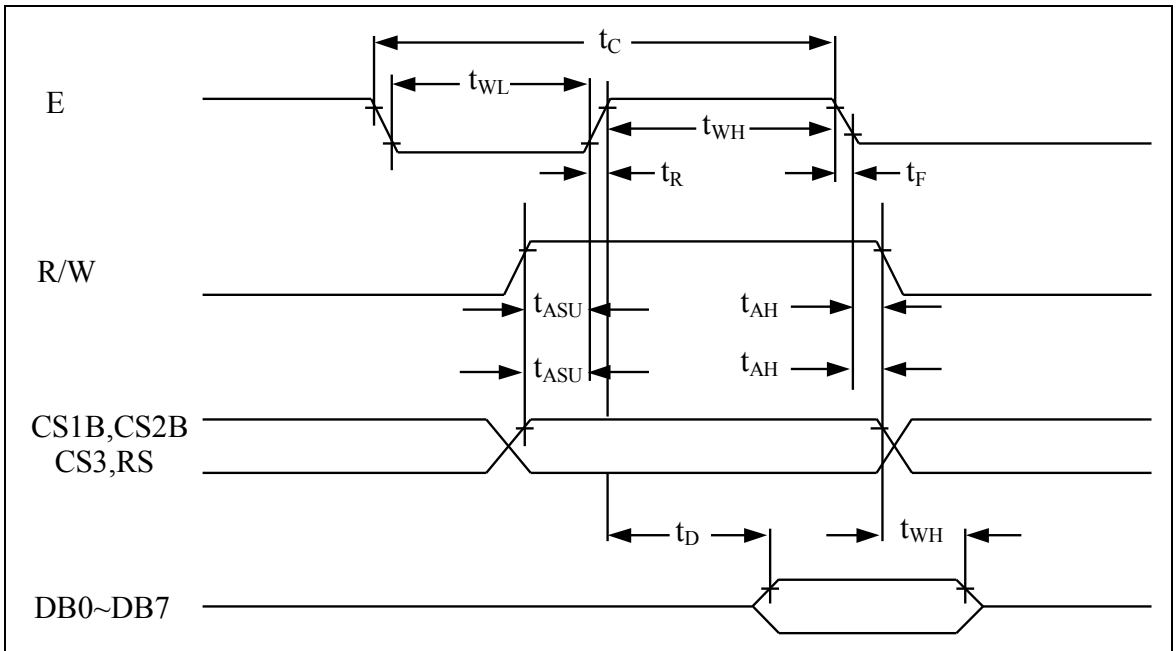
Pin No.	Symbol	Function
1	Vss	Ground
2	Vdd	+5V
3	Vo	LCD contrast adjust
4	D/I	Register select
5	R/W	Read / write
6	E	Enable
7~14	DB0~DB7	Data bus[0~7]bit
15	CS1	Select IC2 active high
16	CS2	Select IC2 active high
17	RESET	Reset signal active low
18	VEE	Negative voltage output
19	A	Power Supply for BL+
20	K	Power Supply for BL-

7. MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E Cycle	t_C	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	
E Low Level Width	t_{WL}	450	-	-	
E Rise Time	t_R	-	-	25	
E Fall Time	t_F	-	-	25	
Address Set-Up Time	t_{ASU}	140	-	-	
Address Hold Time	t_{AH}	10	-	-	
Data Set-Up Time	t_{SU}	200	-	-	
Data Delay Time	t_D	-	-	320	
Data Hold Time (Write)	t_{DHW}	10	-	-	
Data Hold Time (Read)	t_{DHR}	20	-	-	



MPU Write timing



MPU Read timing

8. OPERATING PRINCIPLES & METHODS

1. I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS!B-CS3.

2. Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.
When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3. Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H , RS=L, status data (busy check) can read out.
To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

4. Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.

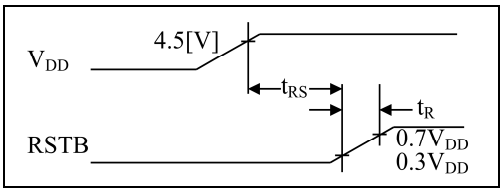
1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low, No instruction except status read can by accepted. Therefore, execute other instructions after making sure that DB4= (clear RSTB) and DB7=0 (ready) by status read instruction.

The conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

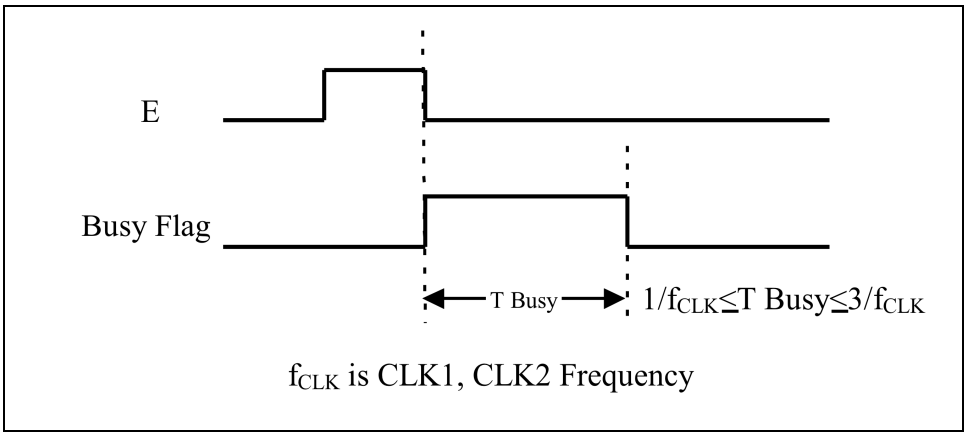
Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	-	-	us
Rise Time	t_R	-	-	200	ns



5. Busy flag

Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating . When busy flag is low, KS0108B can accept the data or instruction.

DB7indicates busy flag of the KS0108B.



6. Display On/Off Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data.
The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low.
The status of the flip-flop is output to DB5 by status read instruction.
The display on/off flip-flop synchronized by CL signal.

7. X Page Register

X page register designates pages of the internal display data RAM.
Count function is not available. An address is set by instruction.

8. Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

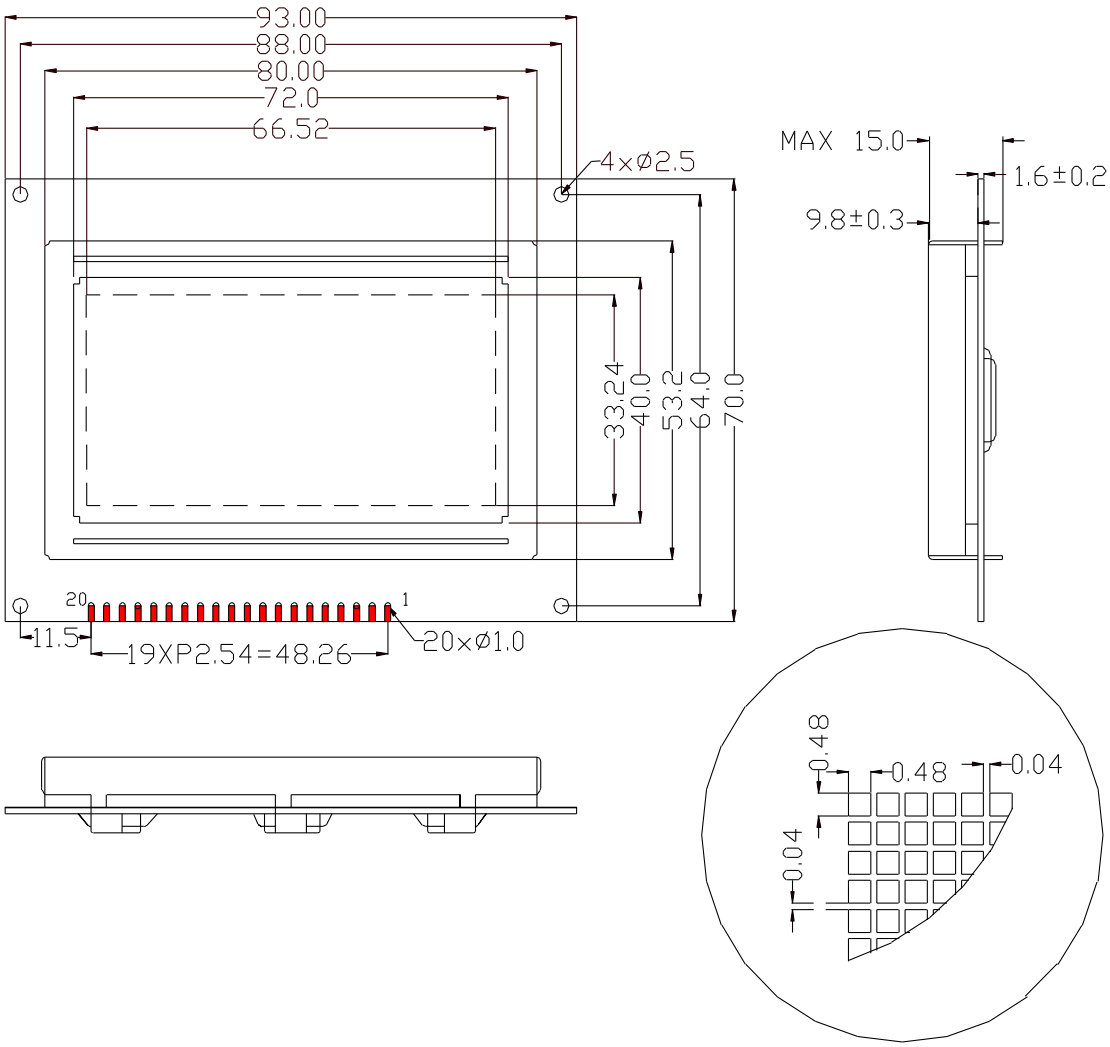
9. Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display , write datra1. The other way , off state, writes 0.
Display data RAM address and segment output can be controlled by ADC signal.
ADC=H => Y-address 0: S1~Y address 63: S64
ADC=L => Y-address 0: S64~Yaddress 63: S1
ADC terminal connect the V_{DD} or V_{SS}.

10. Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display.
Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.
It is used for scrolling of the liquid crystal display screen.

9.0 MECHANICAL DIAGRAM



10.0 RELIABILITY TEST

Storage Condition	Content	Evaluations and Assessment*			
		Current Consumption	Oozing	Contrast	Other Appearances
Operation at high temperature and humidity	40ºC,90% RH,240hrs	Twice initial value or less	none	More than 80% of initial value	No abnormality
High temperature storage	60ºC, 240hrs	Twice initial value or less	none	More than 80% of initial value	No abnormality
Low temperature storage	-20ºC, 240hrs	Twice initial value or less		More than 80% of initial value	No abnormality

*Evaluations and assessment to be made two hours after returning to room temperature (25ºC±5ºC).
*The LCDs subjected to the test must not have dew condensation.

11.0 Display Control Instruction

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instructions.

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Read Display Date	1	1	Read data								Reads data (DB[7:0]) from display data RAM to the data bus.
Write Display Date	1	0	Write data								Writes data (DB[7:0]) into the DDRAM. After writing instruction, Y address is incriminated by 1 automatically
Status Read	0	1	Busy	0	ON/ OFF	Re-set	0	0	0	0	Reads the internal status BUSY 0: Ready 1: In operation ON/OFF 0: Display ON 1: Display OFF RESET 0: Normal 1: Reset
Set Address (Y address)	0	0	0	1	Y address (0~63)						Sets the Y address at the column address counter
Set Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the Display Data RAM displayed at the top of the screen.
Set Address (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display On/off	0	0	0	0	1	1	1	1	1	0/1	Controls the display ON or OFF. The internal status and the DDRAM data is not affected. 0: OFF, 1: ON

1. Display On/Off

The display data appears when D is 1 and disappears when D is 0.
Though the data is not on the screen with D=0, it remains in the display data RAM.
Therefore, you can make it appear by changing D=0 into D=1.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

2. Set Address (Y Address)

Y address (AC0~AC5) of the display data RAM is set in the Y address counter.
An address is set by instruction and increased by 1 automatically by read or write operations of display data.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

3. Set Page (X Address)

X address (AC0~AC2) of the display data RAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page until the next page is set.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

4. Display Start Line (Z Address)

Z address (AC0~AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen.
When the display duty cycle is 1/64 or others (1/32~1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

5. Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY
  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.
  When BUSY is 0, the Chip is ready to accept any instructions.
- ON/OFF
  When ON/OFF is 1, the display is on.
  When ON/OFF is 0, the display is off.
- RESET
  When RESET is 1, the system is being initialized.
  In this condition, no instructions except status read can be accepted.
  When RESET is 0, initializing has finished and the system is in the usual operation condition.

6. Write Display Data

Writes data (D0~D7) into the display data RAM.
After writing instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

7. Read Display Data

Reads data (D0~D7) from the display data RAM.
After reading instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0