TLVx197-Q1 Automotive, High-Voltage, Precision, Rail-to-Rail In, Rail-to-Rail Out Op Amp

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Low offset voltage: ±500 µV (maximum)
- Low noise: 5.5 nV/$\sqrt{\text{Hz}}$ at 1 kHz
- High common-mode rejection: 140 dB
- Low bias current: ±5 pA
- Rail-to-rail input and output
- Wide bandwidth: 10-MHz GBW
- High slew rate: 20 V/µs
- Low quiescent current: 1 mA per amplifier
- Wide supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- EMI/RFI filtered inputs
- Differential input-voltage range to supply rail
- High capacitive load drive capability: 1 nF
- Industry-standard package:
  - Single channel in very small 8-pin VSSOP
  - Dual channel in 8-pin VSSOP
  - Quad channel in 14-pin TSSOP

2 Applications

- Inverter and motor control
- DC/DC converter
- On-board (OBC) and wireless charger
- Battery management system (BMS)

3 Description

The TLV197-Q1, TLV2197-Q1 and TLV4197-Q1 (TLVx197-Q1) family of devices are part of a new generation, of low-cost, 36-V, automotive-qualified, operational amplifiers. The TLVx197-Q1 family uses a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding.

Good dc precision and ac performance including rail-to-rail input/output, an optimized cost structure, and AEC-Q100 grade 1 qualification, make this family an excellent choice for low-side current-sensing and signal-conditioning applications in the automotive space.

More unique features, such as a differential input-voltage range to the supply rail, a high output current (±65 mA), a heavy capacitive load drive of up to 1 nF, and a high slew rate (20 V/µs), make these devices a robust, high-performance operational amplifier family for high-voltage automotive applications.

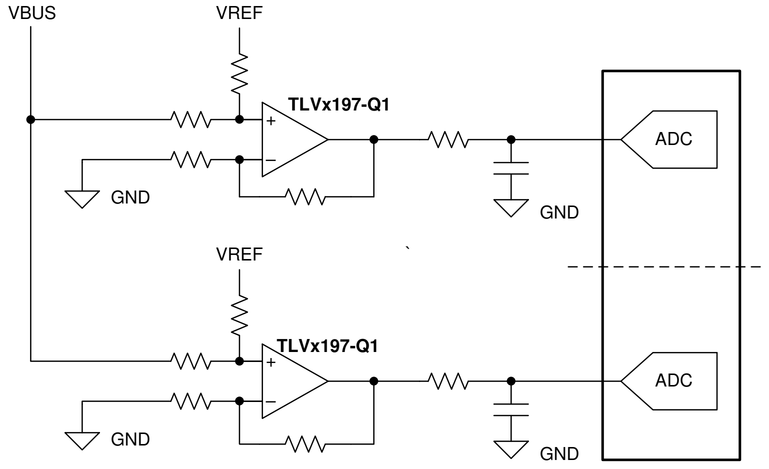
The TLVx197-Q1 family of op amps is available in standard packages and is specified from –40°C to +125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV197-Q1	VSSOP (8)	3.00 mm × 3.00 mm
TLV2197-Q1		
TLV4197-Q1	TSSOP (14)	5.00 mm x 4.40 mm

1. For all available packages, see the package option addendum at the end of the data sheet.

TLVx197-Q1 Detect Voltages in Automotive Applications



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4 Revision History

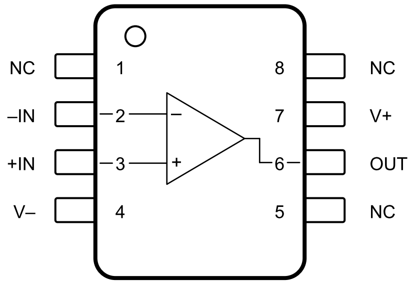
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2020) to Revision B	Page
• Changed TLV197-Q1 and TLV2197-Q1 from advance information (preview) to production data (active)	1

Changes from Original (April 2020) to Revision A	Page
• Changed to correct device names in titles for all *Thermal Information* tables	7

5 Pin Configuration and Functions

TLV197-Q1 DGK Package
8-Pin VSSOP
Top View



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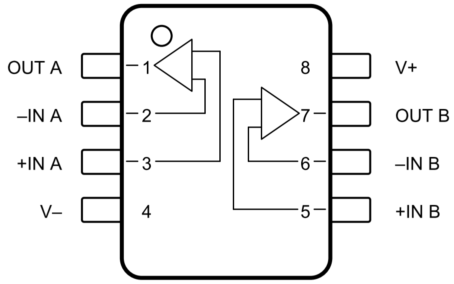
Pin Functions: TLV197-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	2	I	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	O	Output
V+	7	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

TLV2197-Q1 DGK Package
8-Pin VSSOP
Top View



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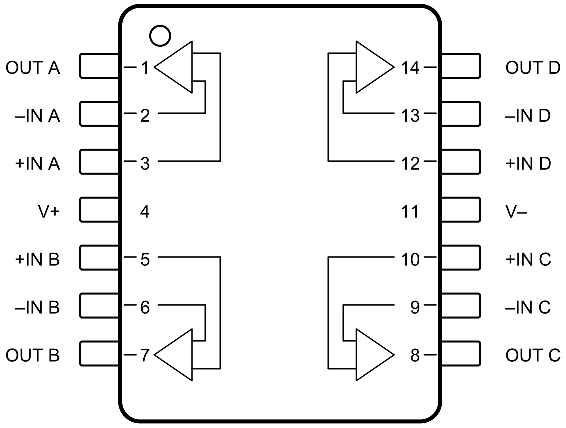
Pin Functions: TLV2197-Q1

PIN		I/O	DESCRIPTION
NAME	**NO.**		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

TLV4197-Q1 PW Package
14-Pin TSSOP
Top View



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Pin Functions: TLV4197-Q1

PIN		I/O	DESCRIPTION
NAME	**NO.**		
+IN A	3	I	Noninverting input, channel A
–IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+)		40	V
		Dual-supply, V_S = (V+) – (V–)		±20	
+IN, –IN	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
	Output short circuit(2)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	
T_{stg}	Storage temperature		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charge Device Model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+)	4.5		36	V
		Dual-supply, V_S = (V+) – (V–)	±2.25		±18	
T_A	Operating temperature		–40		125	°C

6.4 Thermal Information: TLV197-Q1

THERMAL METRIC[1]		TLV197-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A

(1) For more information about traditional and new thermal metrics, see the *Semiconductorand IC Package Thermal Metrics* application report.

6.5 Thermal Information: TLV2197-Q1

THERMAL METRIC[1]		TLV2197-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A

(1) For more information about traditional and new thermal metrics, see the *Semiconductorand IC Package Thermal Metrics* application report.

6.6 Thermal Information: TLV4197-Q1

THERMAL METRIC[1]		TLV4197-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A

(1) For more information about traditional and new thermal metrics, see the *Semiconductorand IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

at T_A = +25°C, $V_{CM} = V_{OUT} = V_S / 2$, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±500	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±1	±5	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±0.3	±1.0	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.3		μV_{PP}
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		4		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		nV/√Hz
			f = 1 kHz		5.5		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		
			f = 1 kHz		12.5		
i_n	Input current noise density	f = 1 kHz			1.5		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		120	140		dB
		(V–) < V_{CM} < (V+) – 3 V	T_A = –40°C to +125°C	114	126		
		(V+) – 1.5 V < V_{CM} < (V+)		100	120		
			T_A = –40°C to +125°C	86	100		
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF

Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

at T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ		120	134		dB
		(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ	T_A = –40°C to +125°C	114	126		
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ		126	140		
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ	T_A = –40°C to +125°C	120	134		
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	G = 1, 10-V step		1.4		µs
			G = 1, 5-V step		0.9		
		To 0.001%	G = 1, 10-V step		2.1		
t_s	Settling time		G = 1, 5-V step		1.8		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			0.2		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00008%		
	Crosstalk	TLV4197-Q1 at dc			150		dB
		TLV4197-Q1, f = 100 kHz			130		dB
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_L = 10 kΩ		95	110	
			R_L = 2 kΩ		430	500	
		Negative rail	No load		5	15	
			R_L = 10 kΩ		95	110	
			R_L = 2 kΩ		430	500	
I_{SC}	Short-circuit current				±65		mA
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.2	mA
			T_A = –40°C to +125°C			1.5	
TEMPERATURE							
	Thermal protection				140		°C

6.8 Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V)

at T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = (V+) – 3 V			±5	±500	µV
dV_{OS}/dT	Input offset voltage drift	V_{CM} = (V+) – 1.5 V			±1	±5	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±2		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.3		μV_{PP}
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		4		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		$nV/\sqrt{Hz}$
			f = 1 kHz		5.5		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		
			f = 1 kHz		12.5		
i_n	Input current noise density	f = 1 kHz			1.5		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		94	110		dB
		(V–) < V_{CM} < (V+) – 3 V	T_A = –40°C to +125°C	90	104		
		(V+) – 1.5 V < V_{CM} < (V+)		100	120		
			T_A = –40°C to +125°C	84	100		
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF

Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V) (continued)

at T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ		110	120		dB
		(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ	T_A = –40°C to +125°C	100	114		
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ		110	126		
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ	T_A = –40°C to +125°C	110	120		dB
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 5-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±3V, G = 1, 5-V step		1		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			0.2		µs
	Crosstalk	TLV4197-Q1 at dc			150		dB
		TLV4197-Q1, f = 100 kHz			130		dB
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_L = 10 kΩ		95	110	
			R_L = 2 kΩ		430	500	
		Negative rail	No load		5	15	
			R_L = 10 kΩ		95	110	
			R_L = 2 kΩ		430	500	
I_{SC}	Short-circuit current				±65		mA
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.2	mA
			T_A = –40°C to +125°C			1.5	
TEMPERATURE							
	Thermal protection				140		°C

6.9 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

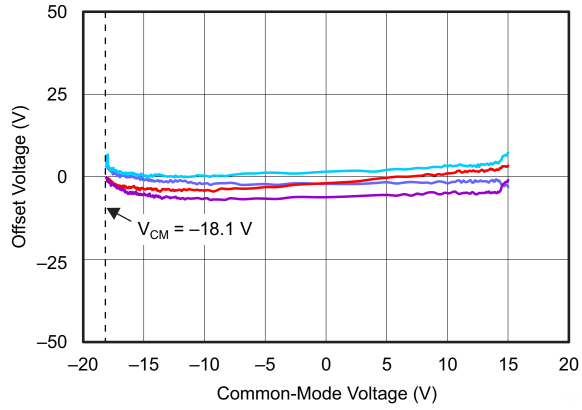


Figure 1. Offset Voltage vs Common-Mode Voltage

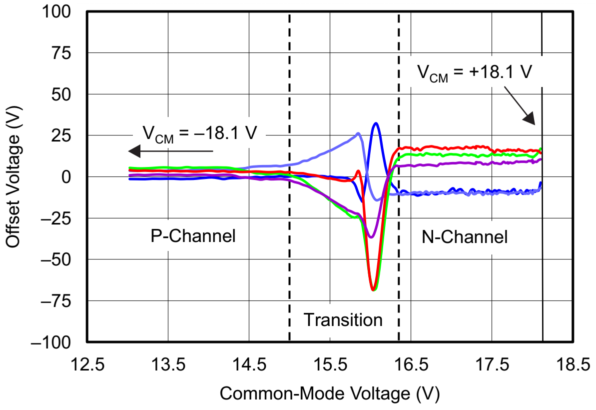
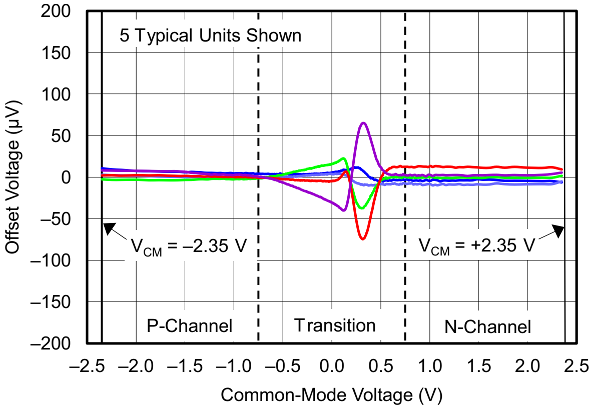
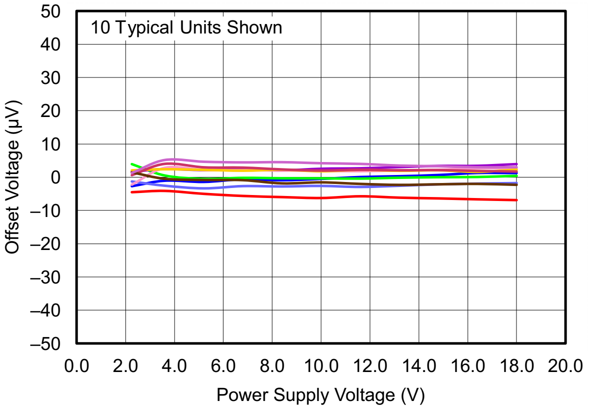


Figure 2. Offset Voltage vs Common-Mode Voltage



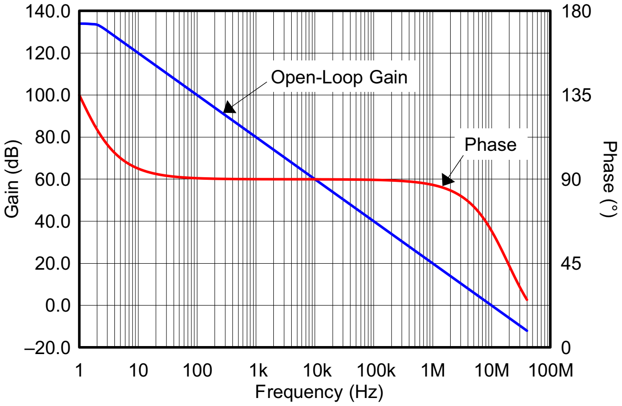
V_S = ±2.25 V

Figure 3. Offset Voltage vs Common-Mode Voltage



V_S = ±2.25 V to ±18 V

Figure 4. Offset Voltage vs Power Supply



C_{LOAD} = 15 pF

Figure 5. Open-Loop Gain and Phase vs Frequency

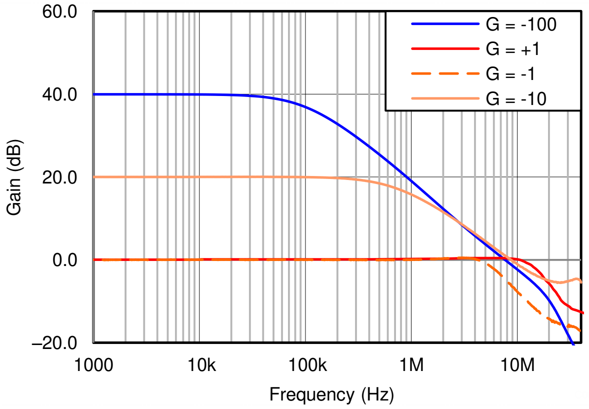


Figure 6. Closed-Loop Gain and Phase vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

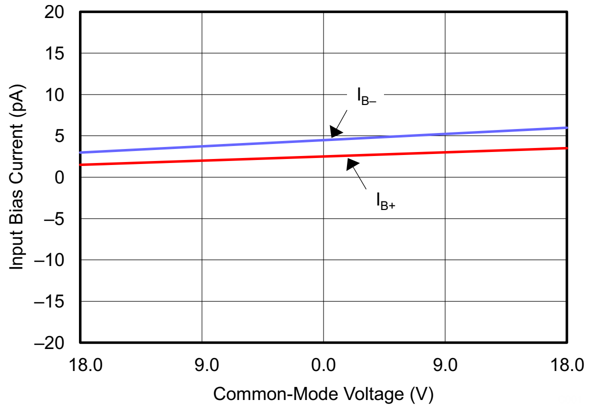


Figure 7. Input Bias Current vs Common-Mode Voltage

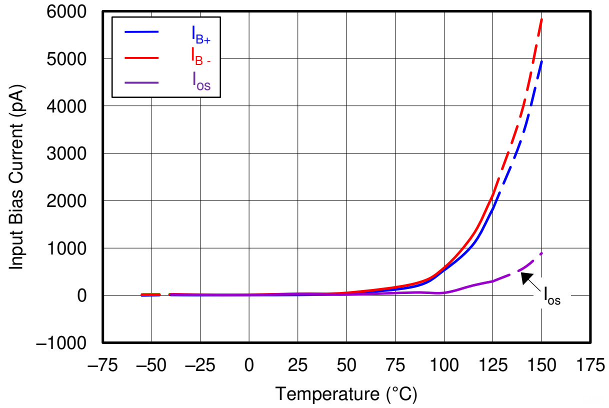


Figure 8. Input Bias Current vs Temperature

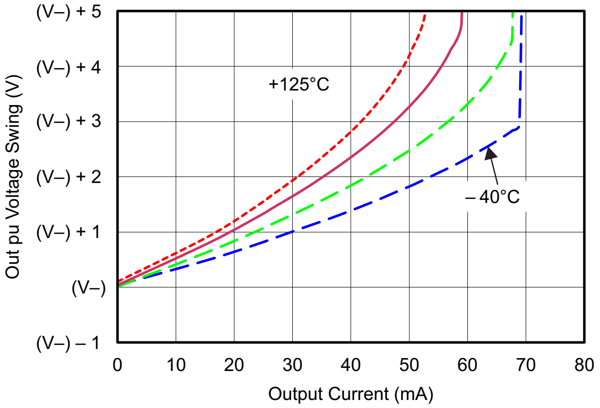


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

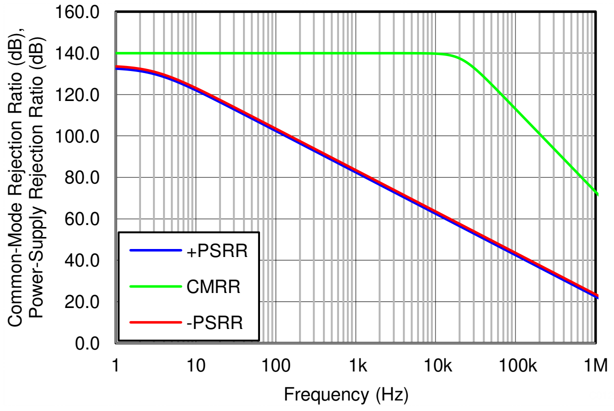


Figure 10. CMRR and PSRR vs Frequency

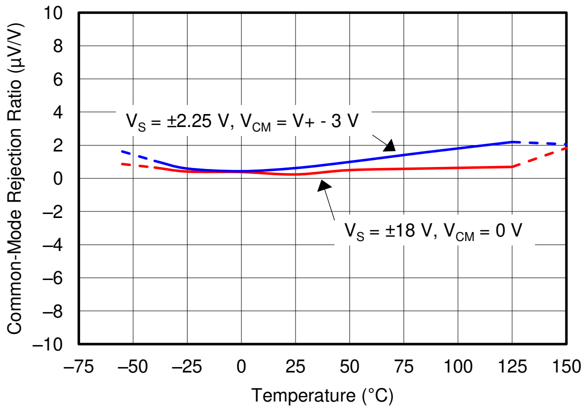


Figure 11. CMRR vs Temperature

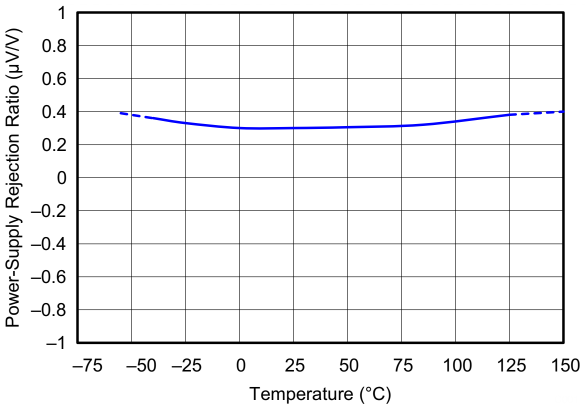


Figure 12. PSRR vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

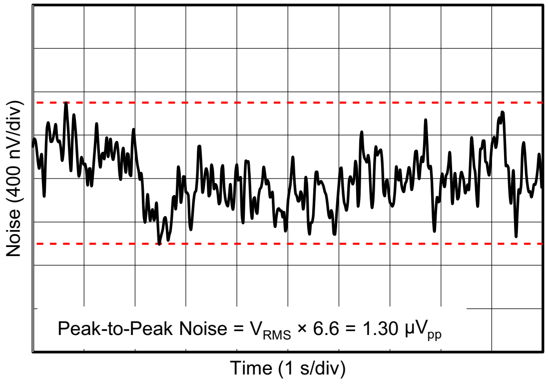


Figure 13. 0.1-Hz to 10-Hz Noise

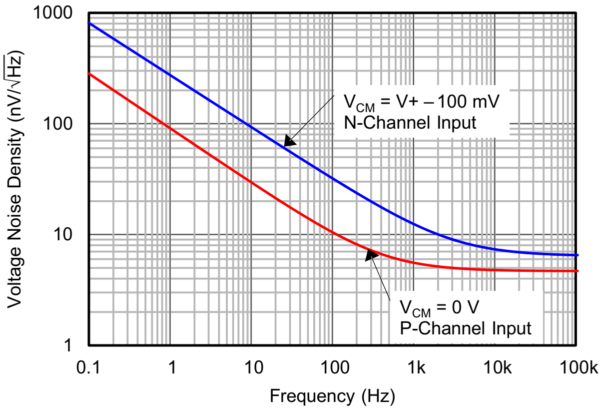
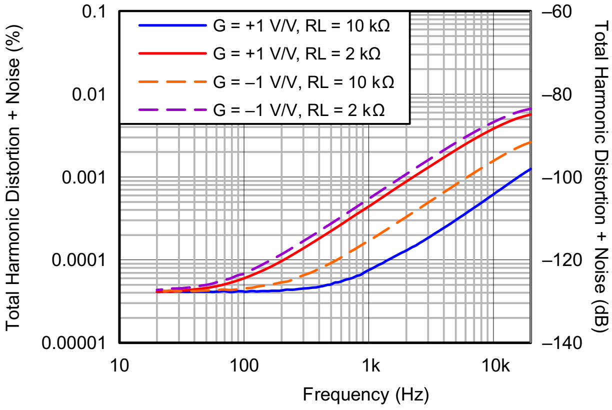
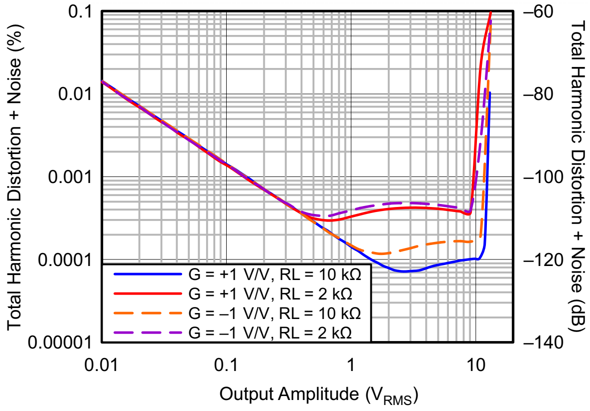


Figure 14. Input Voltage Noise Spectral Density vs Frequency



V_{OUT} = 3.5 V_{RMS}, BW = 80 kHz

Figure 15. THD+N Ratio vs Frequency



f = 1 kHz, BW = 80 kHz

Figure 16. THD+N vs Output Amplitude

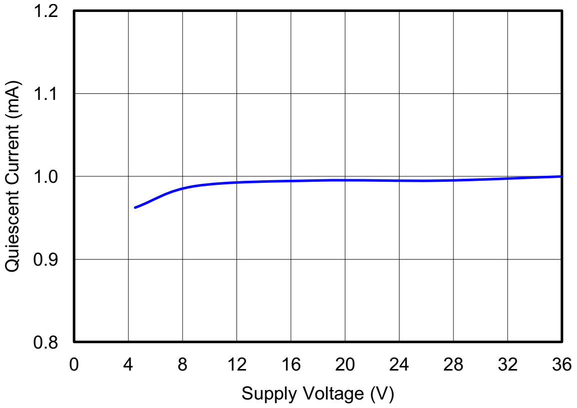


Figure 17. Quiescent Current vs Supply Voltage

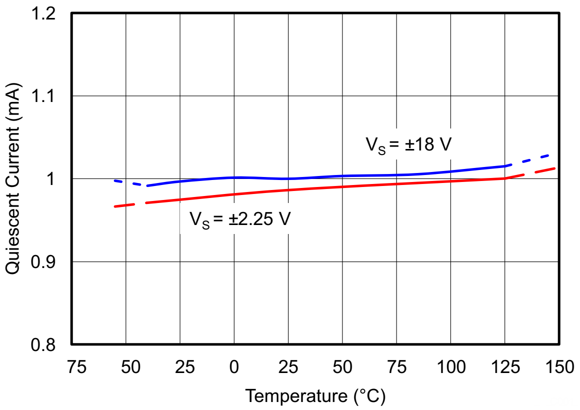
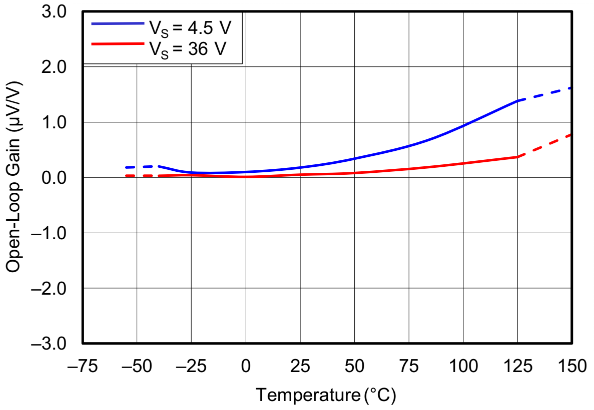


Figure 18. Quiescent Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



R_L = 10 kΩ

Figure 19. Open-Loop Gain vs Temperature

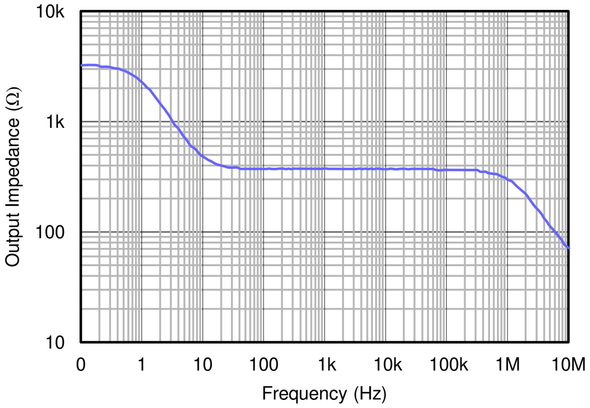
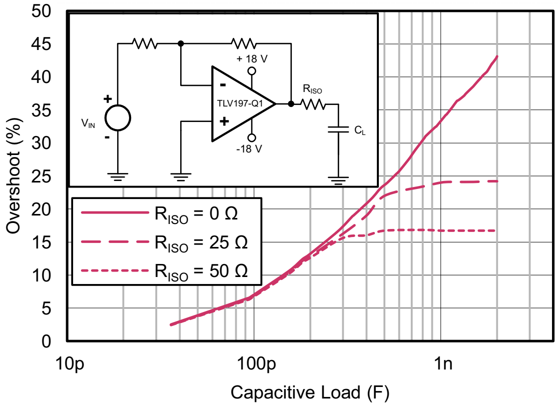
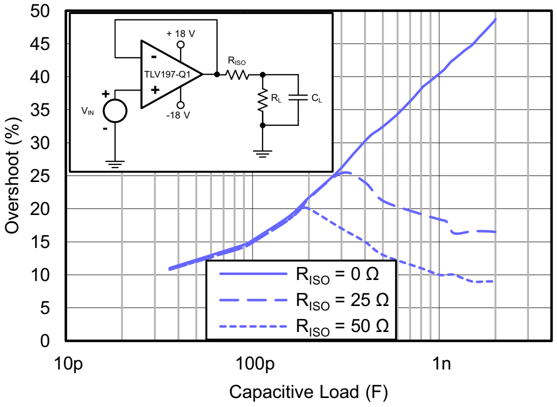


Figure 20. Open-Loop Output Impedance vs Frequency



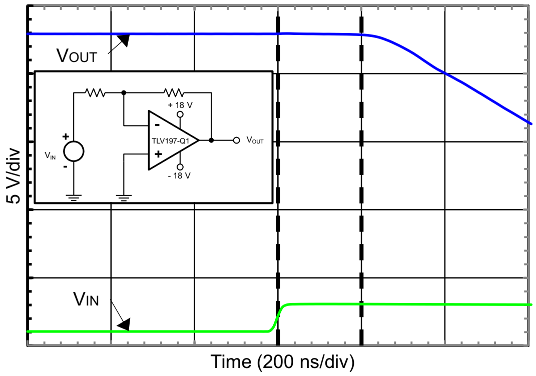
R_I = 1 kΩ, R_F = 1 kΩ, G = –1

Figure 21. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)



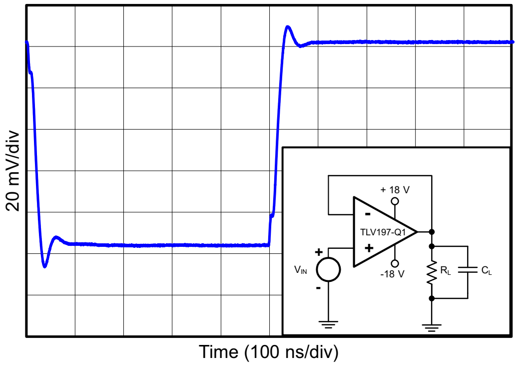
G = 1

Figure 22. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)



R_I = 1 kΩ, R_F = 10 kΩ, G = –10

Figure 23. Positive Overload Recovery

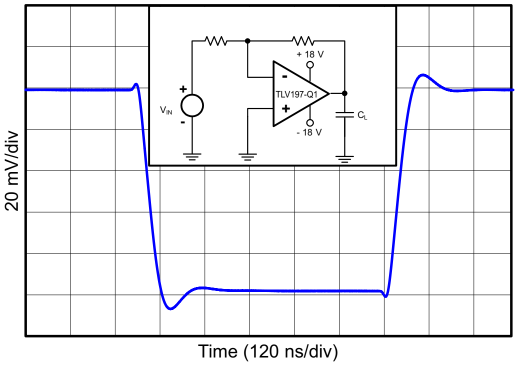


C_L = 10 pF, G = 1

Figure 24. Small-Signal Step Response (100 mV)

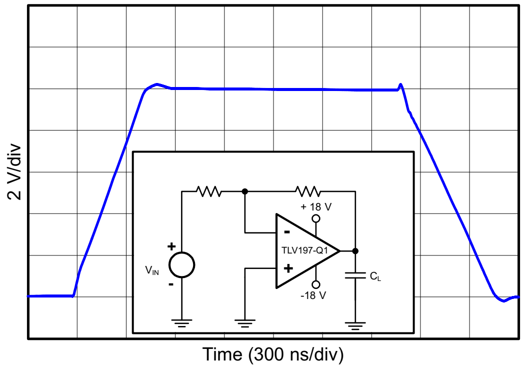
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



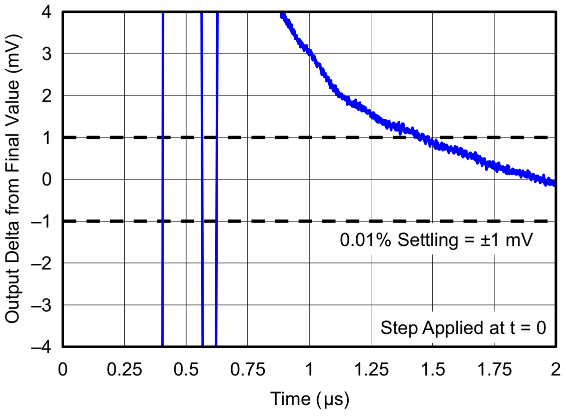
R_L = 1 kΩ, C_L = 10 pF, G = –1

Figure 25. Small-Signal Step Response (100 mV)



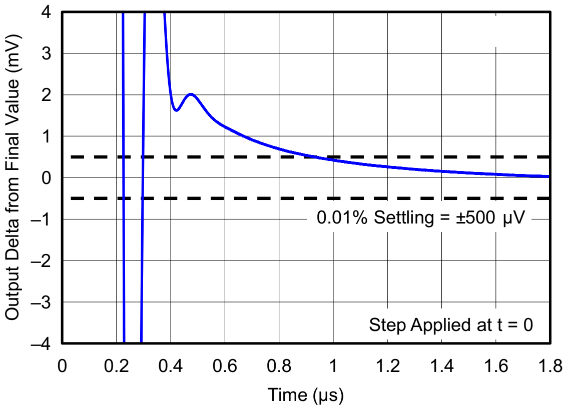
R_L = 1 kΩ, C_L = 10 pF, G = –1

Figure 26. Large-Signal Step Response



G = 1

Figure 27. Settling Time (10-V Positive Step)



G = 1

Figure 28. Settling Time (5-V Positive Step)

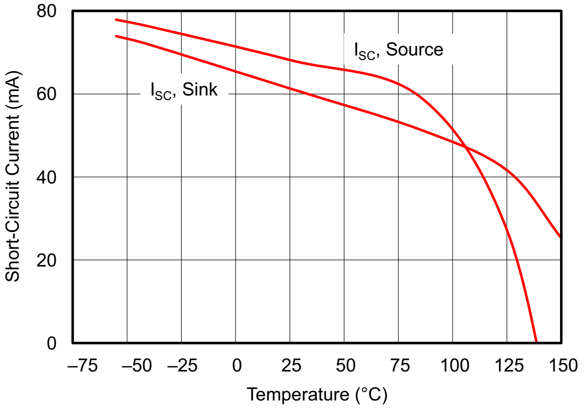


Figure 29. Short-Circuit Current vs Temperature

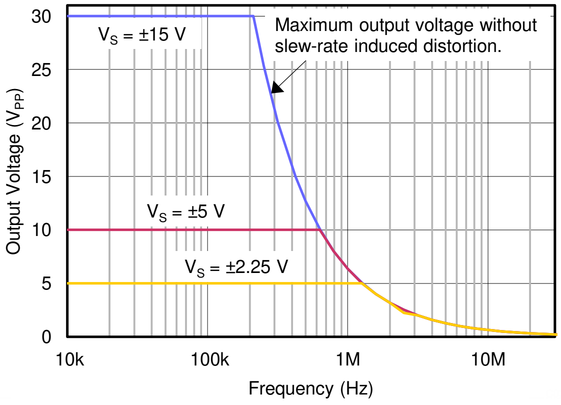


Figure 30. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

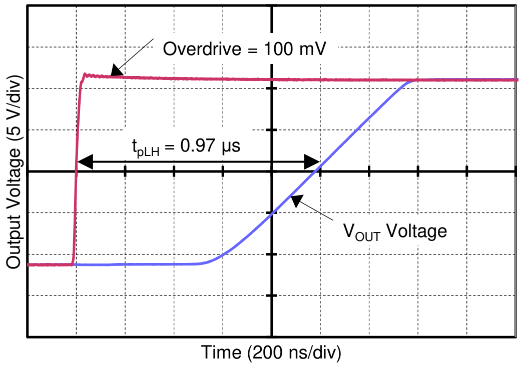


Figure 31. Propagation Delay Rising Edge

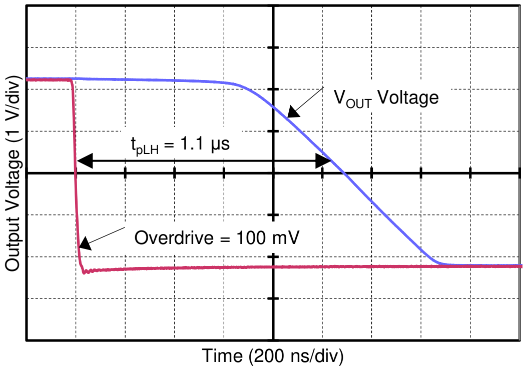


Figure 32. Propagation Delay Falling Edge

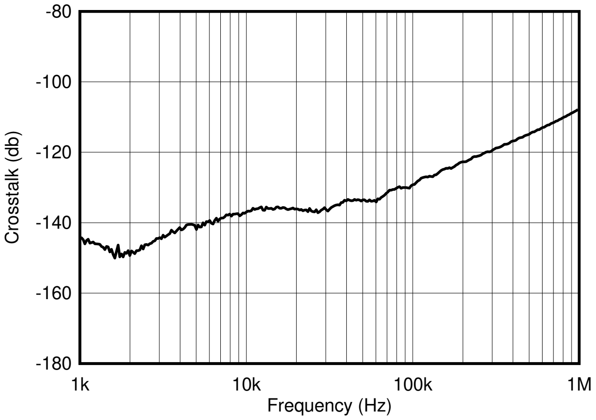


Figure 33. Crosstalk vs Frequency

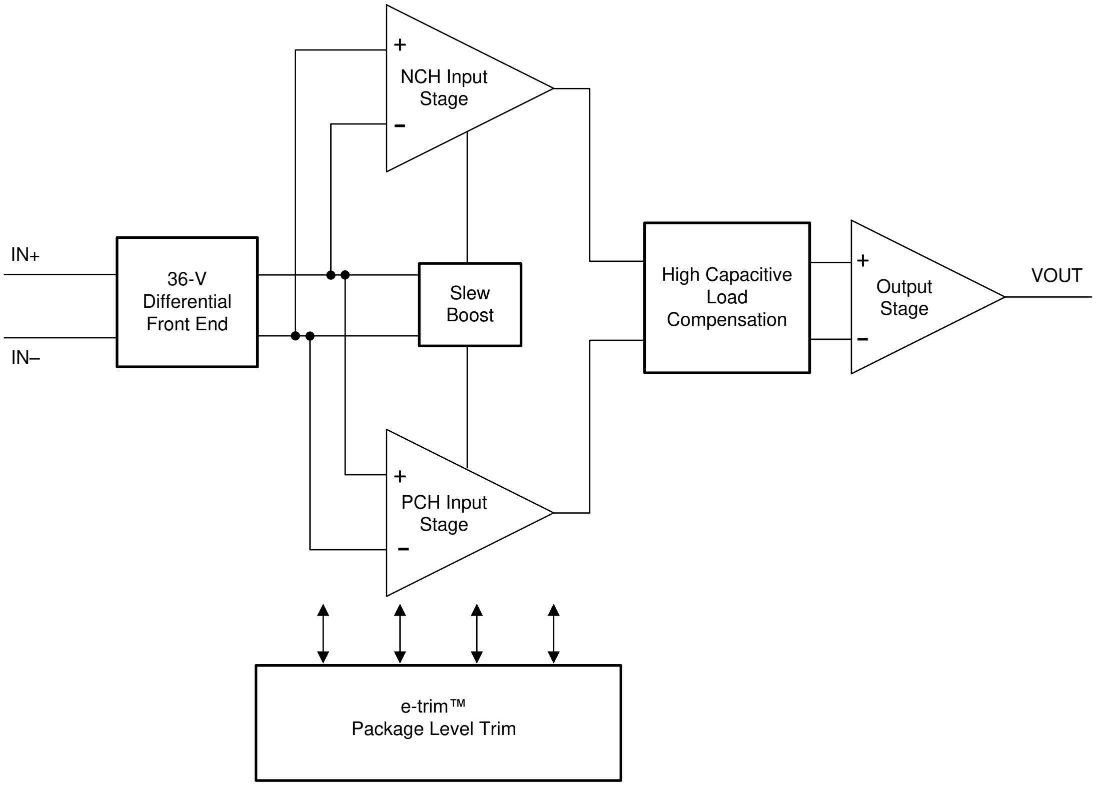
7 Detailed Description

7.1 Overview

The TLVx197-Q1 family of e-trim™ operational amplifiers uses a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. The *Functional Block Diagram* shows the simplified diagram of the TLVx197-Q1 e-trim operational amplifier.

Unlike previous e-trim op amps, the TLVx197-Q1 uses a patented two-temperature trim architecture to achieve a low offset voltage of 500 µV (maximum), and low voltage offset drift of 5 µV/°C (maximum) over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection Circuitry

The TLVx197-Q1 use a unique input architecture to eliminate the need for input protection diodes, but still provide robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 34 can be activated by fast transient step responses, and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 35. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, cause an increase in input current, and result in extended settling time.

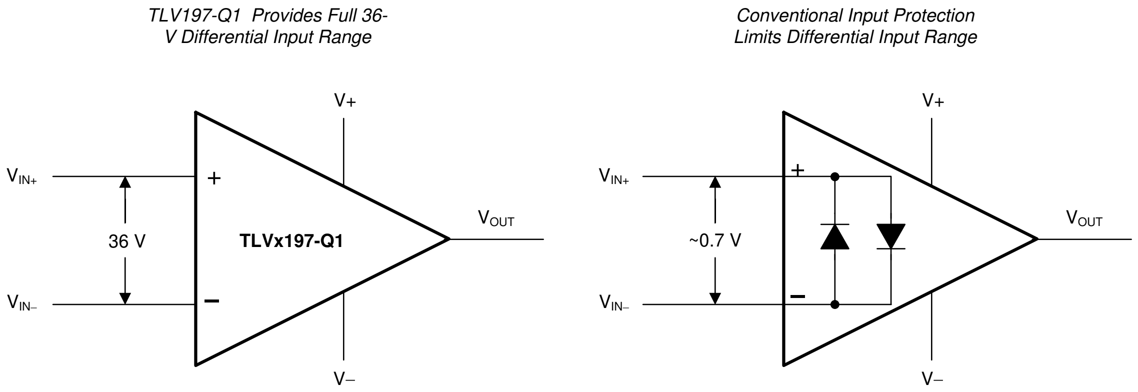


Figure 34. TLVx197-Q1 Input Protection Does Not Limit Differential Input Capability

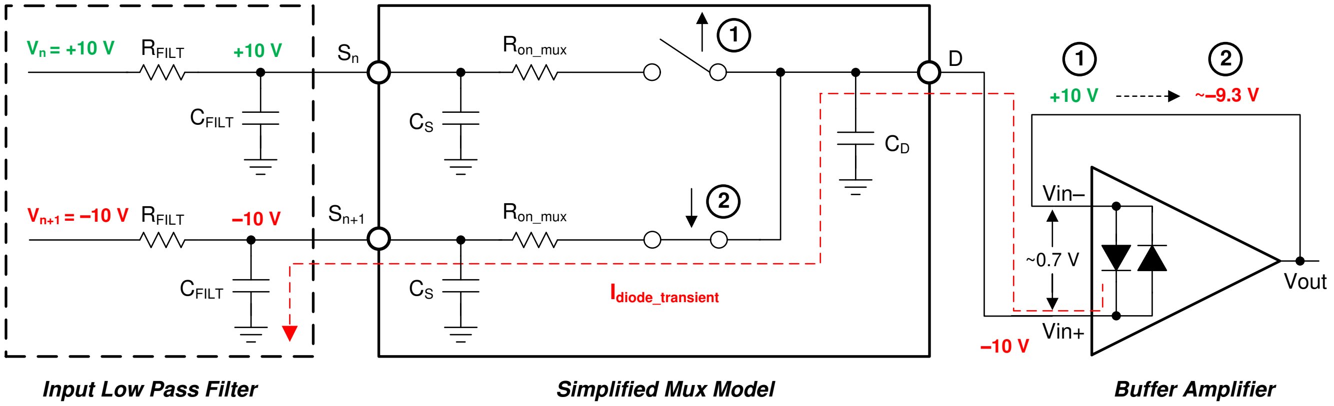


Figure 35. Back-to-Back Diodes Create Settling Issues

The TLVx197-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, and makes the device an excellent choice for multichannel, high-switched, input applications. The TLVx197-Q1 tolerates a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36 V, thus making the device great for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems; see Figure 41.

Feature Description (continued)

7.3.2 EMI Rejection

The TLVx197-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLVx197-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 36 shows the results of this testing on the TLVx197-Q1. Table 1 shows the EMIRR IN+ values for the TLVx197-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

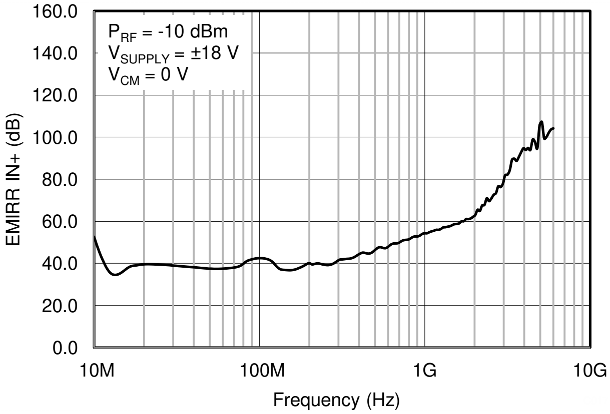


Figure 36. EMIRR Testing

Table 1. TLVx197-Q1 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	44.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	61.0 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.5 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.7 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105.5 dB

7.3.3 Phase Reversal Protection

The TLVx197-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the respective linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLVx197-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail.

7.3.4 Thermal Protection

CAUTION

The absolute maximum junction temperature of the TLVx197-Q1 is 150°C. Exceeding this temperature causes damage to the device.

The internal power dissipation of any amplifier causes the internal (junction) temperature of the amplifier to rise. This phenomenon is called *self heating*. The TLVx197-Q1 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures greater than 140°C. Figure 37 shows an application example for the TLVx197-Q1 that has significant self heating (159°C) because of the power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 37 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer, so the output is 3 V. When self heating causes the device junction temperature to exceed 140°C, the thermal protection forces the output to a high-impedance state, and the output is pulled to ground through resistor RL.

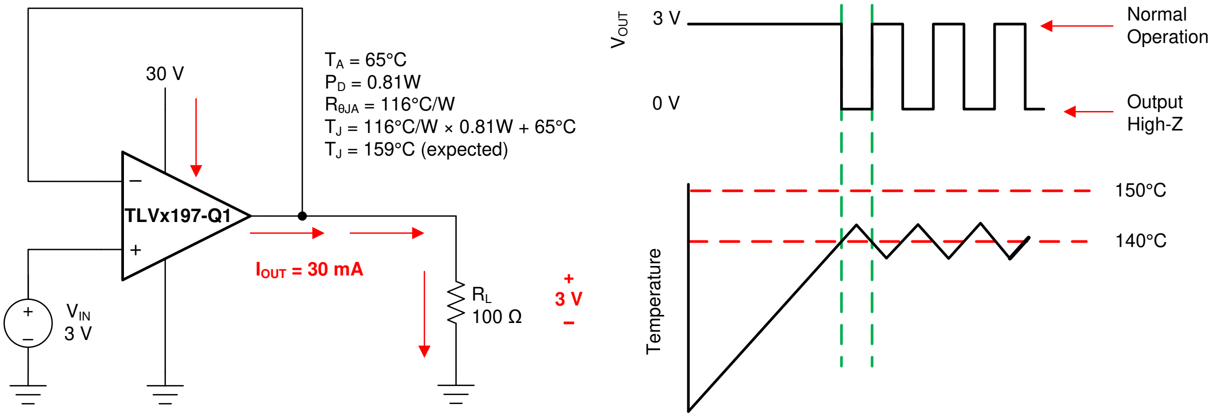


Figure 37. Thermal Protection

7.3.5 Capacitive Load and Stability

The TLVx197-Q1 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads.

The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10-Ω to 20-Ω) resistor, R_{ISO}, in series with the output, as shown in Figure 38. This resistor significantly reduces ringing and maintains dc performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the TLVx197-Q1 a great choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 38 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin, and the results using the TLVx197-Q1 are summarized in Table 2. For additional information on techniques to optimize and design using this circuit, reference design TIPD128, *Capacitive Load Drive Verified Reference Design Using an Isolation Resistor*, details complete design goals, simulation, and test results.

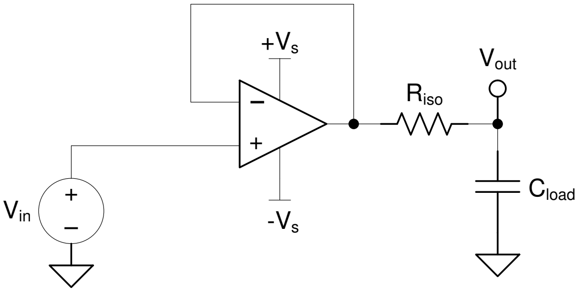


Figure 38. Extending Capacitive Load Drive With the TLVx197-Q1

Table 2. TLVx197-Q1 Capacitive Load Drive Using Isolation Resistor Comparison of Calculated and Measured Results

PARAMETER	VALUE									
Capacitive Load	100 pF		1000 pF		0.01 µF		0.1 µF		1 µF	
Phase Margin	45°	60°	45°	60°	45°	60°	45°	60°	45°	60°
R_{ISO} (Ω)	47	360	24	100	20	51	6.2	15.8	2	4.7
Measured Overshoot (%)	23.2 8.6	10.4	22.5	9	22.1	8.7	23.1	8.6	21	8.6
Calculated PM	45.1°	58.1°	45.8°	59.7°	46.1°	60.1°	45.2°	60.2°	47.2°	60.2°

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, see TI Precision Design TIDU032, *Capacitive Load Drive Solution using an Isolation Resistor* .

7.3.6 Common-Mode Voltage Range

The TLVx197-Q1 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 39. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3 V to 100 mV greater than the positive supply. The P-channel pair is active for inputs from 100 mV less than the negative supply to approximately (V+) – 1.5 V. There is a small transition region, typically (V+) –3 V to (V+) – 1.5 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

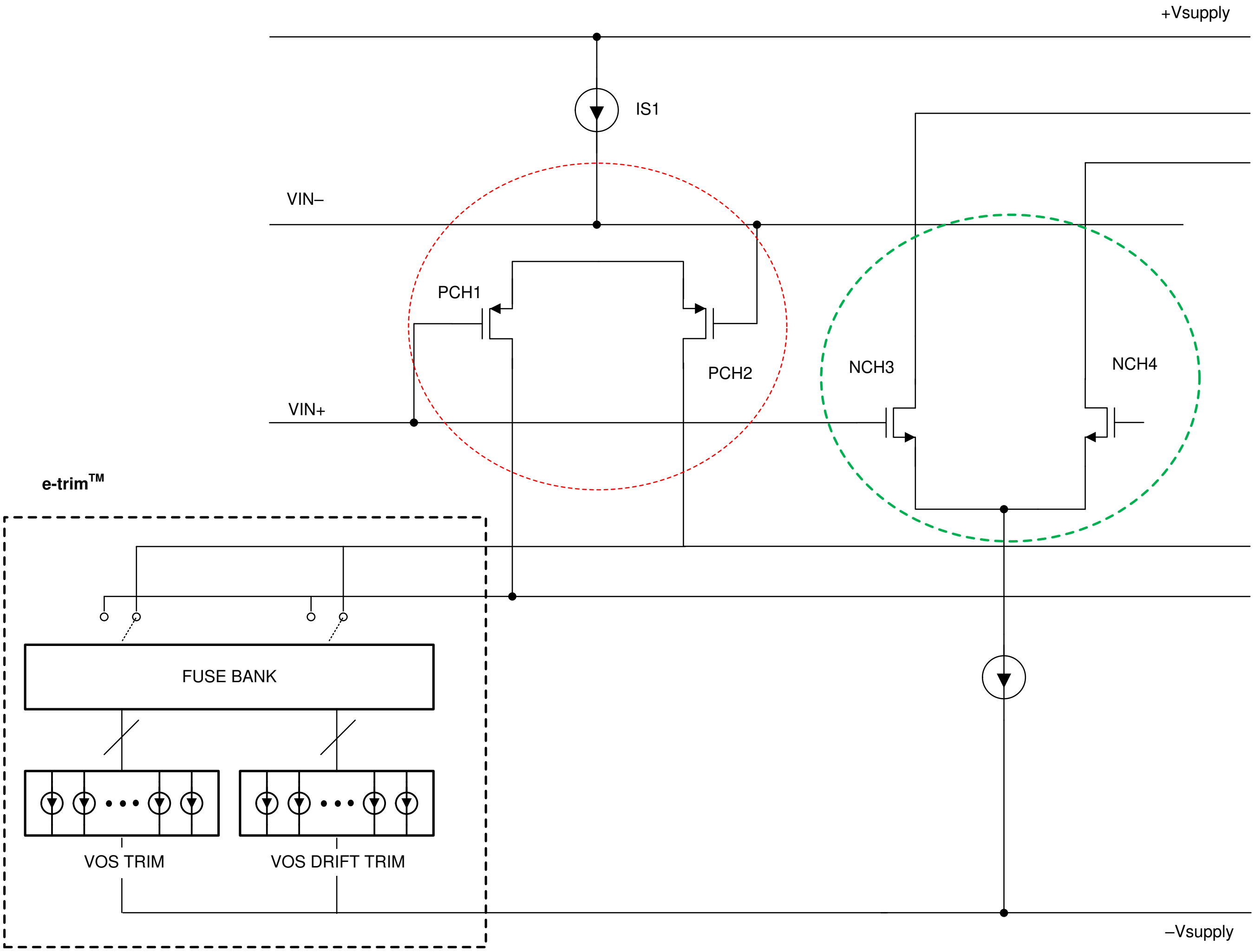


Figure 39. Rail-to-Rail Input Stage

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The TLVx197-Q1 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, and causes the variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range.

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 40 shows an illustration of the ESD circuits contained in the TLVx197-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

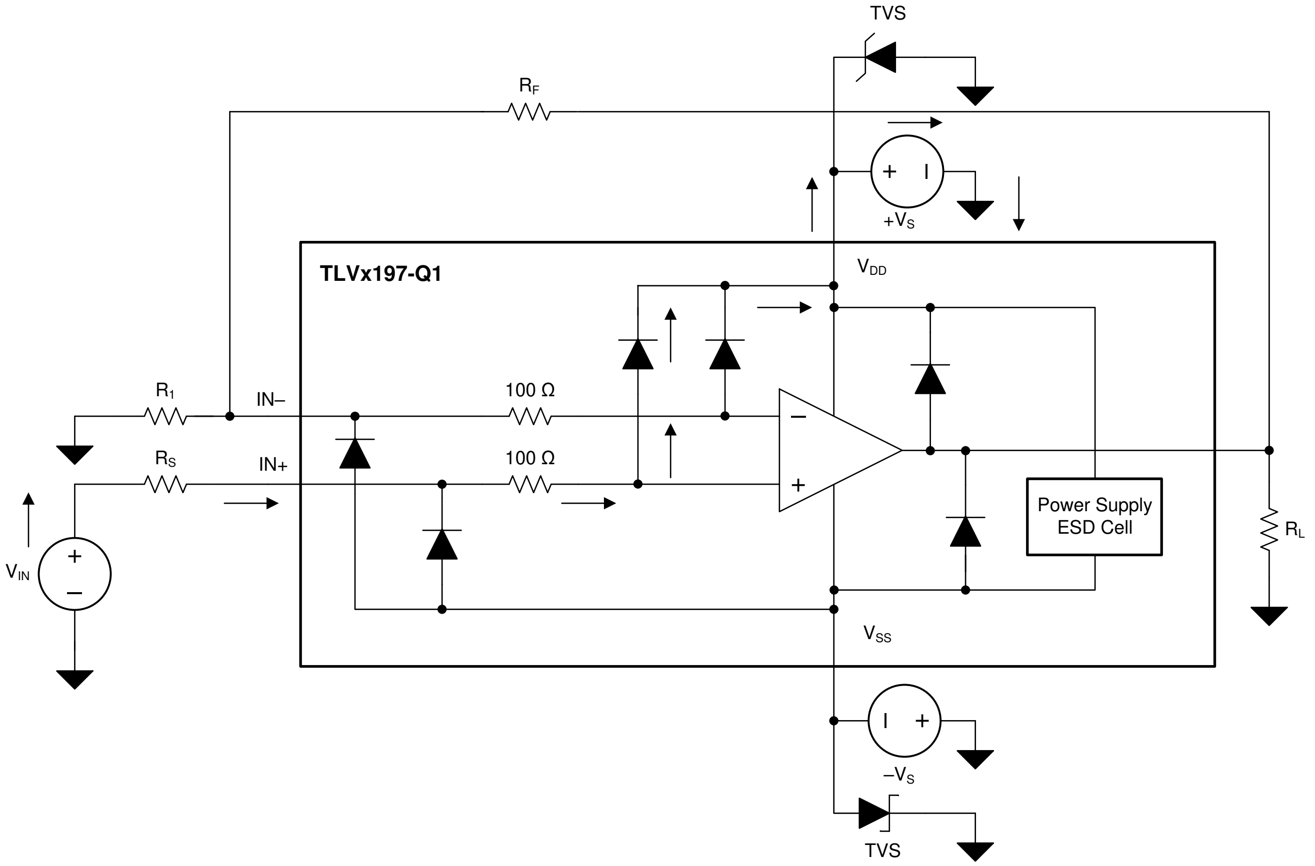


Figure 40. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns); whereas, an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx197-Q1 is approximately 200 ns.

7.4 Device Functional Modes

The TLVx197-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the TLVx197-Q1 is 36 V (±18 V).

8 Application and Implementation

8.1 Application Information

The TLVx197-Q1 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer true rail-to-rail input and output, low offset voltage and offset voltage drift, as well as 10-MHz bandwidth and high capacitive load drive. These features make the TLVx197-Q1 a robust, high-performance operational amplifier for high-voltage automotive applications.

8.2 Typical Applications

8.2.1 16-Bit Precision Multiplexed Data-Acquisition System

Figure 41 shows a 16-bit, differential, 4-channel, multiplexed data-acquisition system. This example is typical in sensor based applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential multiplexer (mux). This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the TLVx197-Q1 and TLV140 to achieve excellent dynamic performance and linearity with the ADS8864.

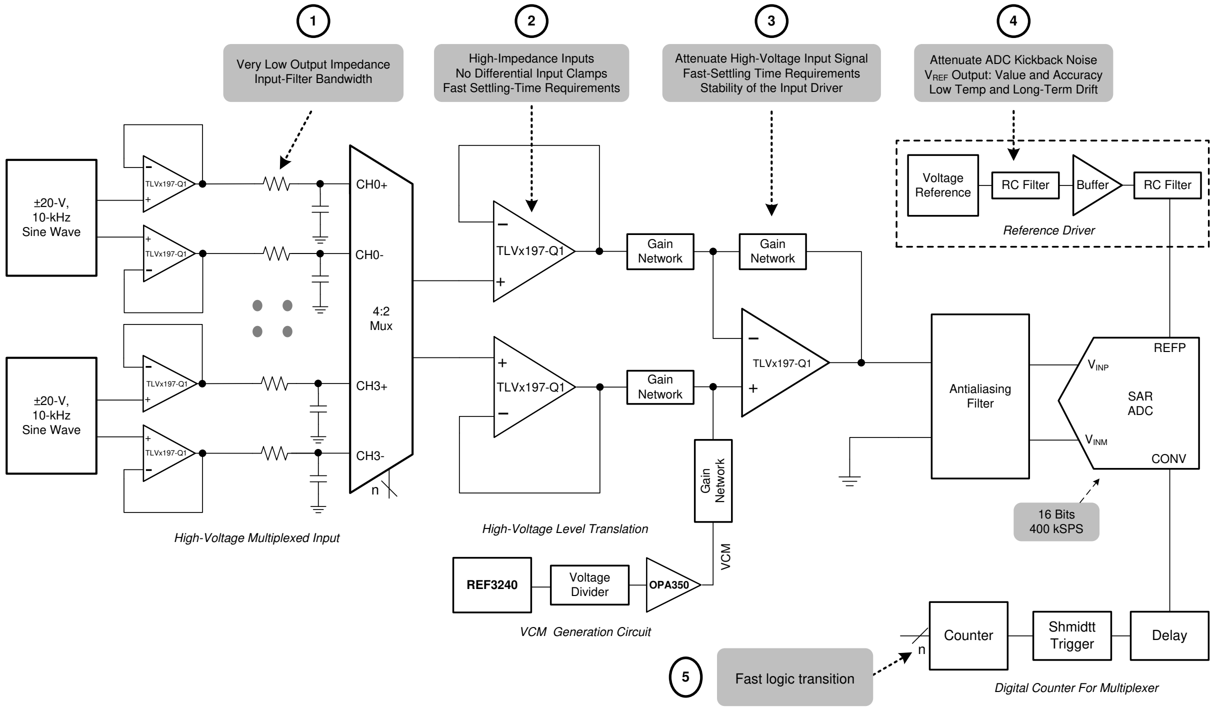


Figure 41. TLVx197-Q1 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs With Lowest Distortion

Typical Applications (continued)

8.2.1.1 Design Requirements

The primary objective is to design a ±20 V, differential 4-channel multiplexed data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10 kHz full-scale pure sine-wave input. The design requirements for this block design are:

- System supply voltage: ±15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 10 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

8.2.1.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal high voltage multiplexed data acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in Figure 41. The circuit is a multichannel data acquisition signal chain consisting of an input low-pass filter, multiplexer (mux), mux output buffer, attenuating SAR ADC driver, digital counter for mux and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two primary design considerations to maximize the performance of a precision multiplexed data acquisition system are the mux input analog front-end and the high-voltage level translation SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. Figure 41 includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for extremely low impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front-end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input when maintaining amplifier stability. The next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.

8.2.1.3 Application Curve

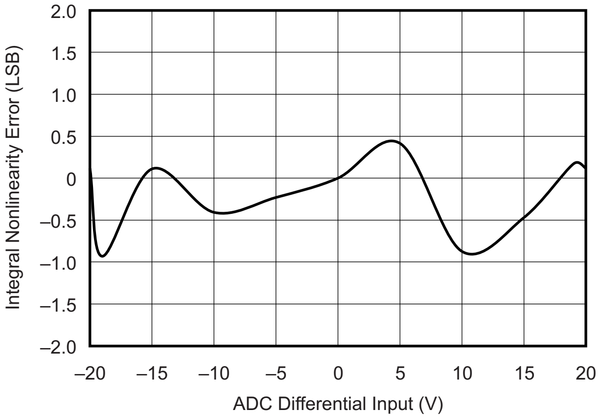


Figure 42. ADC 16-Bit Linearity Error for the Multiplexed Data Acquisition Block

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TIPD151, *16-Bit, 400 kSPS 4-Channell, Multiplexed Data Acquisition Ref erence Design for High Voltage Inputs, Low Distortion*.

8.2.2 Slew-Rate Limit for Input Protection

In control systems for motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the TLVx197-Q1 make these devices an optimal amplifier to achieve slew-rate control for both dual- and single-supply systems.Figure 43 shows the TLVx197-Q1 in a slew-rate limit design.

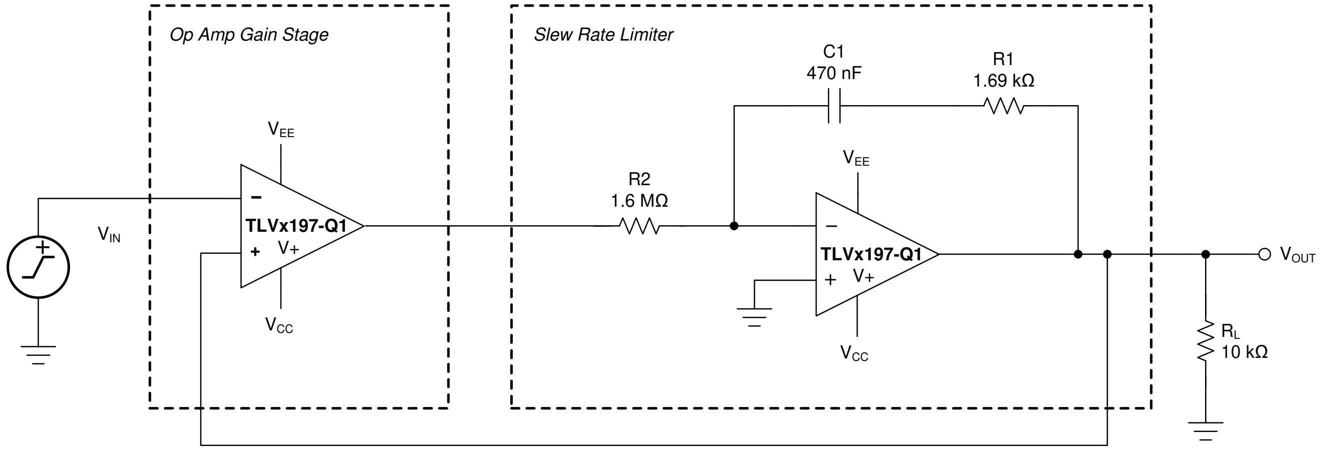


Figure 43. Slew-Rate Limiter Uses One Op Amp

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see TIPD140, *Single Op-Amp Slew Rate Limiter Reference Design*.

8.2.3 Precision Reference Buffer

The TLVx197-Q1 feature high output-current-drive capability and low input offset voltage, making the device an excellent reference buffer to provide an accurate buffered output with ample drive current for transients. For the 10-µF ceramic capacitor shown in Figure 44, R_{ISO}, a 37.4-Ω isolation resistor, provides separation of two feedback paths for optimal stability. Feedback path number one is through R_F and is directly at the output (V_{OUT}). Feedback path number two is through R_{Fx} and C_F and is connected at the output of the op amp. The optimized stability components shown for the 10-µF load give a closed-loop signal bandwidth at V_{OUT} of 4 kHz and still provide a loop gain phase margin of 89°. Any other load capacitances require recalculation of the stability components: R_F, R_{Fx}, C_F, and R_{ISO}.

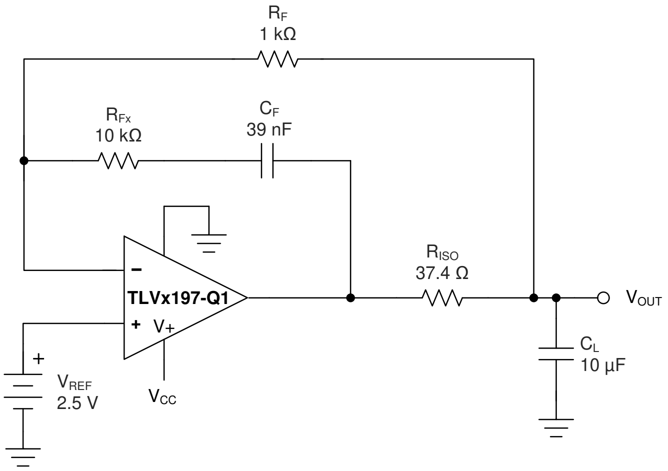


Figure 44. Precision Reference Buffer

9 Power Supply Recommendations

The TLVx197-Q1 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole. and through the individual op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in Figure 46, keep RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Examples

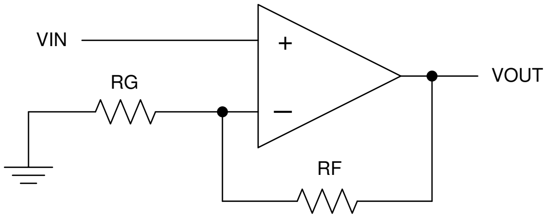


Figure 45. Schematic Representation

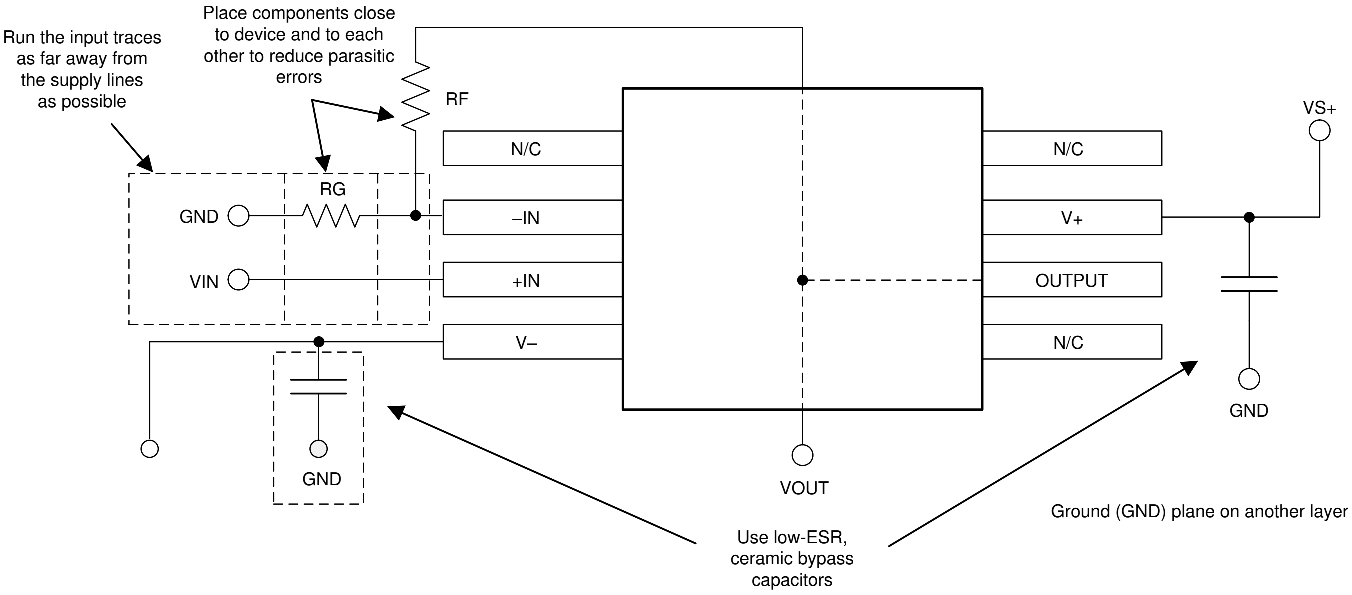


Figure 46. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Capacitive Load Drive Solution using an Isolation Resistor* reference design

11.3 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV197-Q1	Click here	Click here	Click here	Click here	Click here
TLV2197-Q1	Click here	Click here	Click here	Click here	Click here
TLV4197-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV197QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	Q197	Samples
TLV2197QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2BD6	Samples
TLV4197QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	T4197Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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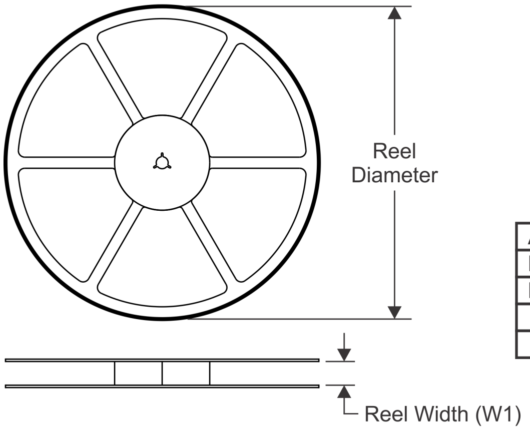
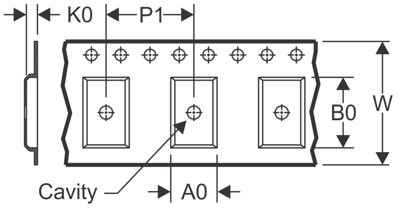
TAPE AND REEL INFORMATION

REEL DIMENSIONS

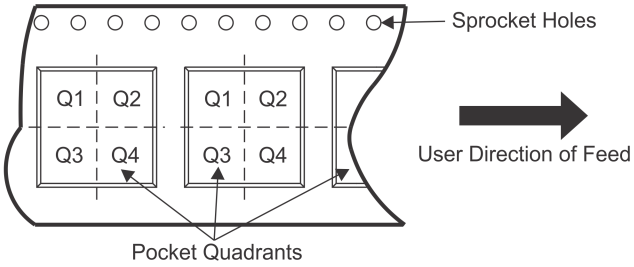


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

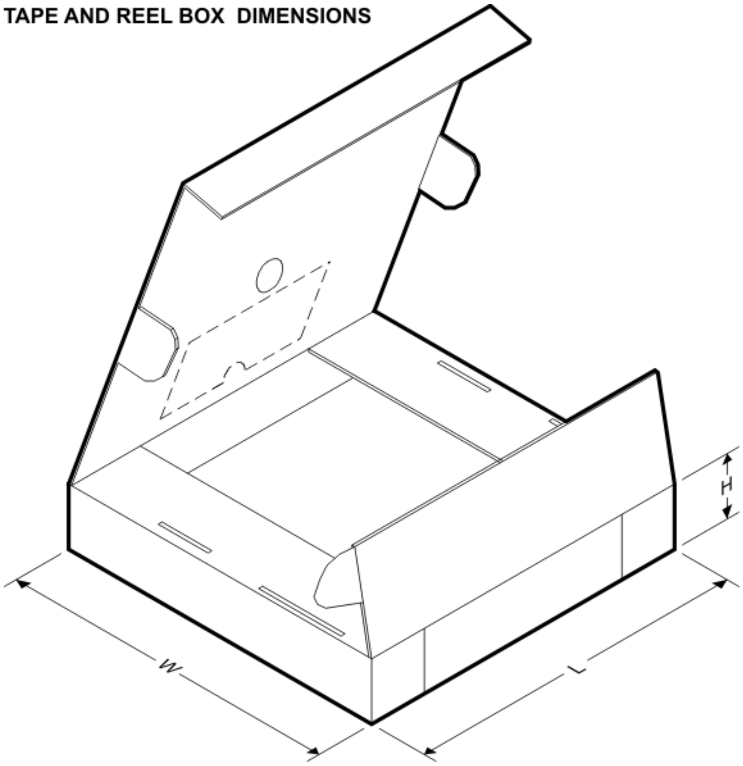
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV197QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2197QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV4197QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

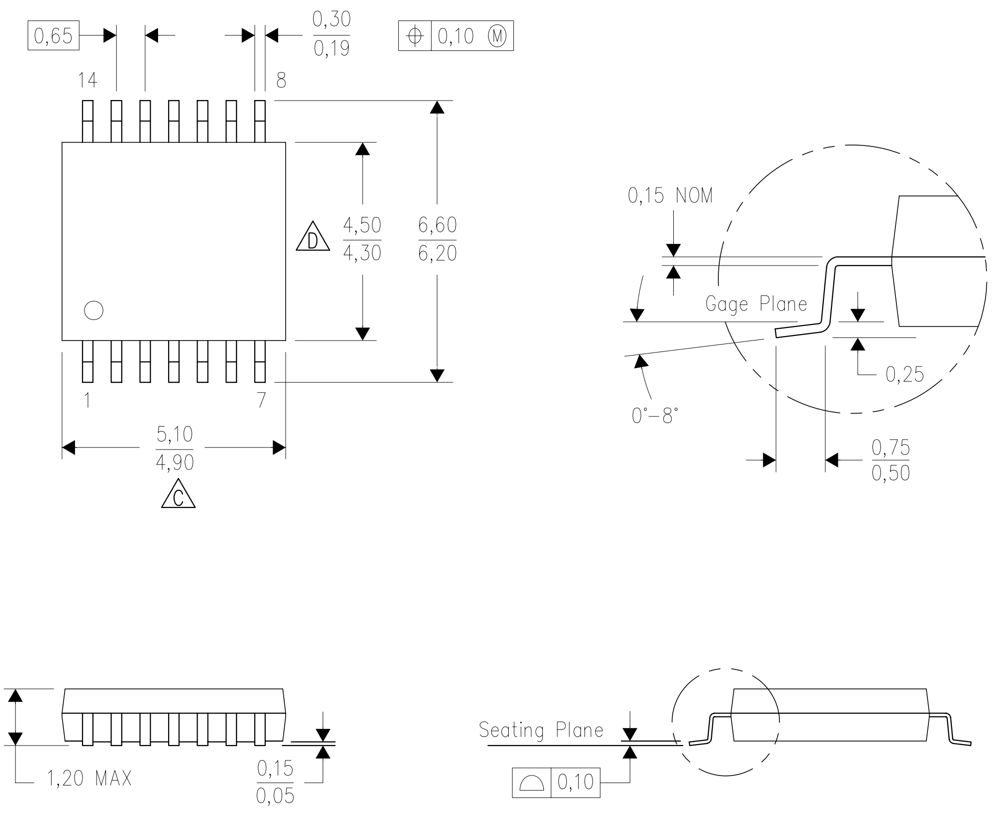
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV197QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2197QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV4197QPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

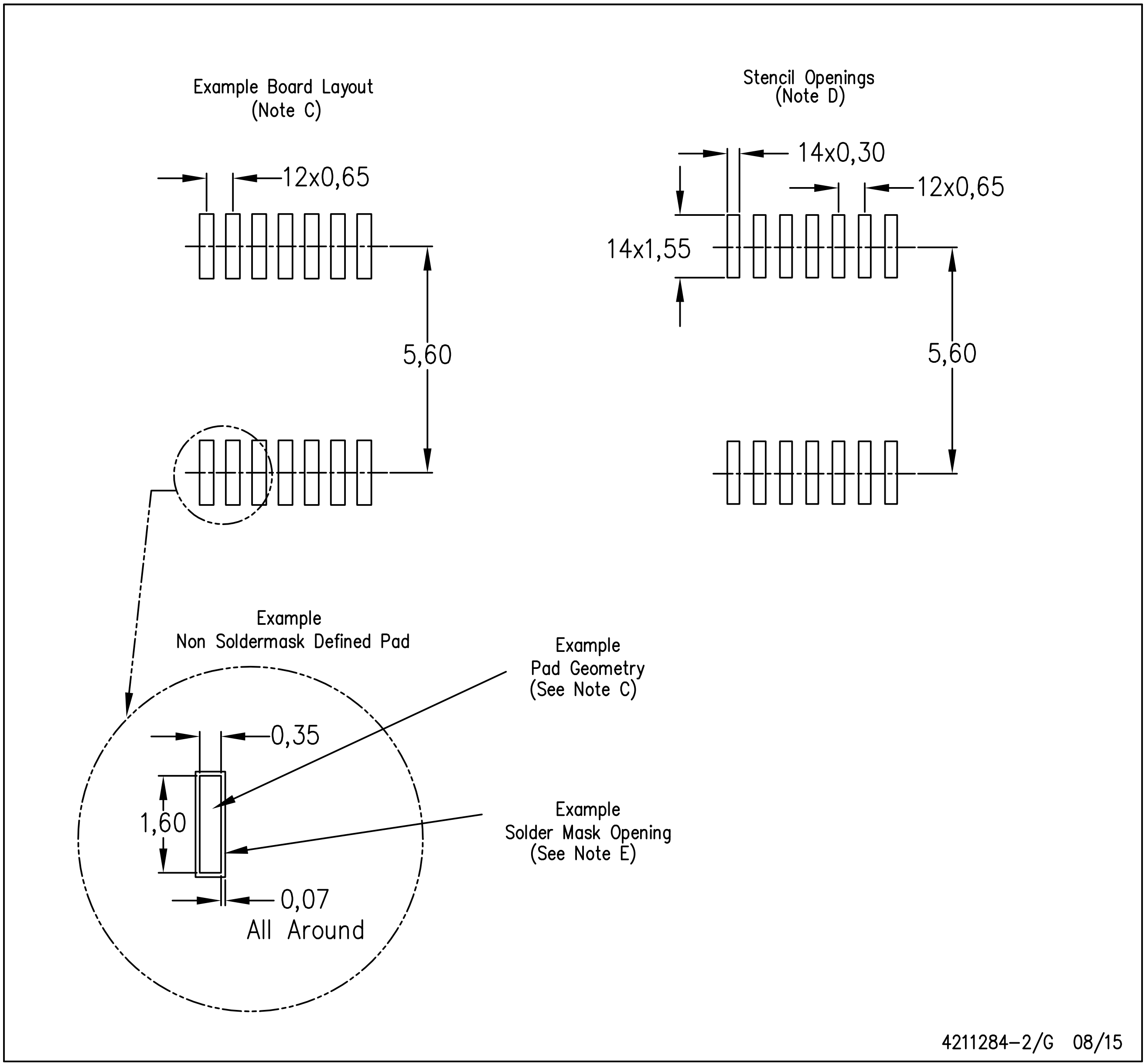
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

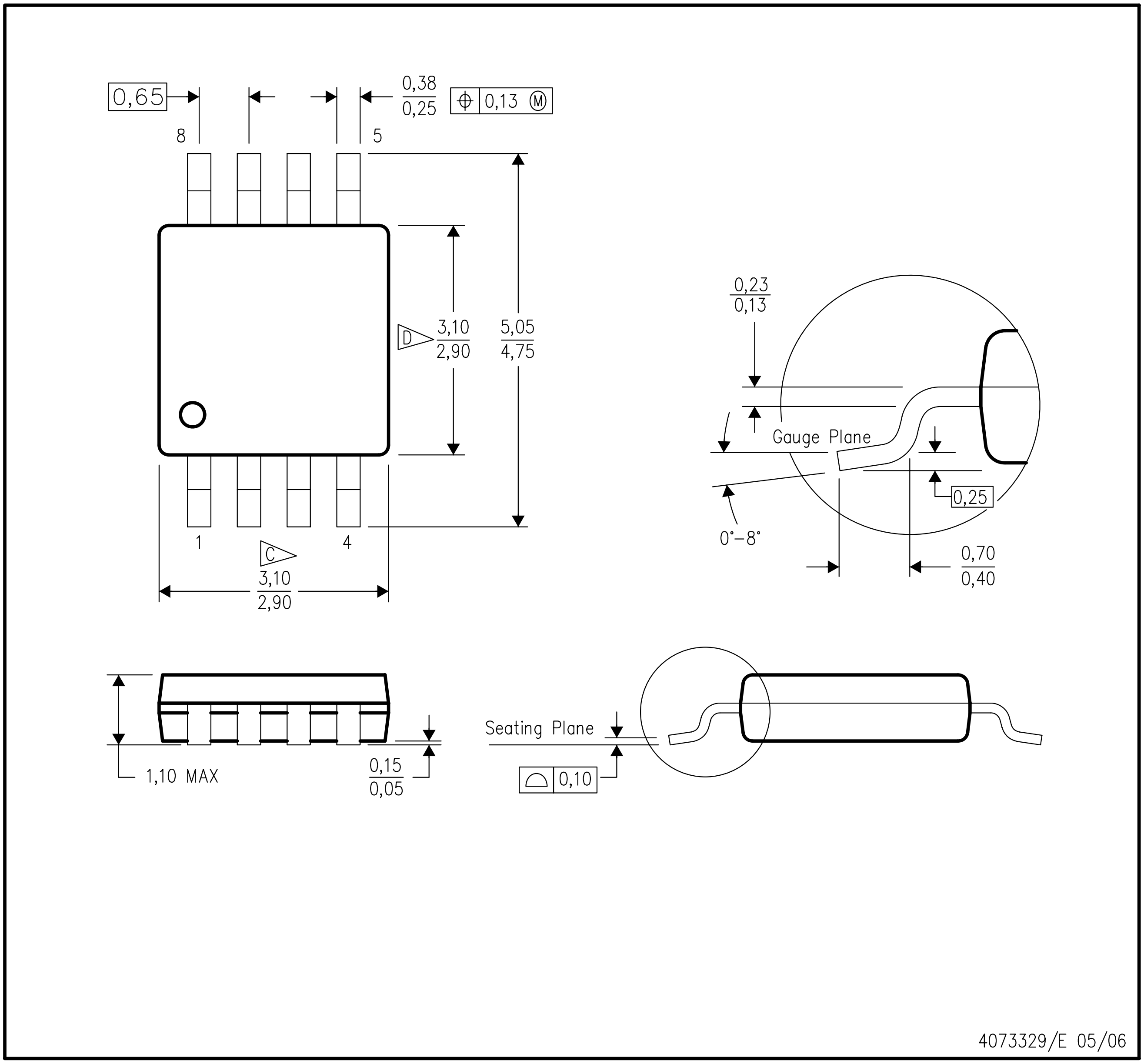
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

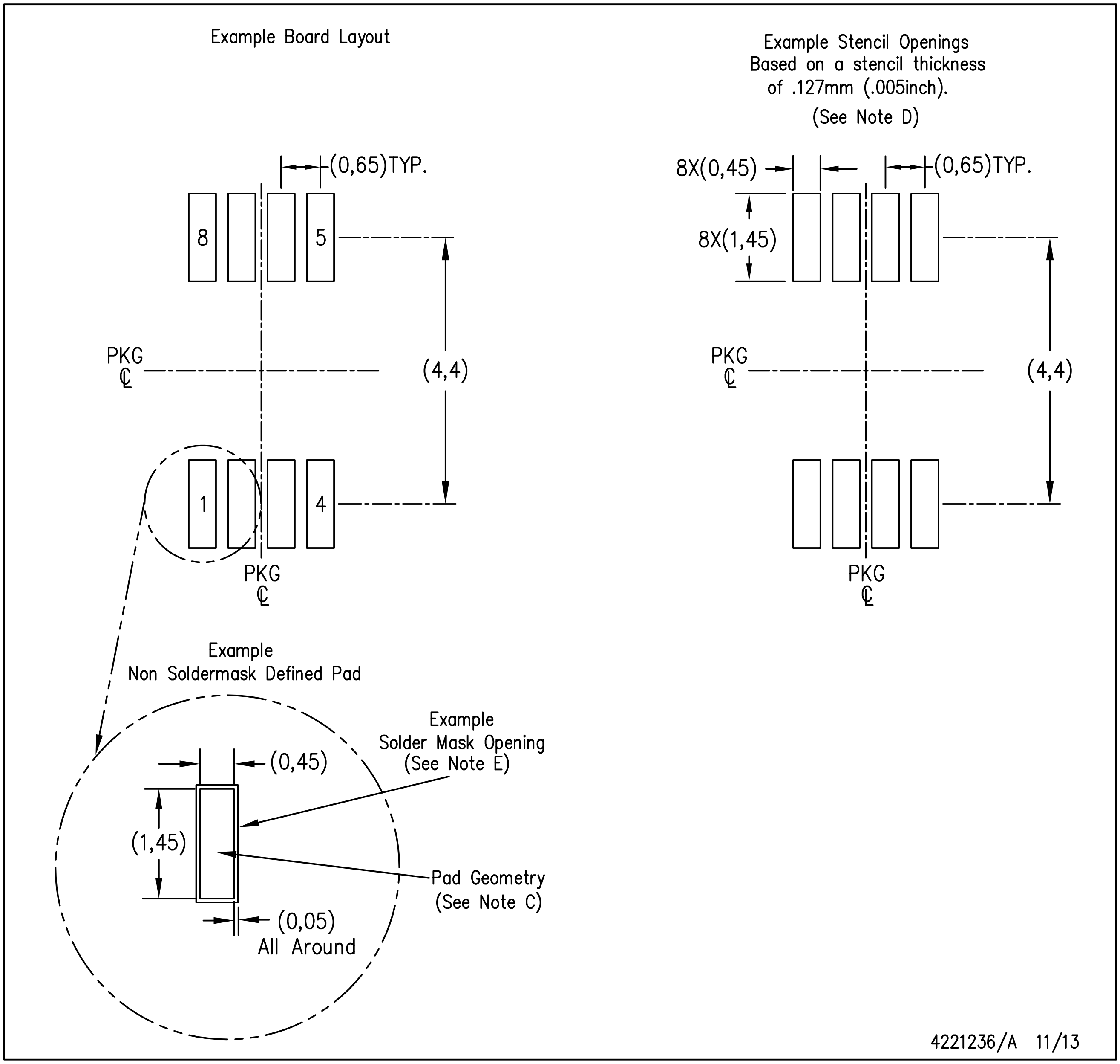
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



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- B. This drawing is subject to change without notice.
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- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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