CURRENT SHUNT MONITORS –16-V to 80-V COMMON MODE RANGE

Check for Samples: INA193A-EP

FEATURES

- **Wide Common-Mode Voltage: –16 V to 80 V**
- **Low Error: 3.0% Over Temp (Max)**
- **Bandwidth: Up to 500 kHz**
- **Three Transfer Functions Available: 20 V/V, 50 V/V, and 100 V/V**
- **Complete Current Sense Solution**

APPLICATIONS

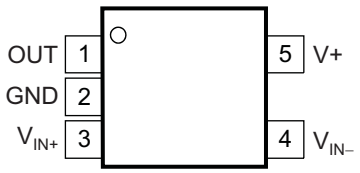
- **Welding Equipment**
- **Notebook Computers**
- **Cell Phones**
- **Telecom Equipment**
- **Automotive**
- **Power Management**
- **Battery Chargers**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges available - contact factory

DBV PACKAGE (TOP VIEW)



DESCRIPTION

The INA193A current shunt monitors with voltage output can sense drops across shunts at common-mode voltages from –16 V to 80 V, independent of the INA19x supply voltage. They are available with three output voltage scales: 20 V/V, 50 V/V, and 100 V/V. The 500-kHz bandwidth simplifies use in current control loops.

The INA193A operates from a single 2.7-V to 18-V supply, drawing a maximum of 1300-µA of supply current. It is specified over the extended operating temperature range (–55°C to 125°C), and is offered in a space-saving SOT23 package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

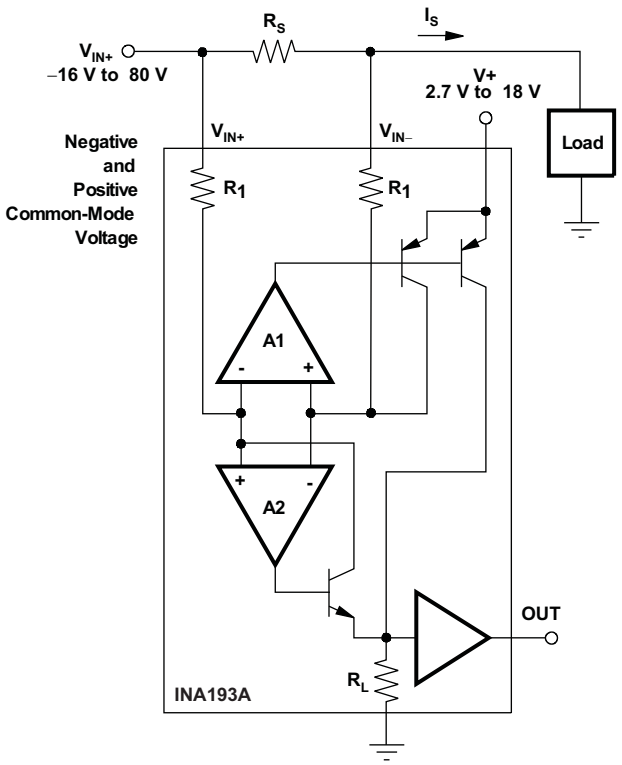
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT23-5 – DBV	INA193AMDBVREP	CCC

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

MODEL	GAIN	PACKAGE
INA193A	20 V/V	SOT23-5



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Supply voltage			18	V
V_{IN+} V_{IN-}	Analog input voltage range	Differential (V_{IN+} – V_{IN-})	–18	18	V
		Common mode(2)	–16	80	
	Analog outputt voltage range(2)	OUT	GND – 0.3	(V+) + 0.3	V
	Input current into any pin(2)			5	mA
	Operating temperature range		–55	150	°C
	Storage temperature range		–65	150	°C
	Junction temperature			150	°C
	ESD ratings	Human-Body Model (HBM)		4000	V
		Charged-Device Model (CDM)		1000	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5 mA.

Electrical Characteristics

V_S = + 12 V. **Boldface** limits apply over the specified temperature range, **T_A = –55°C to 125°C**. All specifications at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
Full-scale input voltage	V_{SENSE}	V_{SENSE} = V_{IN+} – V_{IN-}		0.15	(V_S – 0.2)/Gain	V
Common-mode input range	**V_{CM}**		**–16**		**80**	V
Common-mode rejection	CMR	V_{IN+} = –16 V to 80 V	80	94		dB
Over temperature		**V_{IN+} = 12 V to 80 V**	**100**	**120**		dB
Offset voltage, RTI	V_{OS}			±0.5	2	mV
Over temperature				**0.5**	**3**	mV
vs temperature	**dV_{OS}/dT**			**2.5**		µV/°C
vs power supply	**PSR**	**V_S = 2.7 V to 18 V, V_{IN+} = 18 V**		**5**	**100**	µV/V
Input bias current, V_{IN-} pin	**I_B**			**±8**	**±23**	µA
OUTPUT (V_{SENSE} ≥ 20 mV)						
Gain	G			20		V/V
Gain error		V_{SENSE} = 20 mV to 100 mV, T_A = 25°C		±0.2	±1	%
Over temperature		**V_{SENSE} = 20 mV to 100 mV**			**±2**	%
Total output error(1)				±0.75	±2.2	%
Over temperature				**±1**	**±3**	%
Nonlinearity error		V_{SENSE} = 20 mV to 100 mV		±0.002	±0.1	%
Output impedance	R_O			1.5		Ω
Maximum capacitive load		No sustained oscillation		10		nF

(1) Total output error includes effects of gain error and V_{OS}.

Electrical Characteristics (continued)

V_S = + 12 V. **Boldface** limits apply over the specified temperature range, **T_A = –55°C to 125°C**. All specifications at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted).

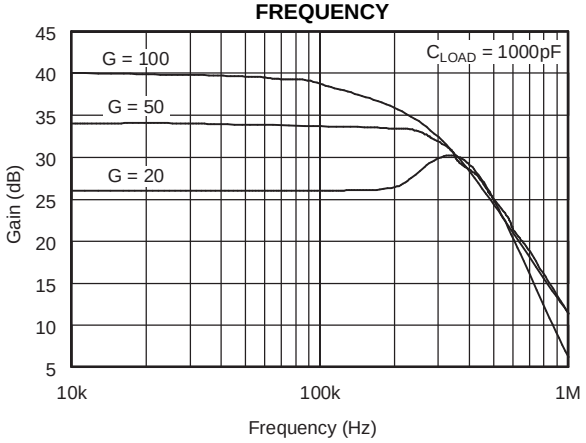
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT (V_{SENSE} < 20 mV)(2)						
		–16 V ≤ V_{CM} < 0 V		300		mV
		0 V ≤ V_{CM} ≤ V_S, V_S = 5 V			0.4	V
		V_S < V_{CM} ≤ 80 V		300		mV
VOLTAGE OUTPUT(3)		**R_L = 100 KΩ to GND**				
Swing to V+ power-supply rail				**(V+) – 0.1**	**(V+) – 0.2**	V
Swing to GND(4)				**V_{GND} + 3**	**V_{GND} + 50**	mV
FREQUENCY RESPONSE						
Bandwidth	BW	C_{LOAD} = 5 pF		500		kHz
Phase margin		C_{LOAD} < 10 nF		40		Degrees
Slew rate	SR			1		V/µs
Settling time (1%)	t_S	V_{SENSE} = 10 mV to 100 mV_{PP}, C_{LOAD} = 5 pF		2		µs
NOISE, RTI						
Voltage noise density				40		nV/√Hz
POWER SUPPLY						
Operating range	**V_S**		**2.7**		**18**	V
Quiescent Current	**I_Q**	**V_{OUT} = 2 V**		**700**	**1300**	µA
		V_{SENSE} = 0 mV		**370**	**950**	µA
TEMPERATURE RANGE						
Specified temperature range			–55		125	°C
Operating temperature range			–55		150	°C
Storage temperature range			–65		150	°C
Thermal resistance, SOT23	θ_{JA}			200		°C/W

(2) For details on this region of operation, see the *Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage* section in the Applications Information.
(3) See Typical Characteristic curve *Output Swing vs Output Current*.
(4) Specified by design

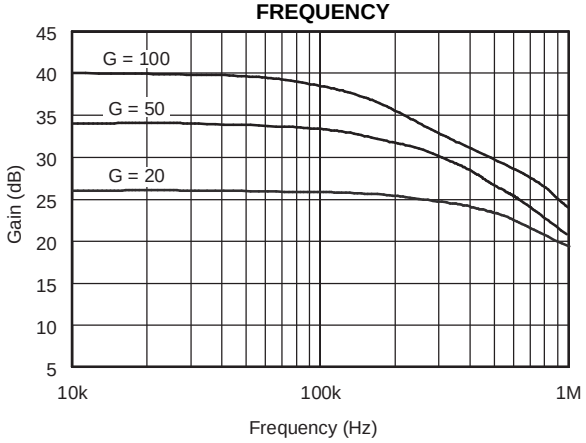
TYPICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_S = 12 V, and V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted).

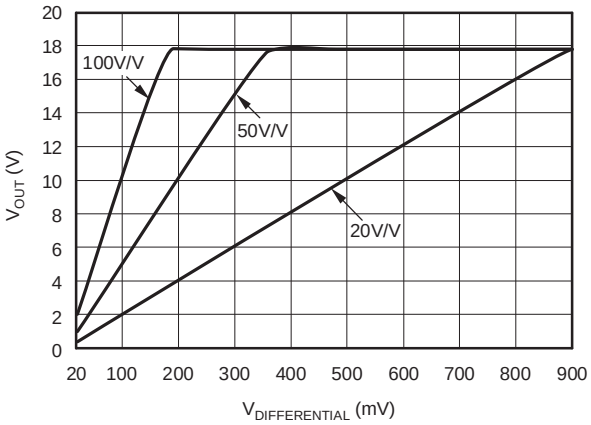
GAIN vs FREQUENCY



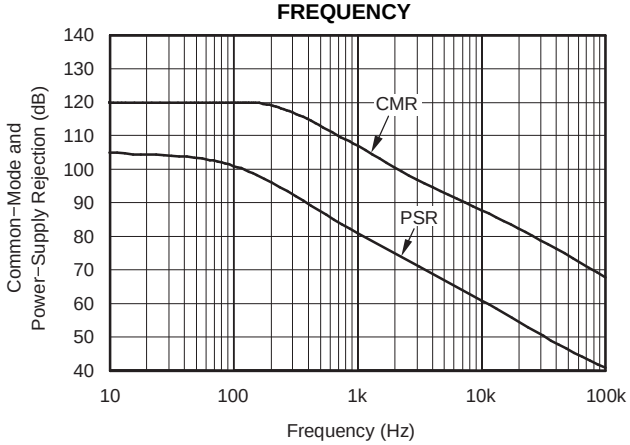
GAIN vs FREQUENCY



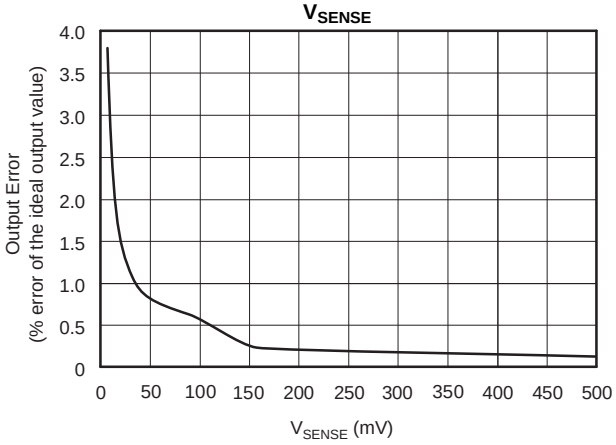
GAIN PLOT



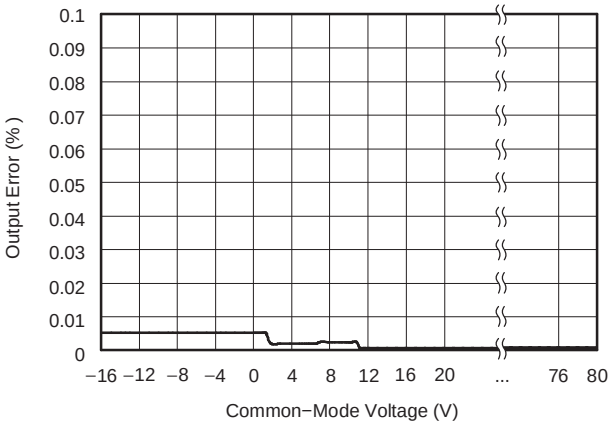
COMMON-MODE AND POWER-SUPPLY REJECTION vs FREQUENCY



OUTPUT ERROR vs V_{SENSE}



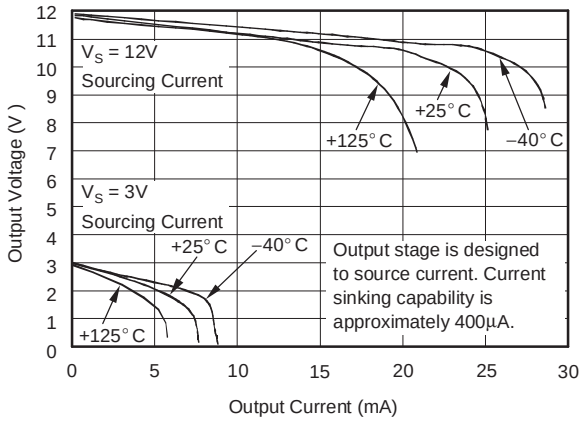
OUTPUT ERROR vs COMMON-MODE VOLTAGE



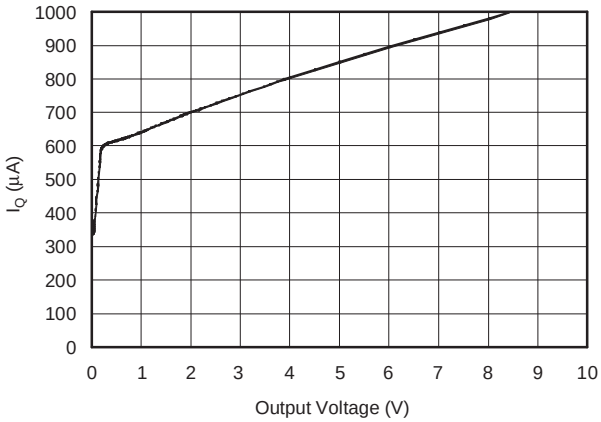
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 12 V, and V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted).

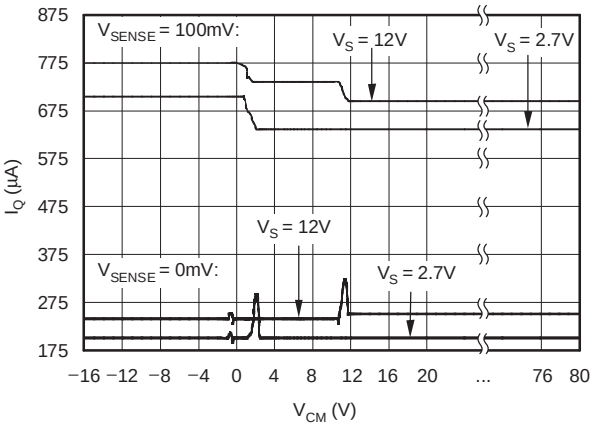
POSITIVE OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



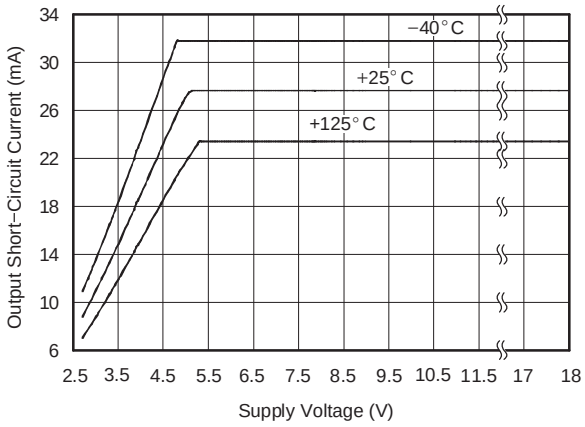
QUIESCENT CURRENT vs OUTPUT VOLTAGE



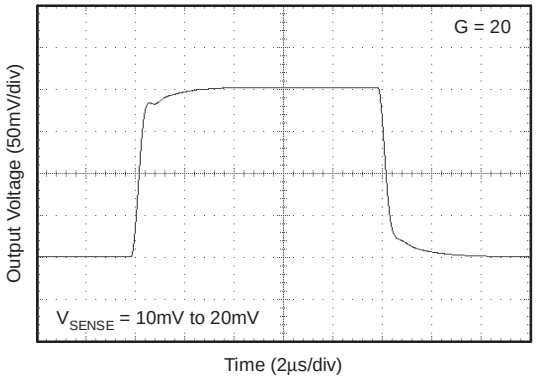
QUIESCENT CURRENT vs COMMON-MODE VOLTAGE



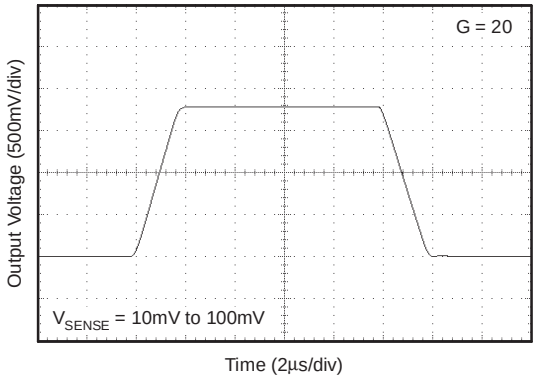
OUTPUT SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE



STEP RESPONSE



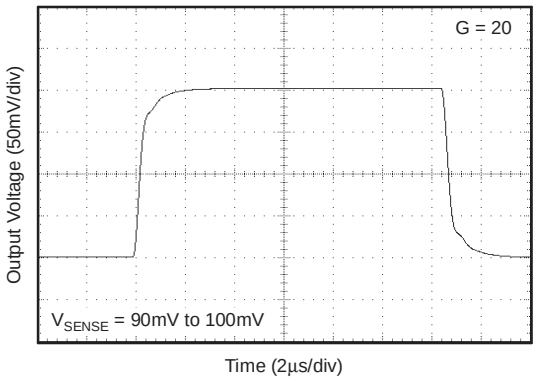
STEP RESPONSE



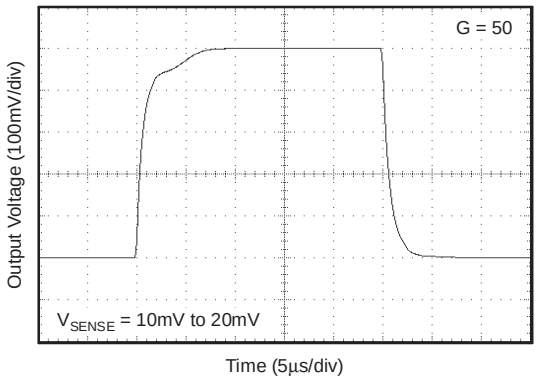
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 12 V, and V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted).

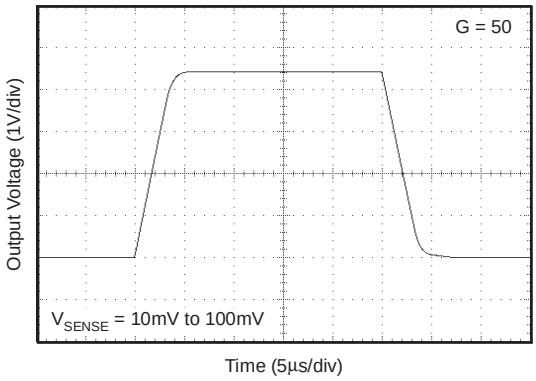
STEP RESPONSE



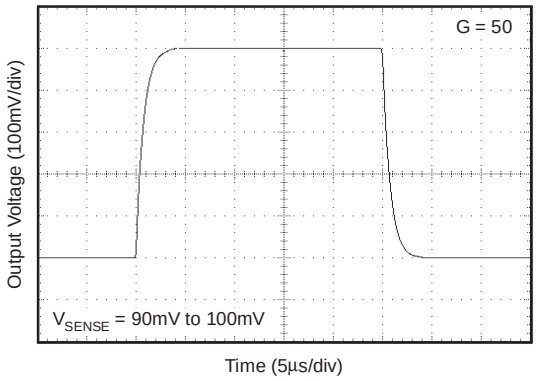
STEP RESPONSE



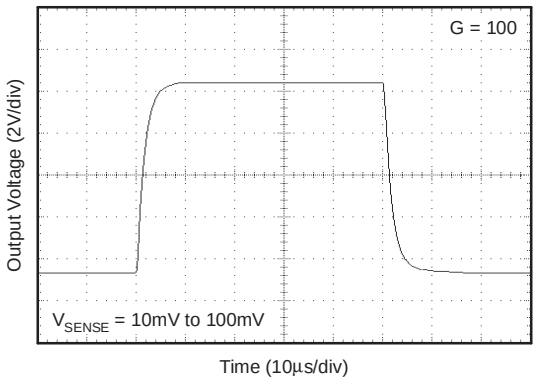
STEP RESPONSE



STEP RESPONSE



STEP RESPONSE



APPLICATION INFORMATION

Basic Connection

Figure 1 shows the basic connection of INA193A. The input pins, V_{IN+} and $V_{IN–}$, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high impedance power supplies may require additional decoupling capacitors to reject power supply noise. Connect bypass capacitors close to the device pins.

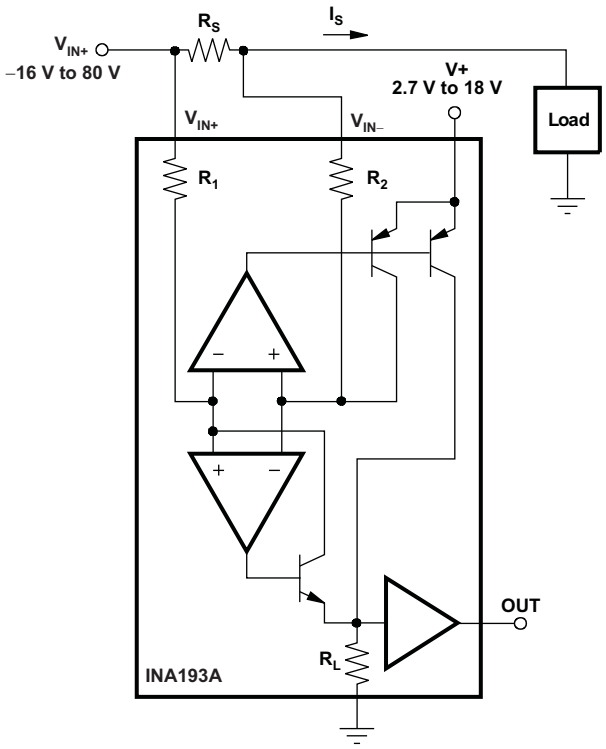


Figure 1. INA193A Basic Connection

Power Supply

The input circuitry of the INA193A can accurately measure beyond its power supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power supply voltage is up to 80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA193A current shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} – V_{IN–}$) and common-mode voltage, V_{CM}, relative to the supply voltage, V_S. V_{CM} is expressed as $(V_{IN+} + V_{IN–})/2$; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

Normal Case 1:	$V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
Normal Case 2:	$V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
Low V_{SENSE} Case 1:	$V_{SENSE} < 20$ mV, -16 V $\leq V_{CM} < 0$
Low V_{SENSE} Case 2:	$V_{SENSE} < 20$ mV, 0 V $\leq V_{CM} \leq V_S$
Low V_{SENSE} Case 3:	$V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by (Equation 1).

$$G = \frac{V_{OUT1} - V_{OUT2}}{100\ mV - 20\ mV} \quad (1)$$

Where:

V_{OUT1} = Output voltage with V_{SENSE} = 100 mV

V_{OUT2} = Output voltage with V_{SENSE} = 20 mV

The offset voltage is then measured at V_{SENSE} = 100 mV and referred to the input (RTI) of the current shunt monitor, as shown in (Equation 2).

$$V_{OS}\text{RTI (Referred−To−Input)} = \left(\frac{V_{OUT1}}{G}\right) - 100\ mV \quad (2)$$

In the Typical Characteristics, the *Output Error vs Common-Mode Voltage* curve shows the highest accuracy for the this region of operation. In this plot, V_S = 12 V; for $V_{CM} \geq 12$ V, the output error is at its minimum. This case is also used to create the $V_{SENSE} \geq 20$ mV output specifications in the Electrical Characteristics table.

Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in the *Output Error vs Common-Mode Voltage* curve. As noted, for this graph V_S = 12 V; for $V_{CM} < 12$ V, the Output Error increases as V_{CM} becomes less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16 V.

Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, -16 V $\leq V_{CM} < 0$; and Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

Although the INA193A is not designed for accurate operation in either of these regions, some applications are exposed to these conditions; for example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA193A. It is important to know what the behavior of the devices will be in these regions.

As V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 300 mV for V_{SENSE} = 0 mV. As V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy as specified in the Electrical Characteristics. Figure 2 illustrates this effect using the INA195A and INA198A (Gain = 100).

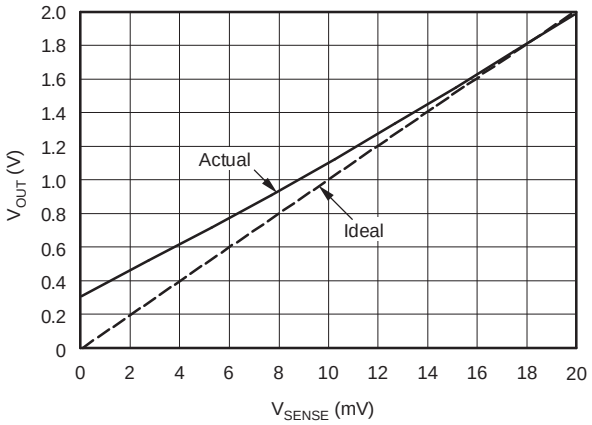
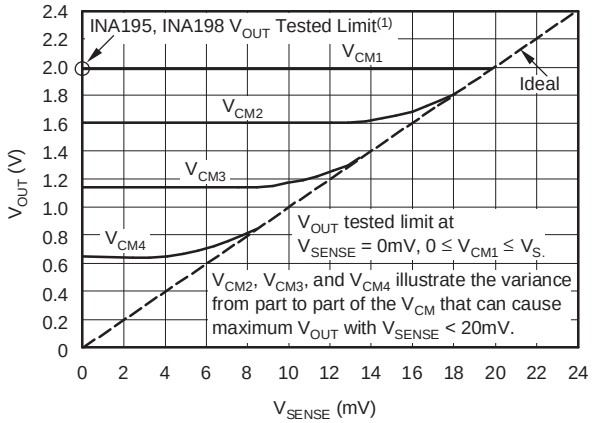


Figure 2. Example for Low V_{SENSE} Cases 1 and 3 (INA195A, INA198A: Gain = 100)

Low V_{SENSE} Case 2: V_{SENSE} < 20 mV, 0 V ≤ V_{CM} ≤ V_S

This region of operation is the least accurate for the INA193A. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2. This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, as V_{SENSE} approaches 20 mV, device operation is closer to that described by Normal Case 2. Figure 3 illustrates this behavior for the INA195A. The V_{OUT} maximum peak for this case is tested by maintaining a constant V_S, setting V_{SENSE} = 0 mV and sweeping V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this test varies from part to part, but the V_{OUT} maximum peak is tested to be less than the specified V_{OUT} tested limit.



NOTE: (1) INA193, INA196 V_{OUT} Tested Limit = 0.4V.
INA194, INA197 V_{OUT} Tested Limit = 1V.

Figure 3. Example for Low V_{SENSE} Case 2 (INA195A, INA198A: Gain = 100)

Shutdown

Because the INA193A consumes a quiescent current less than 1 mA, it can be powered by either the output of logic gates or by transistor switches to supply power. Use a totem pole output buffer or gate that can provide sufficient drive along with 0.1-µF bypass capacitor, preferably ceramic with good high frequency characteristics. This gate should have a supply voltage of 3 V or greater because the INA193A requires a minimum supply greater than 2.7 V. In addition to eliminating quiescent current, this gate also turns off the 10 µA bias current present at each of the inputs. An example shutdown circuit is shown in Figure 4.

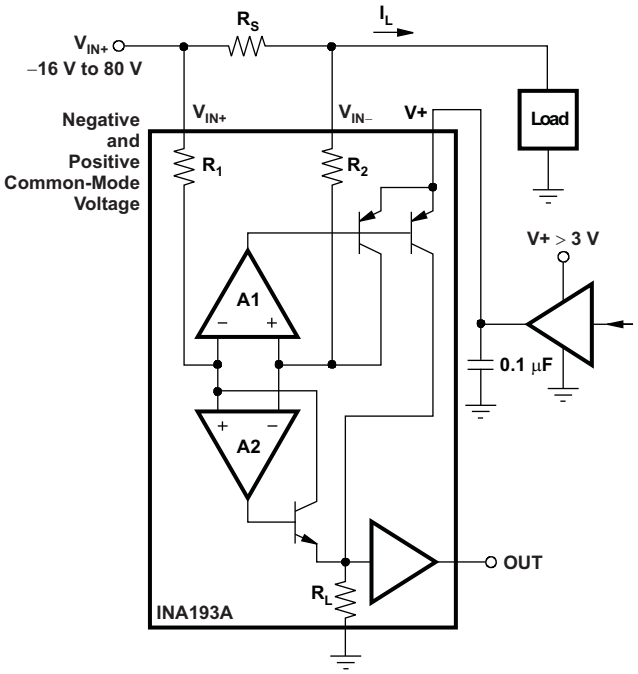


Figure 4. INA193A Example Shutdown Circuit

Selecting R_S

The value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, best performance is attained with an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is 500 mV.

Transient Protection

The –16 V to 80 V common-mode range of the INA193A is ideal for withstanding automotive fault conditions ranging from 12-V battery reversal up to 80-V transients, since no additional protective components are needed up to those levels. In the event that the INA193A is exposed to transients on the inputs in excess of its ratings, then external transient absorption with semiconductor transient absorbers (zeners or Transzorbs) will be necessary. Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA193A to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage due to transient absorber dynamic impedance). Despite the use of internal zener type ESD protection, the INA193A– does not lend itself to using external resistors in series with the inputs since the internal gain resistors can vary up to ±30% (if gain accuracy is not important, then resistors can be added in series with the INA193A inputs with two equal resistors on each input).

Output Voltage Range

The output of the INA193A is accurate within the output voltage swing range set by the power-supply pin, V+. This is best illustrated when using the INA195A or INA198A (which are both versions using a gain of 100), where a 100 mV full-scale input from the shunt resistor requires an output voltage swing of 10 V, and a power-supply voltage sufficient to achieve 10 V on the output.

RFI/EMI

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Small ceramic capacitors placed directly across amplifier inputs can reduce RFI/EMI sensitivity. PCB layout should locate the amplifier as far away as possible from RFI sources. Sources can include other components in the same system as the amplifier itself, such as inductors (particularly switched inductors handling a lot of current and at high frequencies). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. If the amplifier cannot be located away from sources of radiation, shielding may be needed. Twisting wire input leads makes them more resistant to RF fields.

Input Filtering

An obvious and straightforward location for filtering is at the output of the INA193A; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA193A, which is complicated by the internal 5-kΩ + 30% input impedance; this is illustrated in Figure 5. Using the lowest possible resistor values minimizes both the initial shift in gain and effects of tolerance. The effect on initial gain is given by:

$$\text{Gain Error\%} = 100 - \left(100 \times \frac{5\text{k}\,\Omega}{5\text{k}\,\Omega + R_{FILT}}\right) \tag{3}$$

Total effect on gain error can be calculated by replacing the 5-kΩ term with 5 kΩ – 30%, (or 3.5 kΩ) or 5 kΩ + 30% (or 6.5 kΩ). The tolerance extremes of R_{FILT} can also be inserted into the equation. If a pair of 100-Ω 1% resistors are used on the inputs, the initial gain error will be approximately 2%. Worst-case tolerance conditions will always occur at the lower excursion of the internal 5-kΩ resistor (3.5 kΩ), and the higher excursion of R_{FILT} – 3% in this case. Note that the specified accuracy of the INA193A must then be combined in addition to these tolerances. While this discussion treated accuracy worst-case conditions by combining the extremes of the resistor values, it is appropriate to use geometric mean or root sum square calculations to total the effects of accuracy variations.

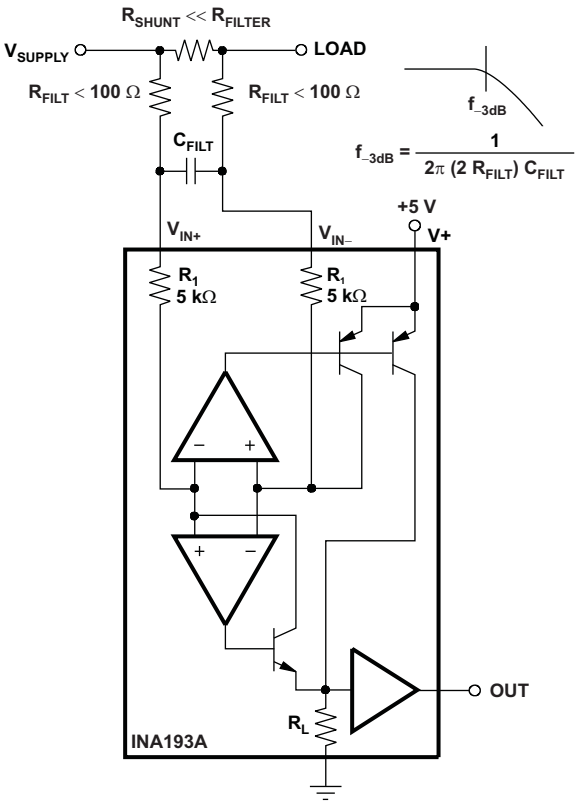


Figure 5. Input Filter (Gain Error – 15% to –2.2%)

Inside the INA193A

The INA193A uses a new, unique internal circuit topology that provides common-mode range extending from –16 V to 80 V while operating from a single power supply. The common-mode rejection in a classic instrumentation amp approach is limited by the requirement for accurate resistor matching. By converting the induced input voltage to a current, the INA193A provides common-mode rejection that is no longer a function of closely matched resistor values, providing the enhanced performance necessary for such a wide common-mode range. A simplified diagram (shown in Figure 6) shows the basic circuit function. When the common-mode voltage is positive, amplifier A2 is active.

The differential input voltage, $(V_{IN+}) – (V_{IN–})$ applied across R_S, is converted to a current through a resistor. This current is converted back to a voltage through R_L, and then amplified by the output buffer amplifier. When the common-mode voltage is negative, amplifier A1 is active. The differential input voltage, $(V_{IN+}) – (V_{IN–})$ applied across R_S, is converted to a current through a resistor. This current is sourced from a precision current mirror whose output is directed into R_L converting the signal back into a voltage and amplified by the output buffer amplifier. Patent-pending circuit architecture ensures smooth device operation, even during the transition period where both amplifiers A1 and A2 are active.

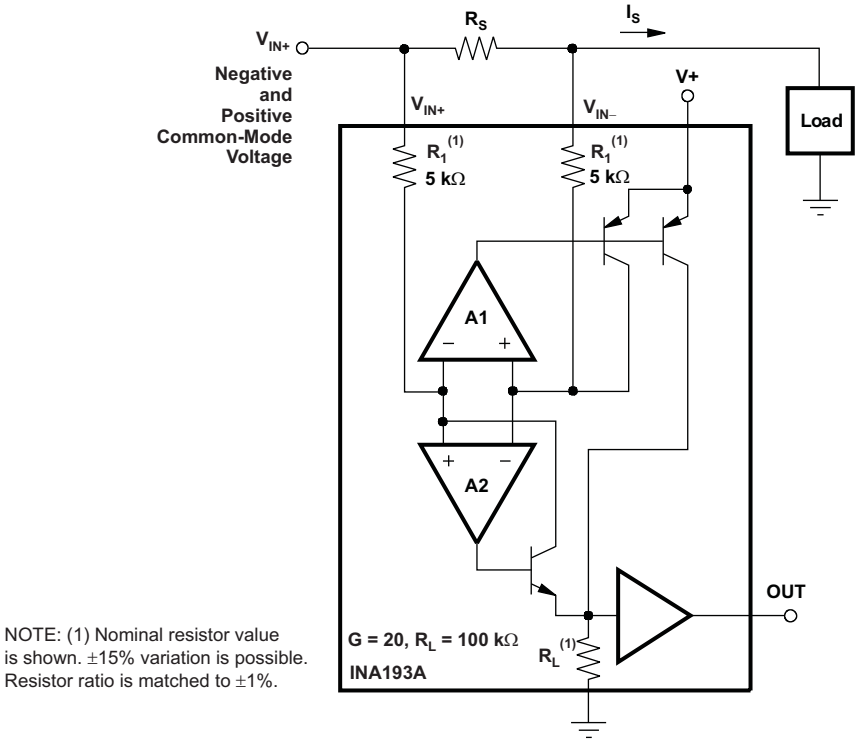


Figure 6. INA193A Simplified Circuit Diagram

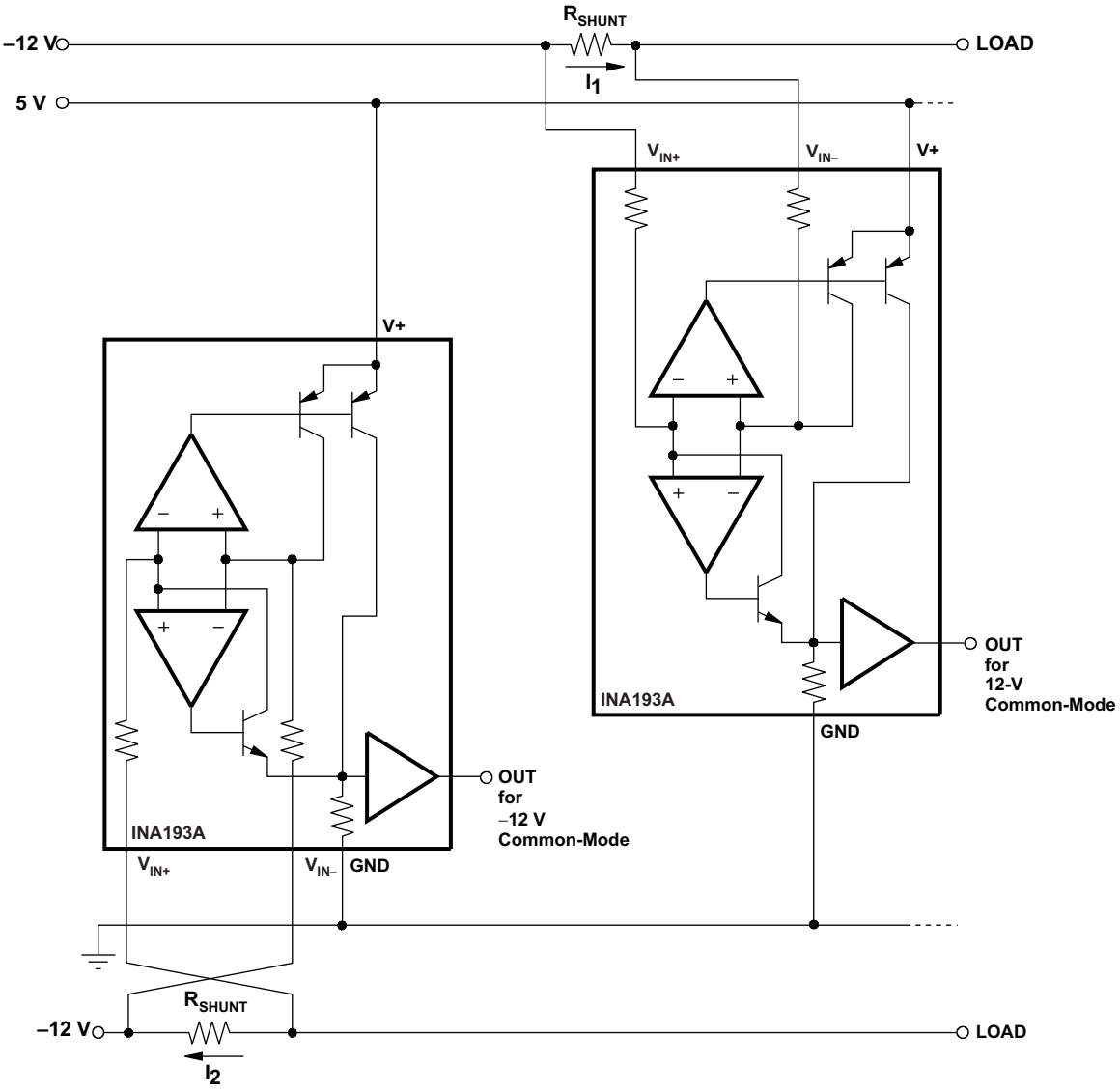


Figure 7. Monitor Bipolar Output Power-Supply Current

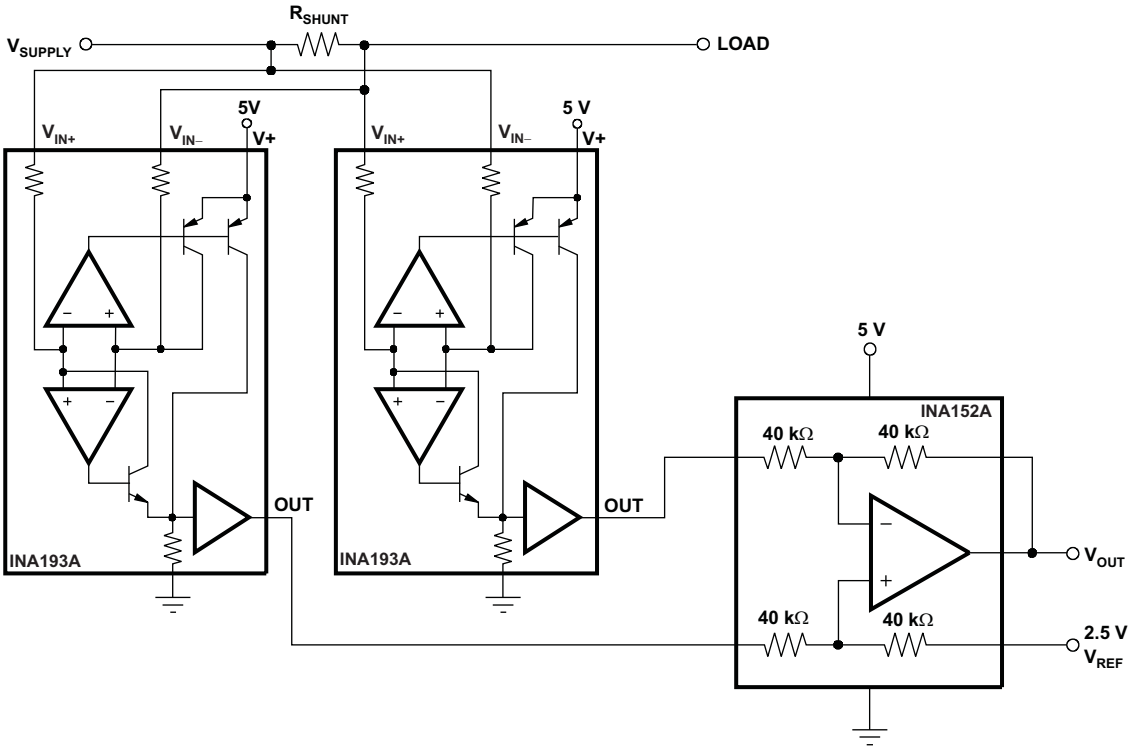


Figure 8. Bidirectional Current Monitoring

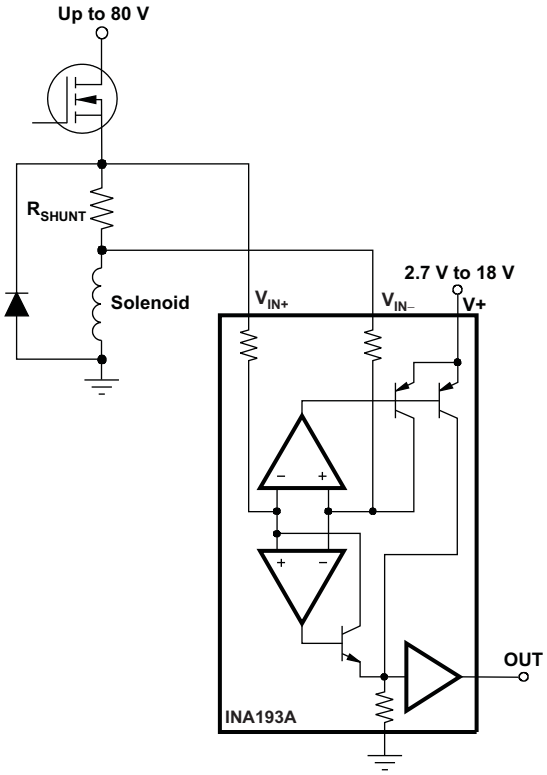


Figure 9. Inductive Current Monitor Including Flyback

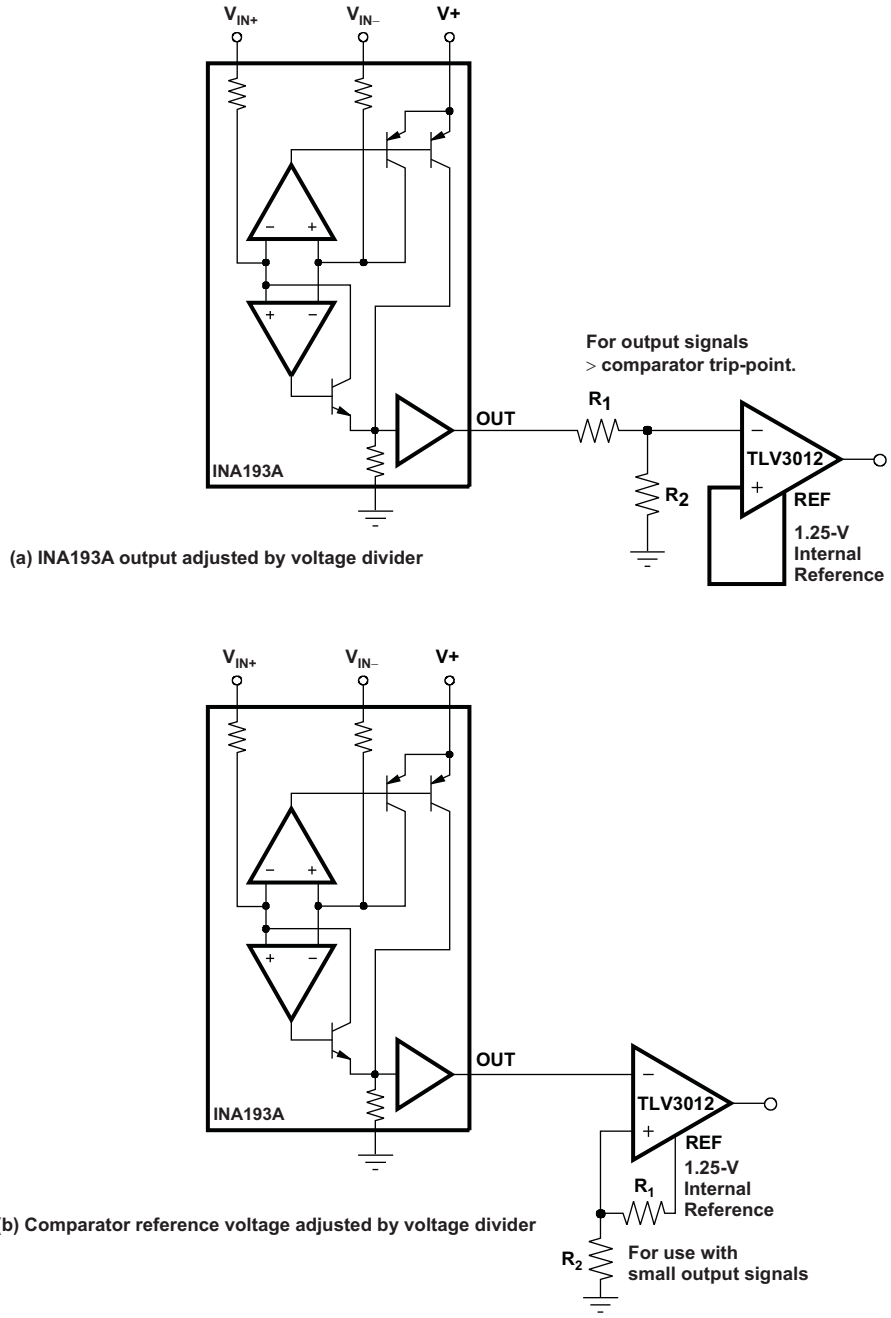


Figure 10. INA193A With Comparator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA193AMDBVREP	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	CCC	Samples
V62/07638-01XE	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	CCC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA193A-EP :

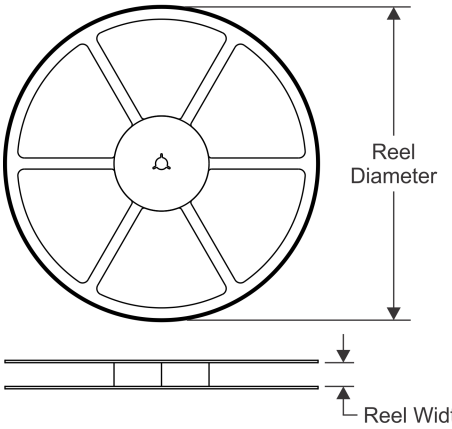
- Automotive: INA193A-Q1

NOTE: Qualified Version Definitions:

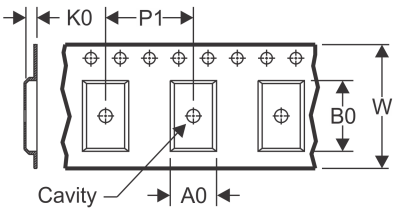
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

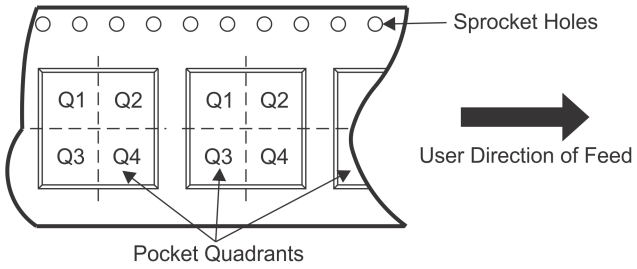


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

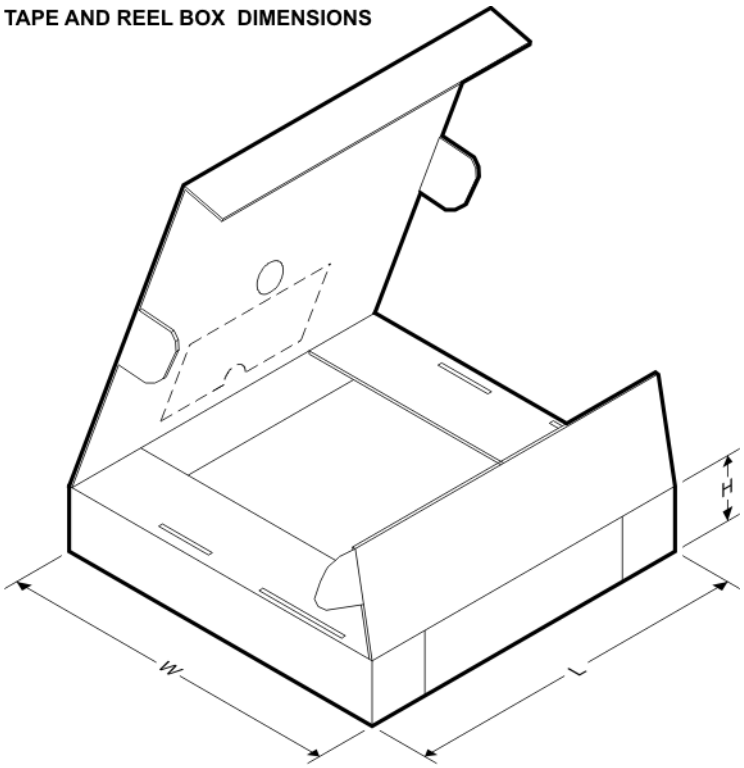
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA193AMDBVREP	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

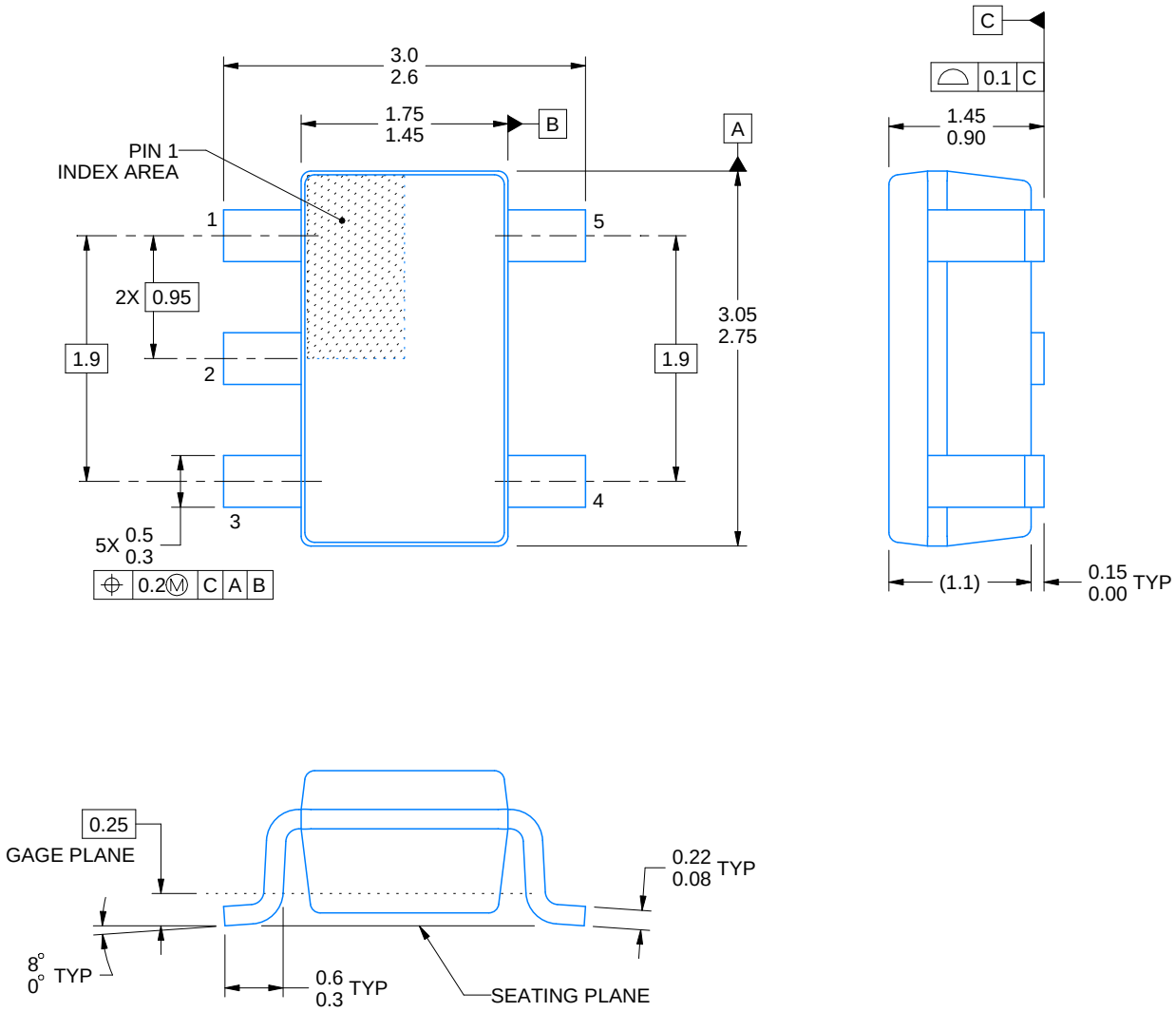
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA193AMDBVREP	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

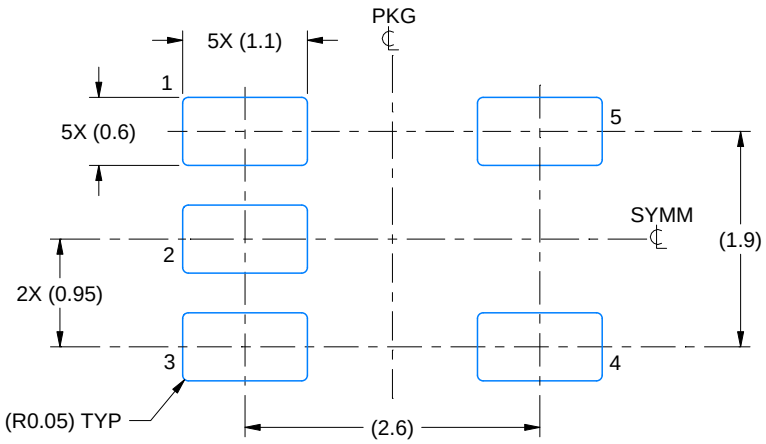
SMALL OUTLINE TRANSISTOR



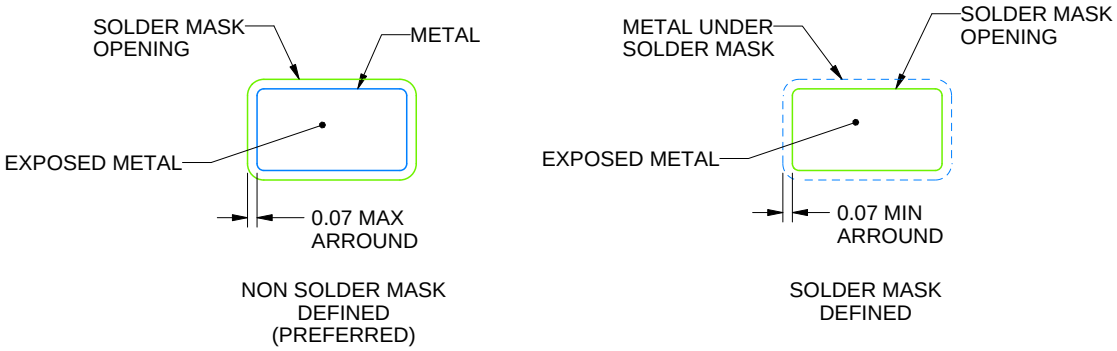
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

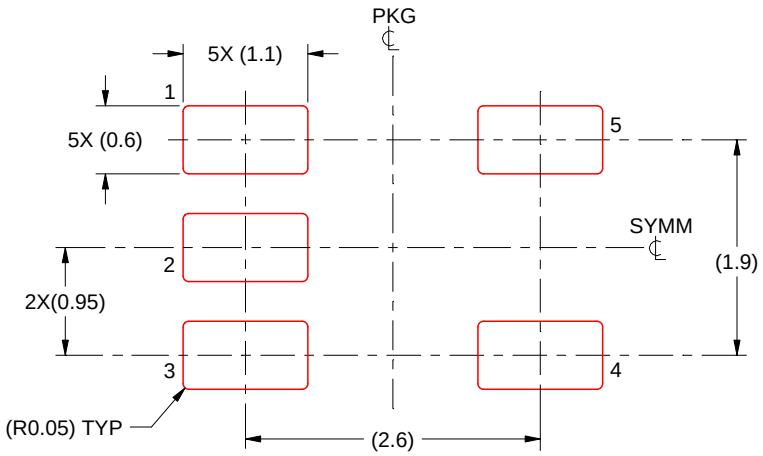


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

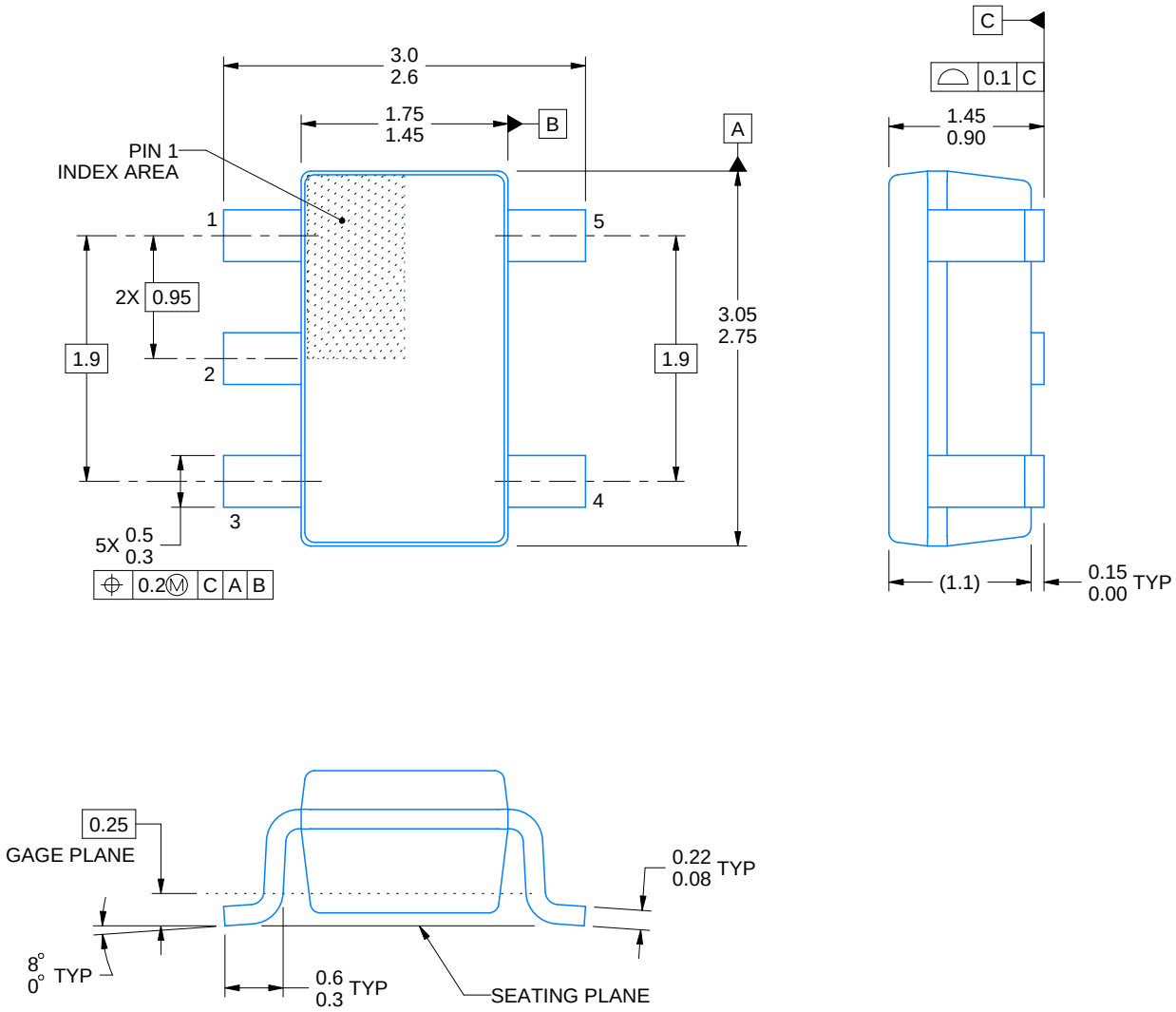
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

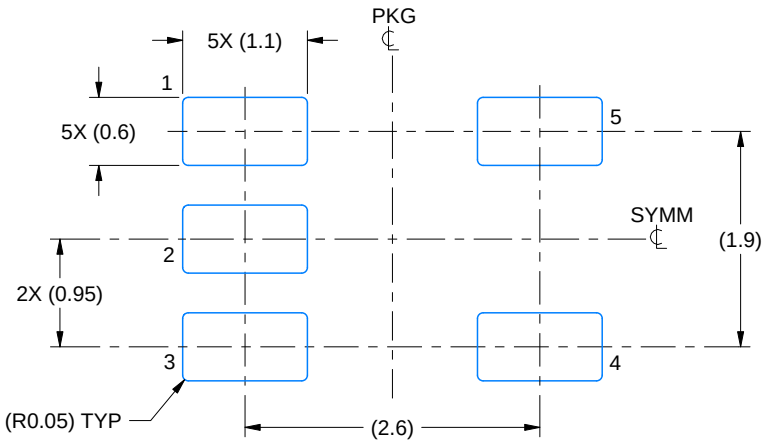
SMALL OUTLINE TRANSISTOR



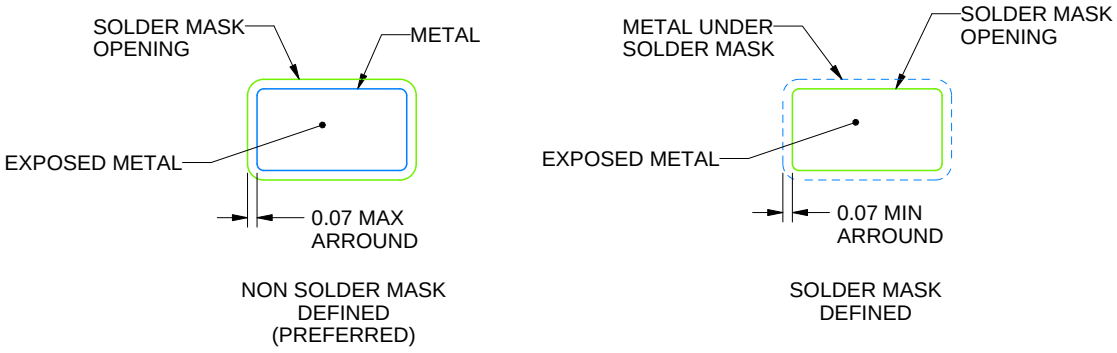
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

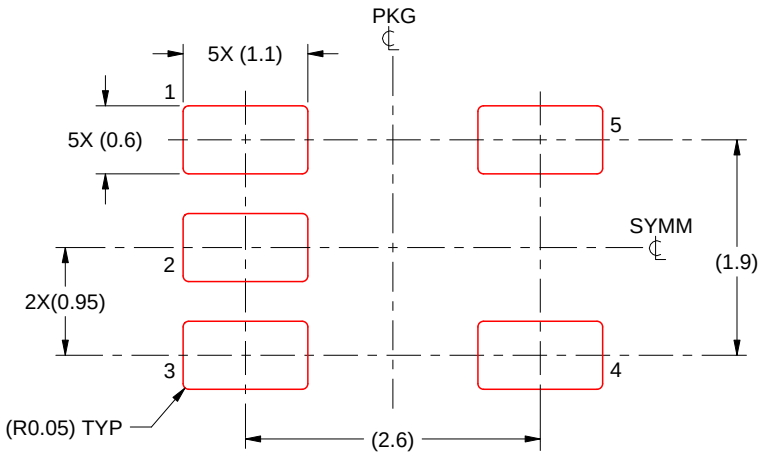


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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