

12A, 650V N-CHANNEL MOSFET

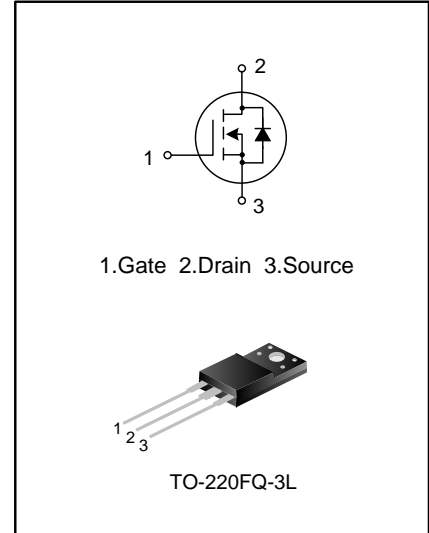
GENERAL DESCRIPTION

SVF12N65FQ is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

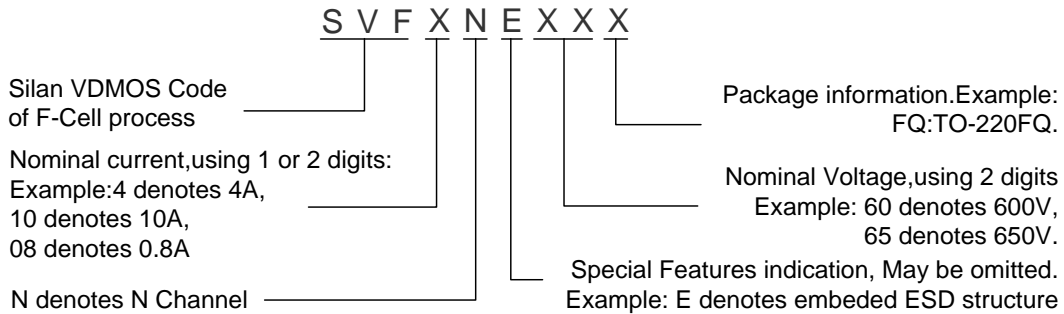
These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 12A,650V, $R_{DS(on)(typ.)}=0.64\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF12N65FQ	TO-220FQ-3L	SVF12N65FQ	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise noted)

Characteristics	Symbol	Ratings		Unit
		SVF12N65FQ		
Drain-Source Voltage	V_{DS}	650		V
Gate-Source Voltage	V_{GS}	± 30		V
Drain Current	I_D	$T_C=25^{\circ}\text{C}$	12	A
		$T_C=100^{\circ}\text{C}$	9	
Drain Current Pulsed	I_{DM}	48		A
Power Dissipation($T_C=25^{\circ}\text{C}$) -Derate above 25°C	P_D	51		W
		0.41		W/ $^{\circ}\text{C}$
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	786		mJ
Operation Junction Temperature Range	T_J	$-55\sim+150$		$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	$-55\sim+150$		$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF12N65FQ		
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.44		$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5		$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650\text{V}, V_{GS}=0\text{V}$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=6.0\text{A}$	--	0.64	0.8	Ω
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V},$ $f=1.0\text{MHZ}$	--	1476	--	pF
Output Capacitance	C_{oss}		--	152	--	
Reverse Transfer Capacitance	C_{rss}		--	4.5	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=325\text{V}, I_D=12\text{A},$ $R_G=25\Omega$ (Note 2,3)	--	37.67	--	ns
Turn-on Rise Time	t_r		--	61.67	--	
Turn-off Delay Time	$t_{d(off)}$		--	80.33	--	
Turn-off Fall Time	t_f		--	46.67	--	
Total Gate Charge	Q_g	$V_{DS}=520\text{V}, I_D=12\text{A},$ $V_{GS}=10\text{V}$ (Note 2,3)	--	24.15	--	nC
Gate-Source Charge	Q_{gs}		--	7.86	--	
Gate-Drain Charge	Q_{gd}		--	7.47	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse p-n Junction	--	--	12	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	48	
Diode Forward Voltage	V_{SD}	$I_S=12A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=12A, V_{GS}=0V,$	--	590.61	--	ns
Reverse Recovery Charge	Q_{rr}	$di_f/dt=100A/\mu S$ (Note 2)	--	5.62	--	μC

Notes:

1. $L=30mH, I_{AS}=6.66A, V_{DD}=140V, R_G=25\Omega,$ starting $T_J=25^\circ C;$
2. Pulse Test: Pulse width $\leq 300\mu s,$ Duty cycle $\leq 2\%;$
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

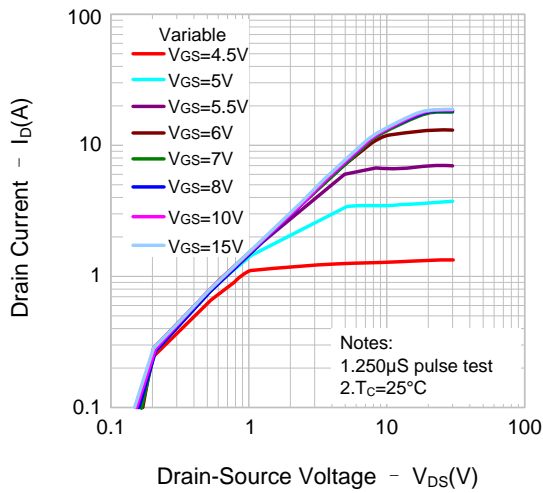


Figure 2. Transfer Characteristics

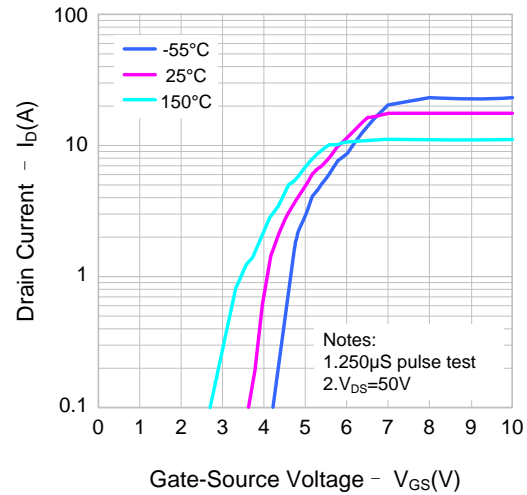


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

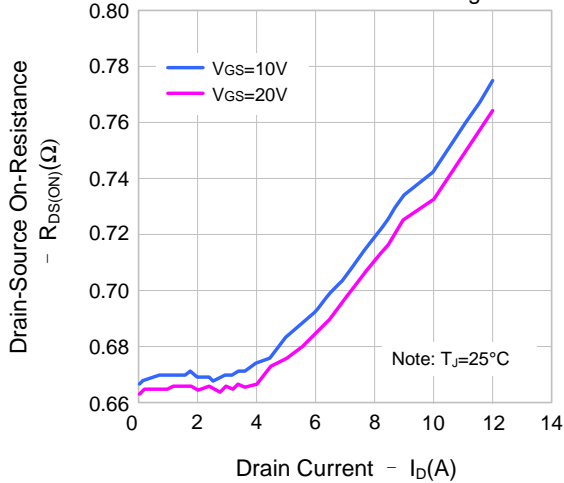
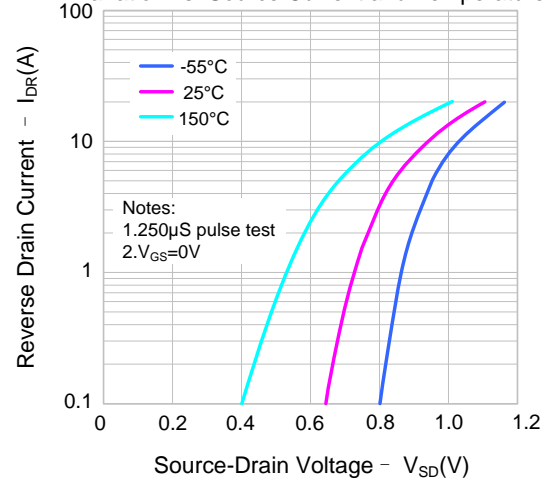


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS(continued)

Figure 5. Capacitance Characteristics

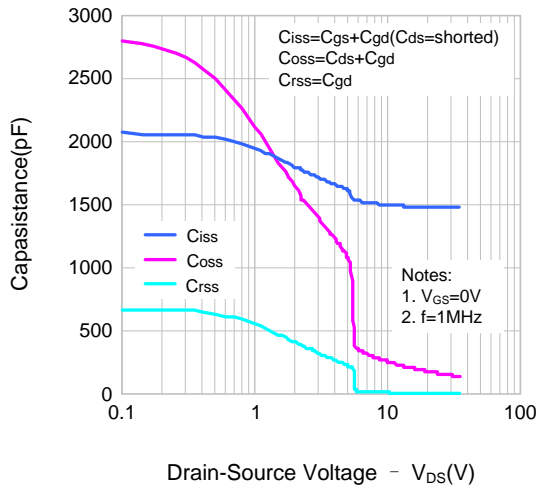


Figure 6. Gate Charge Characteristics

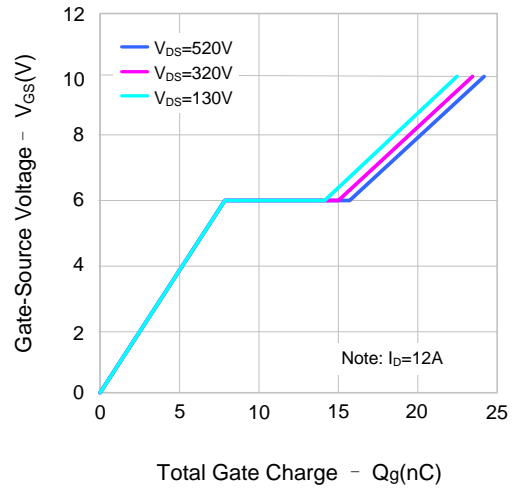


Figure 7. Breakdown Voltage Variation vs. Temperature

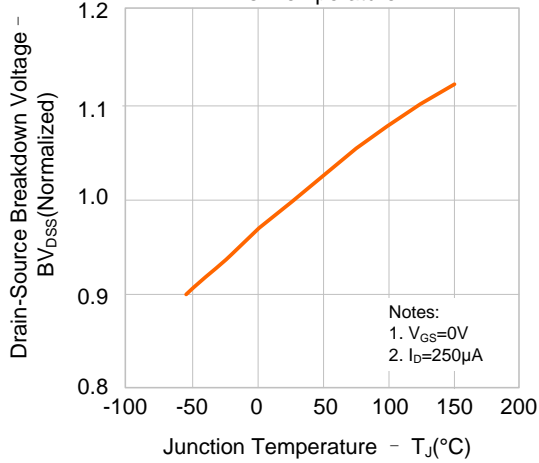


Figure 8. On-resistance Variation vs. Temperature

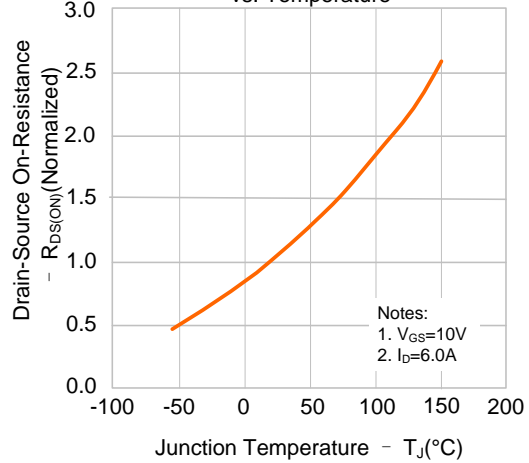


Figure 9. Max. Safe Operating Area

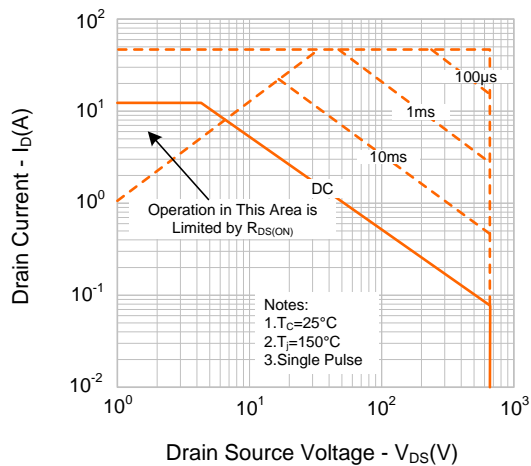
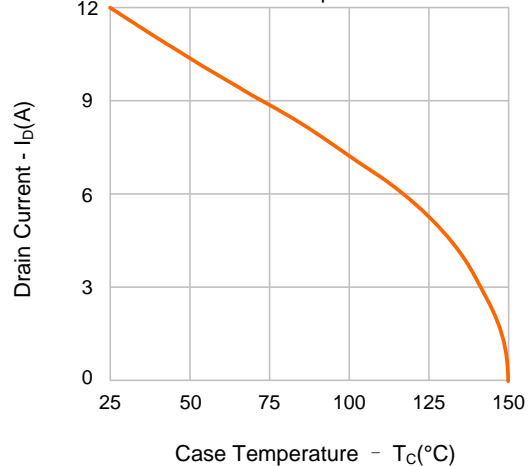
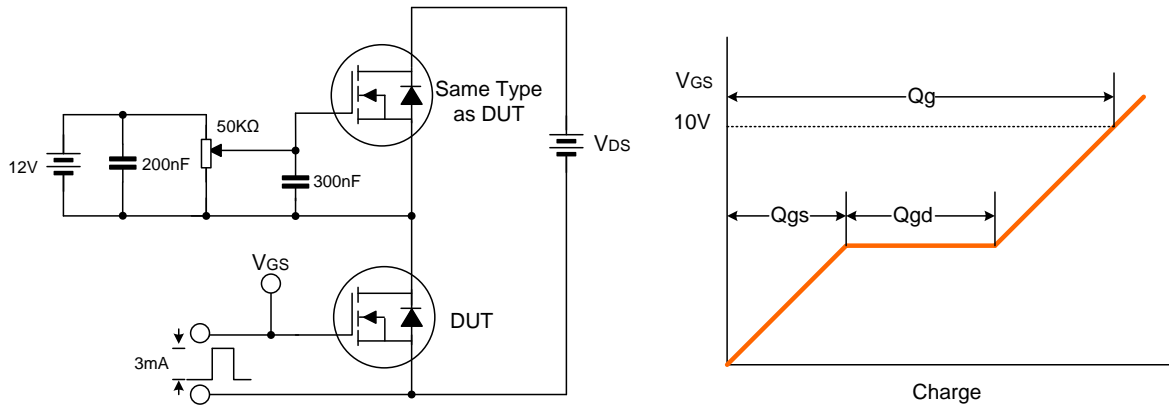


Figure 10. Maximum Drain Current vs. Case Temperature

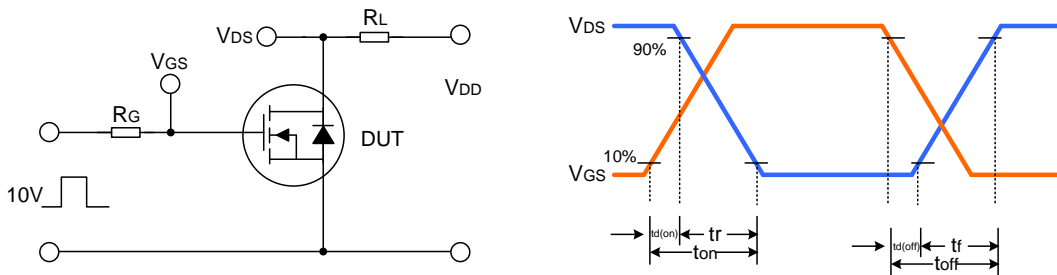


TYPICAL TEST CIRCUIT

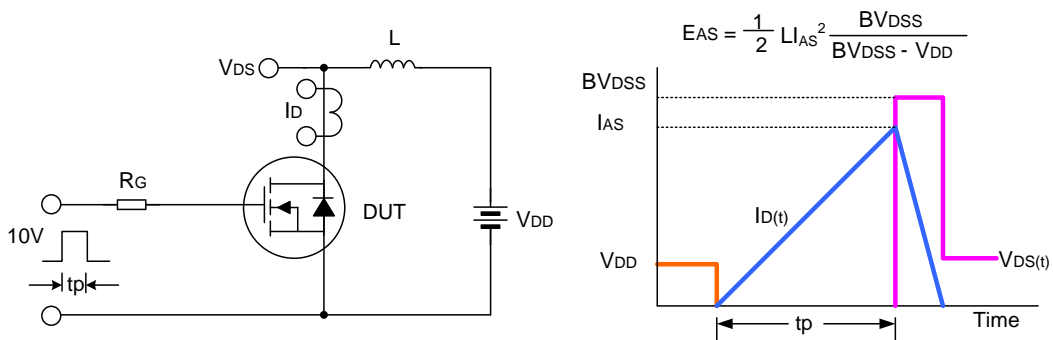
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



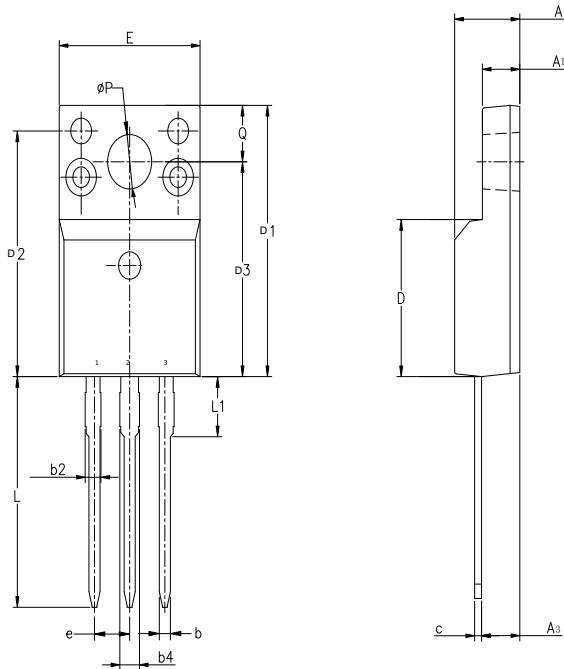
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220FQ-3L

Unit: mm



SYMBOL	MIN	NOM	MAX
A	4.57	4.70	4.83
A1	2.57	2.70	2.83
A3	2.56	2.76	2.93
b	0.76	-	0.90
b2	0.96	-	1.19
b4	1.24	-	1.47
c	0.46	-	0.60
D	8.99	9.19	9.39
D1	15.80	15.87	16.13
D2	14.17	14.37	14.57
D3	12.30	12.57	12.87
E	9.96	10.16	10.36
e	2.54BSC		
L	13.20	13.50	13.70
L1	3.37	3.52	3.67
ϕP	3.08	3.18	3.28
Q	3.20	3.30	3.40

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Rev.: 1.0

Revision History:

1. First release
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