

Small Signal MOSFET

60 V, 380 mA, Single, N-Channel, SOT-23

2N7002K, 2V7002K

Features

- ESD Protected
- Low $R_{DS(on)}$
- Surface Mount Package
- 2V Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Low Side Load Switch
- Level Shift Circuits
- DC-DC Converter
- Portable Applications i.e. DSC, PDA, Cell Phone, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

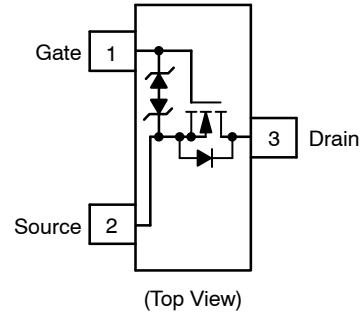
Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Drain Current (Note 1) Steady State 1 sq in Pad	I_D	$T_A = 25^\circ\text{C}$ 380	mA
		$T_A = 85^\circ\text{C}$ 270	
Drain Current (Note 2) Steady State Minimum Pad	I_D	$T_A = 25^\circ\text{C}$ 320	mA
		$T_A = 85^\circ\text{C}$ 230	
Power Dissipation Steady State 1 sq in Pad Steady State Minimum Pad	P_D	420	mW
		300	
Pulsed Drain Current ($t_p = 10 \mu\text{s}$)	I_{DM}	5.0	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	300	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

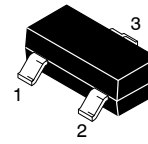
1. Surface-mounted on FR4 board using 1 sq in pad size with 1 oz Cu.
2. Surface-mounted on FR4 board using 0.08 sq in pad size with 1 oz Cu.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	1.6 Ω @ 10 V	380 mA
	2.5 Ω @ 4.5 V	

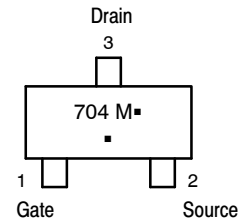
SIMPLIFIED SCHEMATIC



MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23
CASE 318
STYLE 21



- 704 = Specific Device Code*
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)
*Specific Device Code, Date Code or overbar orientation and/or location may vary depending upon manufacturing location. This is a representation only and actual devices may not match this drawing exactly.

ORDERING INFORMATION

Device	Package	Shipping†
2N7002KT1G, 2V7002KT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
2N7002KT7G	SOT-23 (Pb-Free)	3500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

2N7002K, 2V7002K

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	300	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 5$ s (Note 3)		92	
Junction-to-Ambient – Steady State (Note 4)		417	
Junction-to-Ambient – $t \leq 5$ s (Note 4)		154	

3. Surface-mounted on FR4 board using 1 sq in pad size with 1 oz Cu.

4. Surface-mounted on FR4 board using 0.08 sq in pad size with 1 oz Cu.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			71		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0$ V, $V_{DS} = 60$ V	$T_J = 25^{\circ}\text{C}$		1	μA
			$T_J = 125^{\circ}\text{C}$		10	
		$V_{GS} = 0$ V, $V_{DS} = 50$ V	$T_J = 25^{\circ}\text{C}$		100	nA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 10	μA
		$V_{DS} = 0$ V, $V_{GS} = \pm 10$ V			450	nA
		$V_{DS} = 0$ V, $V_{GS} = \pm 5.0$ V			150	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250$ μA	1.0		2.3	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.0		$\text{mV}/^{\circ}\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 500$ mA		1.19	1.6	Ω
		$V_{GS} = 4.5$ V, $I_D = 200$ mA		1.33	2.5	
Forward Transconductance	g_{FS}	$V_{DS} = 5$ V, $I_D = 200$ mA		530		mS

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 20$ V		24.5	45	pF
Output Capacitance	C_{OSS}			4.2	8.0	
Reverse Transfer Capacitance	C_{RSS}			2.2	5.0	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 10$ V; $I_D = 200$ mA		0.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.1		
Gate-to-Source Charge	Q_{GS}			0.3		
Gate-to-Drain Charge	Q_{GD}			0.1		

SWITCHING CHARACTERISTICS, $V_{GS} = V$ (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10$ V, $V_{DD} = 25$ V, $I_D = 500$ mA, $R_G = 25$ Ω		12.2		ns
Rise Time	t_r			9.0		
Turn-Off Delay Time	$t_{d(OFF)}$			55.8		
Fall Time	t_f			29		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = 200$ mA	$T_J = 25^{\circ}\text{C}$		0.8	1.2	V
			$T_J = 85^{\circ}\text{C}$		0.7		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs , duty cycle $\leq 2\%$

6. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

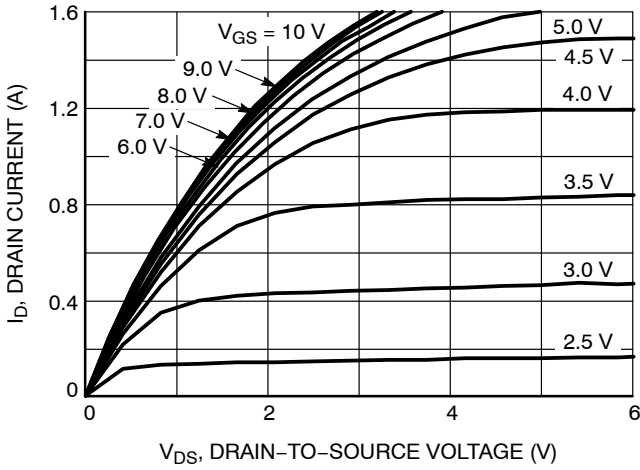


Figure 1. On-Region Characteristics

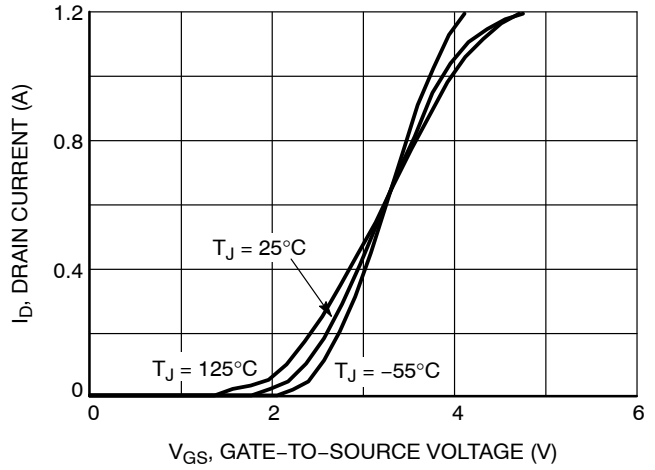


Figure 2. Transfer Characteristics

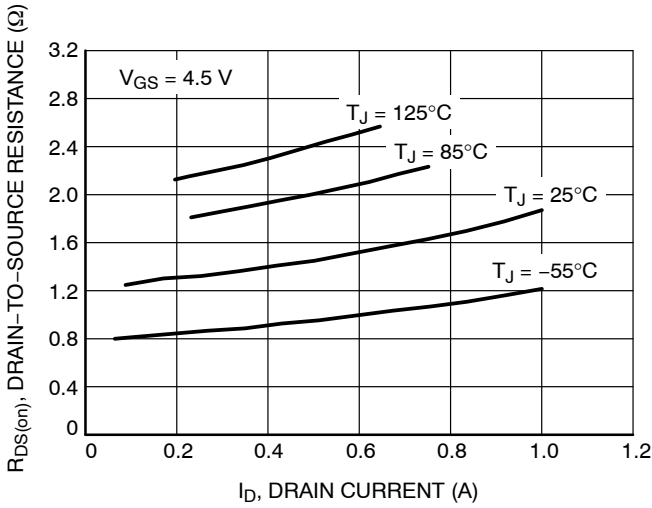


Figure 3. On-Resistance vs. Drain Current and Temperature

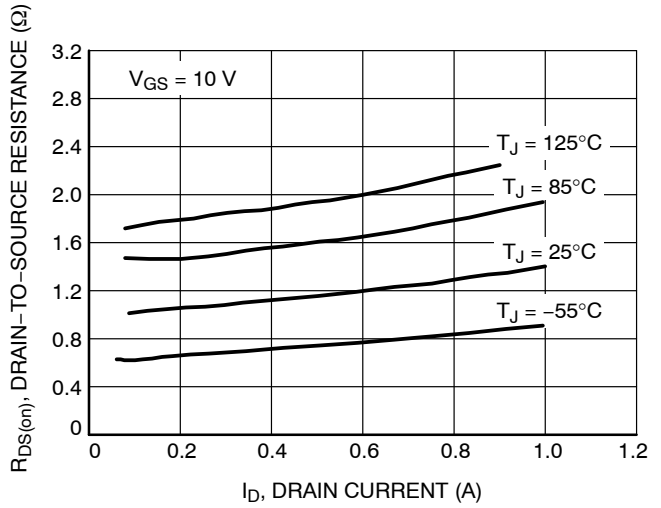


Figure 4. On-Resistance vs. Drain Current and Temperature

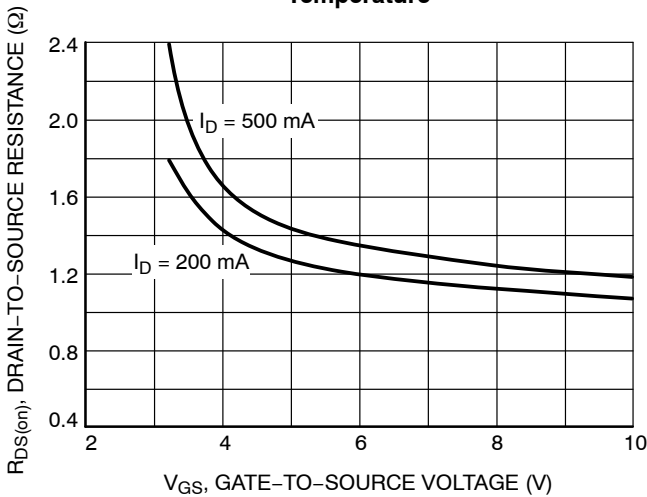


Figure 5. On-Resistance vs. Gate-to-Source Voltage

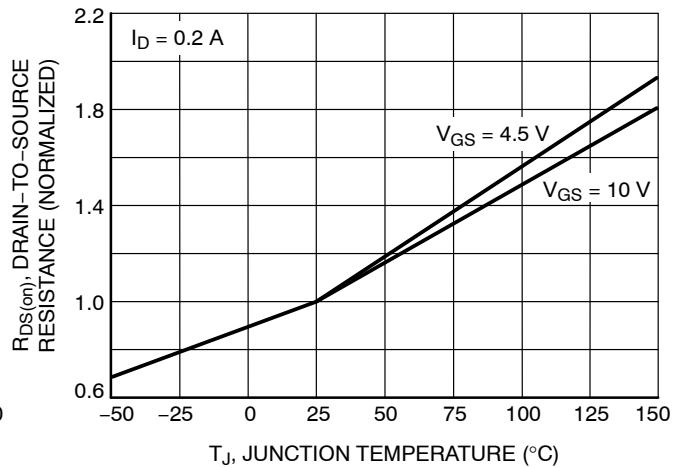


Figure 6. On-Resistance Variation with Temperature

2N7002K, 2V7002K

TYPICAL CHARACTERISTICS

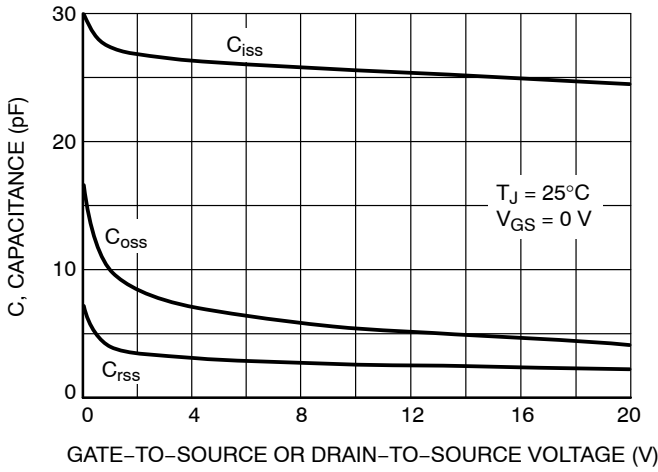


Figure 7. Capacitance Variation

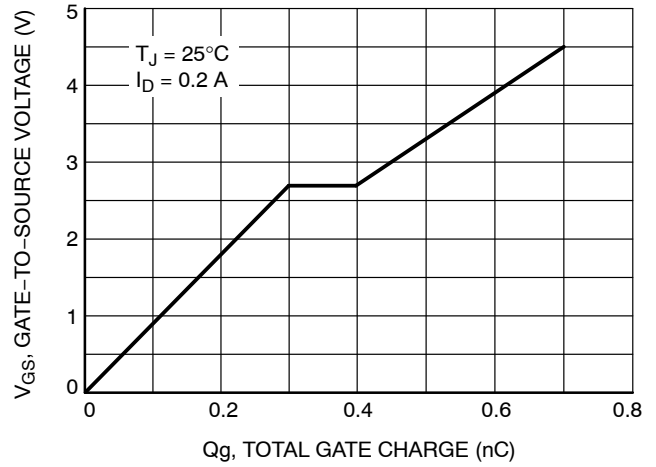


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

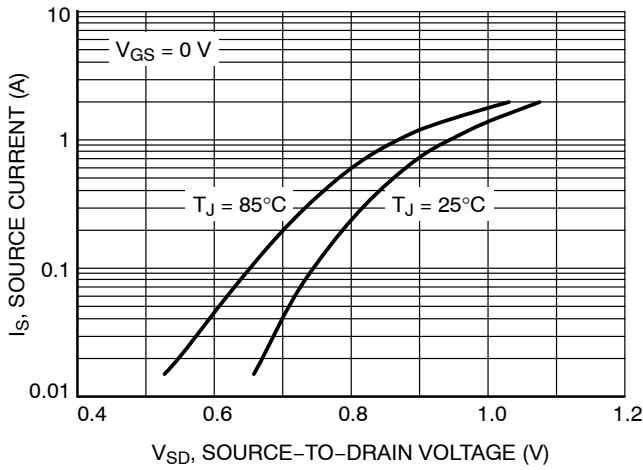


Figure 9. Diode Forward Voltage vs. Current

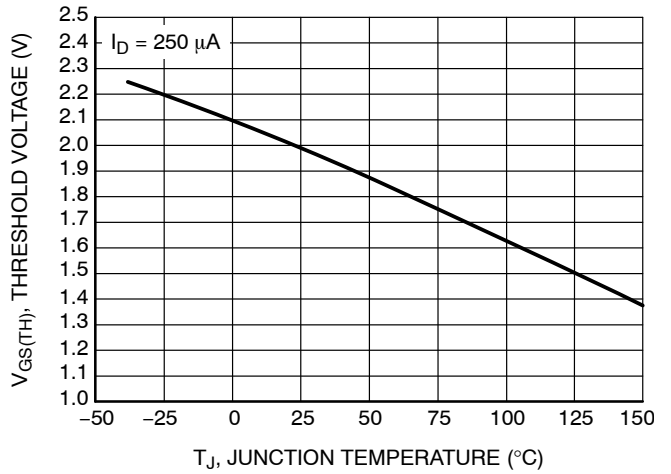


Figure 10. Threshold Voltage with Temperature

2N7002K, 2V7002K

TYPICAL CHARACTERISTICS

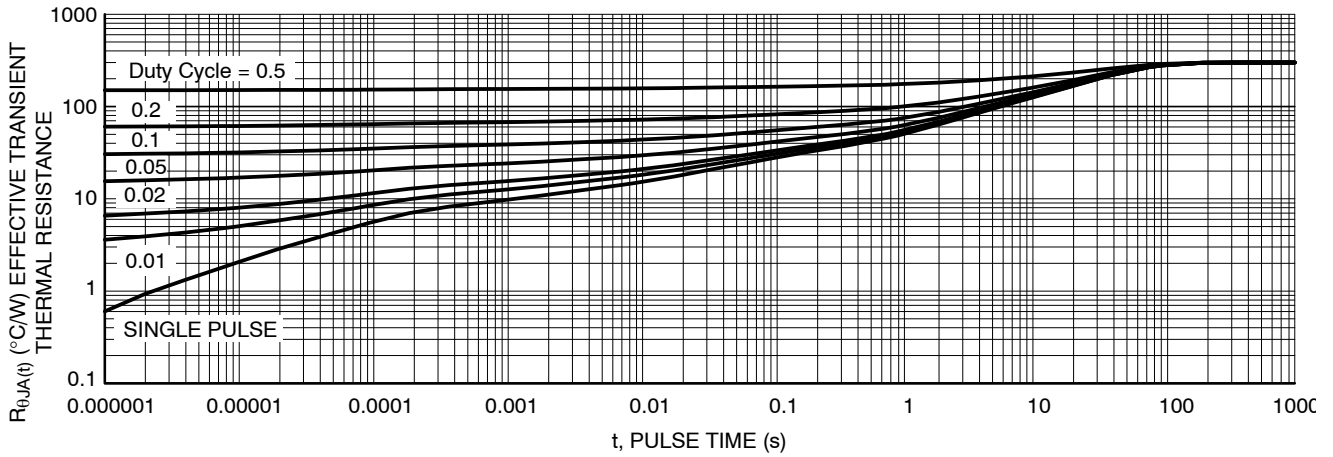


Figure 11. Thermal Response - 1 sq in pad

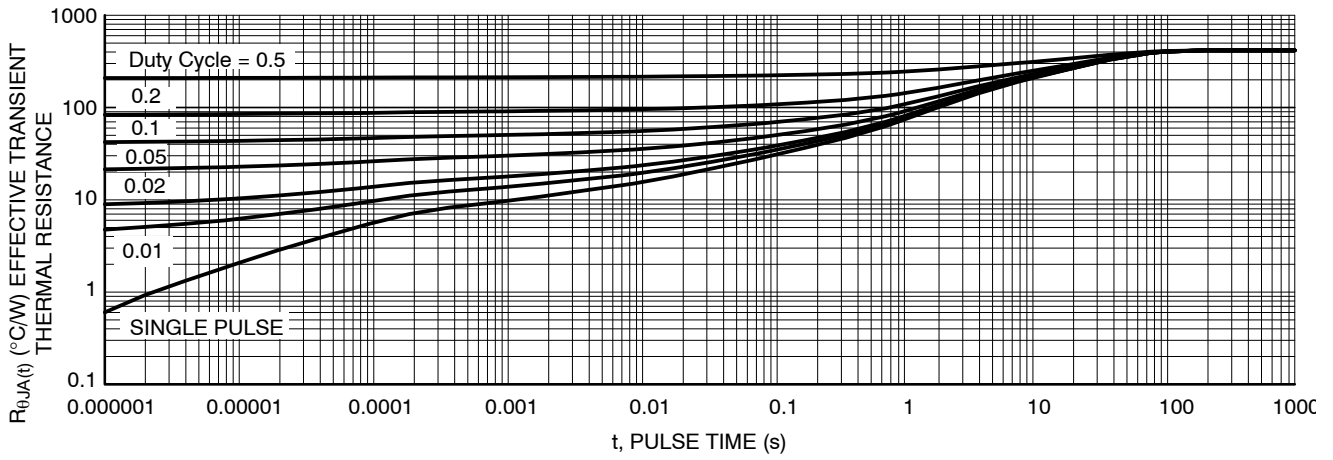


Figure 12. Thermal Response - minimum pad

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SOT-23 (TO-236)
CASE 318-08
ISSUE AS

DATE 30 JAN 2018

SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

RECOMMENDED SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- | | | | | | |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:
CANCELLED | STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE | | |
| STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE | STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE | STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE | STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE |
| STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE | STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE | STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE | STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE | STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE-ANODE | STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE |
| STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT | STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE | STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE | STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION |
| STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE | STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE | | | | |

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