INVENSOM-6UL

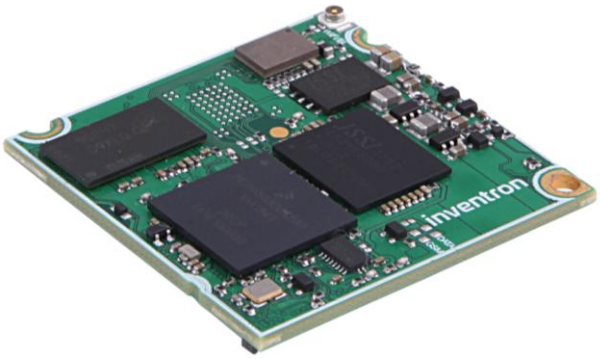
Technical Datasheet

Revision: 1.0

INVENSOM-6UL System on Module (SOM) based on NXP iMX6UL processor is an ultra compact embedded computer for applications that require security, connectivity and high performance. Most demanding technologies like Wi-fi, Bluetooth, 2G, 4G/NBIoT, GNSS are - integrated into one package. Invensom-6UL hardware comes with a proven Linux Board Support Package (BSP) including plug & play security, connectivity and device management drivers. The module delivers high performance with ultra-efficient power management that targets HMI, smart home, EFT-POS, mobile/fixed terminals, industry control, communications, healthcare, wearables and IoT applications. 2x100 pin high speed board-to-board connector carries all functions of the iMx6UL processor to the carrier board. The module supports multiple compatible options of G0, G1, G2, G3 sub family processors and industrial operating temperatures ranging from -40°C to +85°C.

Using INVENSOM-6UL accelerates innovation and reduces time to market. It is production ready and has a proven BSP. Companies can get into the market in 3-6 months for mid-complexity products. Also they can focus more on their product rather than low level hardware and software development.

Inventron offers a full range of customization and support services to its customers including security consultancy (security risk assesment & management, Common Criteria documentation & pre-assessment, etc.), software development, Linux and Android support, carrier board pcb design & production. Customers with tight project schedules or limited resources can benefit from these professional services to save from time and cost.



Product Features:

- Secure Processor NXP i.MX6UL ARM® Cortex®-A7 up to 696MHz
- Integrates Linux, security, NBIoT, EGPRS, Wi-Fi, Bluetooth, GNSS and Ethernet into one stamp size module
- Embedded Linux kernel with plug & play drivers
- Integrated API for security functions like cryptography, mesh, tamper detection, key management, OpenSSL Integration
- Open source application support for fast software development (connectivity, fi-rmware management, IoT protocols, sensor drivers)
- Future ready 4G LTE NBIoT & CAT M1 communication with 2G EGPRS fallback for backup
- Different set of connectivity features can be ordered
- Low power consumption, suitable for battery powered devices
- Linux/Yocto Compatible Board Support Package (BSP)
- Small form factor: 40.2x40.2 mm

1 General Specifications

APPLICATION PROCESSOR	NXP i.MX6UL, ARM® Cortex®-A7, 128 KB L2 cache with NEON™ MPE (Media Processor Engine) co-processor
MEMORY OPTIONS	up to 2 GB NAND flash (SLC)
	up to 1 GB DDR3
	up to 128 MB SPI NOR Flash
	up to 64 GB e-MMC
GRAPHICS	2D Pixel Processing Pipeline (PXP)
LCD	8-/16-/18-/24-bit parallel LCD Display up to WXGA (1366x768)
CAMERA	8/10/16/24-bit Parallel CSI with BT.656 support
SECURITY	ARM TrustZone, Secure Boot (HAB), Hardware cryptographic accelerators (AES 128/256, DES/3DES, SHA-1/224/256, ARCFour, RSA-1024/2048/3072/4096, MD5, HMAC, AES-CMAC, AESXCBC-MAC, AES-CCM),True Random Number Generator (TRNG), e-FUSE (OTP Memory), Secure JTAG, Secure RTC, Secure Non-Volatile Storage, Security State Machine, Master Key Control and Violation, Security Monitor, Zeroizable Secret Key, Secure Time and Monotonic Counter, Active& Passive Tamper Detection, Power Glitch Detectors, Mesh Monitoring, Universal unique ID, Hardware bus encryption, TrustZone Watchdog, RSA4096 DPA Protection
ETHERNET	2x 10/100 Mbit Ethernet MAC + IEEE 1588
USB	2x high speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
EXPENSION CARD:	1x SD/SDIO/MMC (eMMC)
SMART CARD	2x ISO/IEC 7816 (Compatible with EMV Version 4.3)
SERIAL	5x UART, 4x I2C, 3x SPI, 2x CAN
AUDIO	3x I2S, 1xS/PDIF
PWM	8x
ADC	2x 12-bit
KEYPAD	8x8
GPIO	upto 65 pins
JTAG	1x Secure
RTC	1x Secure
TAMPER PINS	5x Active 10x Passive
WATCHDOG	3x
TOUCH SCREEN	1x 4-wire/5-wire touch controller
Wi-Fi (optional)	802.11 b/g/n 65Mbps; Modulation: DSSS / CCK / OFDM, FCC/IC
BLUETOOTH (optional)	V5.1 BR/EDR/LE
4G LTE Cat M1/ NB1 (NB-IoT) (optional)	LTE FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/B26/B28 Cat M1: Max. 375Kbps (DL), Max. 375Kbps (UL) Cat NB1: Max. 32Kbps (DL), Max. 70Kbps (UL)
2G EGPRS (optional)	850/900/1800/1900MHz EDGE: Max. 296Kbps (DL), Max. 236.8Kbps (UL) GPRS: Max. 107Kbps (DL), Max. 85.6Kbps (UL)
GNSS (optional)	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS (with active antenna supply)
ANTENNA	3x IPX U.FL RF Connector (4G/2G, Wi-fi+Bluetooth, GNSS))
OPERATING VOLTAGE	3.6V-4.2V (typ. 3.8V)
OPERATING TEMP.	CT: 0° C to +70° C IT:-30° C to +70° C / -40° C to +85° C (No WiFi)
STORAGE TEMP.	-40° C to +85° C / -50° C to +125° C (No WiFi)
MOUNTING / PIN COUNT	2x100 pin surface mount connector
MECHANICAL DIM.	40.2 mm x 40.2 mm x 5.2 mm

Table 1 – General Specifications

2 Block Diagram

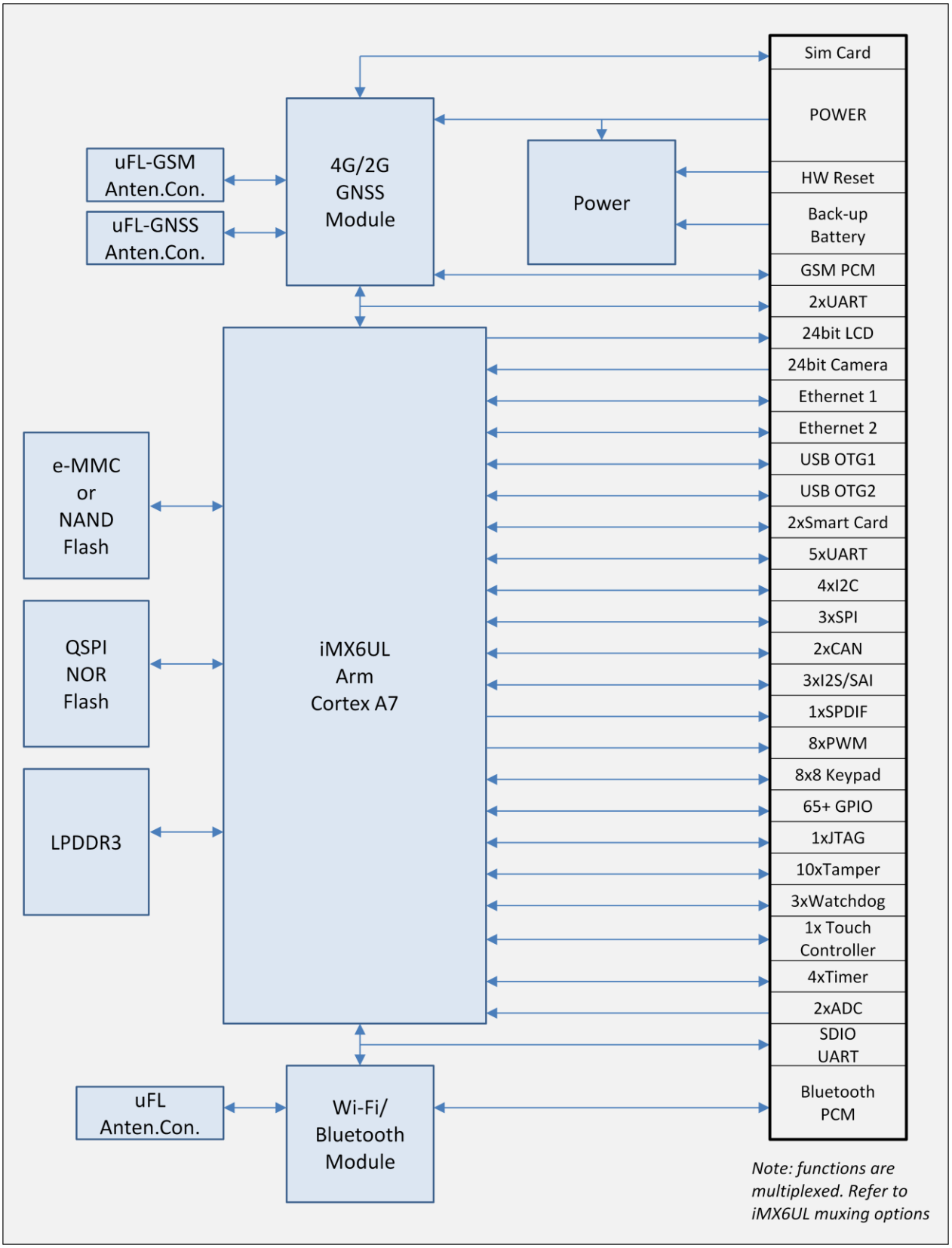


Figure 1 – INVENSOM-6UL Block Diagram

3 Component Placement

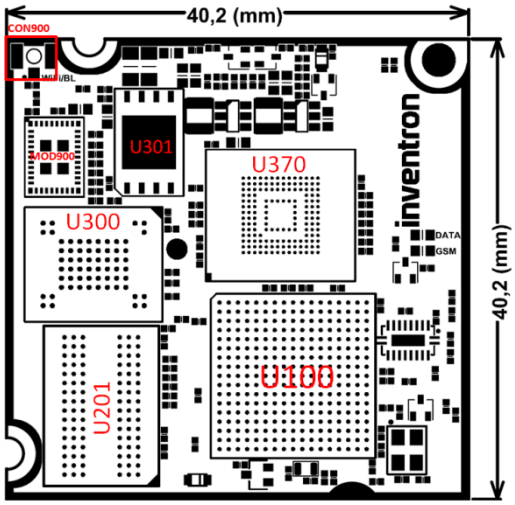


Figure 2 - Top View

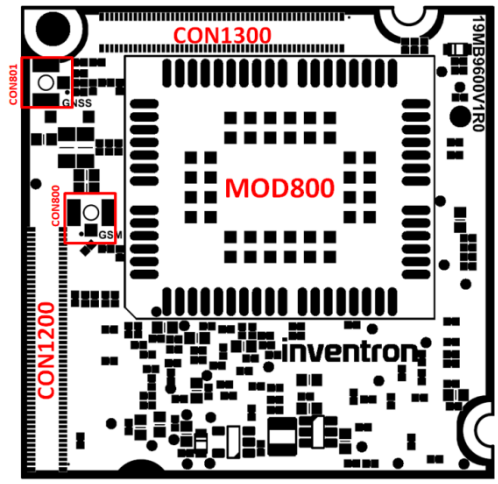


Figure 3 - Bottom View

No	Designator	Part
1	U100	Application Processor
2	U201	DDR3 SDRAM
3	U300	NAND Flash
4	U370	e-MMC
5	U301	QSPI Flash
6	MOD900	Wi-Fi Bluetooth Module
7	CON900	Wi-Fi Bluetooth Antenna Connector
8	MOD800	4G LTE Cat M1/ NB1 (NB-IoT)
9	CON1300	Board-to-board Connector
10	CON1200	Board-to-board Connector
11	CON800	GSM Antenna Connector
12	CON801	GNSS Antenna Connector

Table 2 - Placement of parts on the pcb

4 Board-to-board Connector Pin Description

The following tables describes the signal types an the signals at the INVENSOM-6UL board-to-board connectors. The pins whose name starts with [6UL] notation belongs directly to iMX6UL processor and the alternative functions of these pins can be found on NXP iMX6UL datasheet pin muxing options. Carrier board signal options can be configured by software, hardware or both.

4.1 Types of Signals:

Signal Type	Abbreviation	Notes:
Power Input	PI	
Power Output	PO	Do not exceed given current rating
Battery Input	BAT	

Input	I	
Output	O	
Input/Output	IO	
Open Drain - Input/Output	OD-IO	Needs pull-up to function
Differential Pair	DIF P	90Ω differential impedance required for USB pairs

Table 3 – Signal Types

4.2 Board-to-Board Connector CON1300 Pin Definitions

Pin No	Pin Name	Signal Type	Power Domain	Description	Carrier Board Opt-1	Signal Type Opt-1	Carrier Board Opt-2	Signal Type Opt-2
1	VDD_GNSS[4]	PI	+3.3V	GNSS active antenna power supply	VDD_GNSS	PI		
2	GND	-	-	Ground	GND	-		
3	VDD_GNSS[4]	PI	+3.3V	GNSS active antenna power supply	VDD_GNSS	PI		
4	32K_OSC[2]	I	+3.3V	WiFi/BL external 32kHz sleep clock	32K_OSC	I		
5	GND	-	-	Ground	GND	-		
6	GND	-	-	Ground	GND	-		
7	GND	-	-	Ground	GND	-		
8	+3V_COIN	PI	+3V	+3V back-up battery supply	+3V_COIN	PI		
9	GND	-	-	Ground	GND	-		
10	+3V_COIN	BAT	+3V	+3V back-up battery supply	+3V_COIN	BAT		
11	[6UL]SD1_DATA0[1]	IO	+3.3V	uSDHC1 data 0	SD1_DATA0	IO		
12	GND	-	-	Ground	GND	-		
13	[6UL]SD1_DATA1[1]	IO	+3.3V	uSDHC1 data 1	SD1_DATA1	IO		
14	HW_RST	I	+3.3V	SOM Hardware Reset	HW_RST	I		
15	[6UL]SD1_DATA2[1]	IO	+3.3V	uSDHC1 data 2	SD1_DATA2	IO		
16	POWER_ON	O	+5V	Power on output	PWR_ON	O		
17	[6UL]SD1_DATA3[1]	IO	+3.3V	uSDHC1 data 3	SD1_DATA3	IO		
18	+3V3_OUT	PO	+3.3V	+3.3V powet output max 50 mA	+3V3_OUT	PO		
19	GND	-	-	Ground	GND	-		
20	GND	-	-	Ground	GND	-		
21	[6UL]SD1_CMD[1]	O	+3.3V	uSDHC1 command	SD1_CMD	O		
22	[6UL]UART1_TXD[1]	O	+3.3V	UART1 serial data transmit	UART1_TXD	O		
23	GND	-	-	Ground	GND	-		
24	[6UL]UART1_RXD[1]	I	+3.3V	UART1 serial data receive	UART1_RXD[1]	I		
25	[6UL]SD1_CLK[1]	O	+3.3V	uSDHC1 clock	SD1_CLK	O		
26	[6UL]UART1_CTS[1]	O	+3.3V	UART1 serial clear to send	UART1_CTS	O		
27	GND	-	-	Ground	GND	-		

28	[6UL]UART1_RTS[1]	I	+3.3V	UART1 serial request to send	UART1_RTS	I		
29	BT_PCM_SYNC[2]	IO	+3.3V	Bluetooth PCM sync	BT_PCM_SYNC	IO		
30	GND	-	-	Ground	GND	-		
31	BT_PCM_OUT[2]	O	+3.3V	Bluetooth PCM data output	BT_PCM_OUT	O		
32	[6UL]CSI_DATA07	I	+3.3V	CSI data 7	CSI_DATA7	I	SPI_MISO	IO
33	BT_PCM_CLK[2]	IO	+3.3V	Bluetooth PCM clock	BT_PCM_CLK	IO		
34	[6UL]CSI_DATA06	I	+3.3V	CSI data 6	CSI_DATA6	I	SPI_MOSI	IO
35	BT_PCM_IN[2]	I	+3.3V	Bluetooth PCM data input	BT_PCM_IN	I		
36	[6UL]CSI_DATA05	I	+3.3V	CSI data 5	CSI_DATA5	I	SPI_SS	IO
37	BT_HOST_WAKE[2]	IO	+3.3V	Bluetooth host wake	BT_HOST_WAKE	IO		
38	[6UL]CSI_DATA04	I	+3.3V	CSI data 4	CSI_DATA4	I	SPI_CLK	IO
39	[6UL]LCD_RESET	O	+3.3V	LCD reset	LCD_RESET	O		
40	[6UL]CSI_DATA03	I	+3.3V	CSI data 3	CSI_DATA03	I	SD2_DATA3[5]	IO
41	[6UL]LCD_VSYNC	O	+3.3V	LCD vertical sync	LCD_VSYNC	O		
42	[6UL]CSI_DATA02	I	+3.3V	CSI data 2	CSI_DATA02	I	SD2_DATA2[5]	IO
43	[6UL]LCD_HSYNC	O	+3.3V	LCD horiz.sync	LCD_HSYNC	O		
44	[6UL]CSI_DATA01	I	+3.3V	CSI data 1	CSI_DATA01	I	SD2_DATA1[5]	IO
45	[6UL]LCD_CLK	O	+3.3V	LCD clock	LCD_CLK	O		
46	[6UL]CSI_DATA00	I	+3.3V	CSI data 0	CSI_DATA00	I	SD2_DATA0[5]	IO
47	[6UL]LCD_ENABLE	O	+3.3V	LCD enable	LCD_ENABLE	O		
48	GND	-	-	Ground	GND	-		-
49	GND	-	-	Ground	GND	-		-
50	[6UL]CSI_VSYNC	I	+3.3V	CSI vertical sync	CSI_VSYNC	I	SD2_CLK[5]	O
51	[6UL]LCD_DATA00	O	+3.3V	LCD data 0	LCD_DATA00	O		
52	[6UL]CSI_HSYNC	I	+3.3V	CSI horizontal sync	CSI_HSYNC	I	SD2_CMD[5]	O
53	[6UL]LCD_DATA01	O	+3.3V	LCD data 1	LCD_DATA01	O		
54	[6UL]CSI_PIXCLK	I	+3.3V	CSI pixel clock	CSI_PIXCLK	I	I2C1_SCL	OD-IO
55	[6UL]LCD_DATA02	O	+3.3V	LCD data 2	LCD_DATA02	O		
56	[6UL]CSI_MCLK	O	+3.3V	CSI master clock	CSI_MCLK	O	I2C1_SDA	OD-IO
57	[6UL]LCD_DATA03	O	+3.3V	LCD data 3	LCD_DATA03	O		
58	GND	-	-	Ground	GND	-		
59	[6UL]LCD_DATA04	O	+3.3V	LCD data 4	LCD_DATA04	O		
60	WL_HOST_WAKE[2]	IO	+3.3V	Wifi GPIO_0	WL_HOST_WAKE	IO		
61	[6UL]LCD_DATA05	O	+3.3V	LCD data 5	LCD_DATA05	O		
62	BT_DEV_WAKE[2]	IO	+3.3V	BT device wake	BT_DEV_WAKE	IO		
63	[6UL]LCD_DATA06	O	+3.3V	LCD data 6	LCD_DATA06	O		
64	[6UL]GPIO1_IO04[1]	IO	+3.3V	GPIO1_4	GPIO1_4	IO		
65	[6UL]LCD_DATA07	O	+3.3V	LCD data 7	LCD_DATA07	O		
66	[6UL]GPIO1_IO01	IO	+3.3V	GPIO1_1	I2C1_SDA	OD-IO		
67	[6UL]LCD_DATA08	O	+3.3V	LCD data 8	LCD_DATA08	O		
68	[6UL]GPIO1_IO00	IO	+3.3V	GPIO1_0	I2C1_SCL	OD-IO		
69	[6UL]LCD_DATA09	O	+3.3V	LCD data 9	LCD_DATA09	O		

70	W_DISABLE#[4]	I	+1.8V	GSM airplane mode control	W_DISABLE#	I		
71	[6UL]LCD_DATA10	O	+3.3V	LCD data 10	LCD_DATA10	O		
72	GSM_NETLIGHT[4]	O	+1.8V	GSM network activity status	GSM_NETLIGHT	O		
73	[6UL]LCD_DATA11	O	+3.3V	LCD data 11	LCD_DATA11	O		
74	[6UL]GPIO1_IO08[2]	IO	+3.3V	GPIO1_8	GPIO1_8	IO		
75	[6UL]LCD_DATA12	O	+3.3V	LCD data 12	LCD_DATA12	O		
76	GSM_RST[4]	I	+3.3V	GSM reset	GSM_RST	I		
77	[6UL]LCD_DATA13	O	+3.3V	LCD data 13	LCD_DATA13	O		
78	PSM_IND_GSM[4]	O	+1.8V	GSM power saving mode indicator	PSM_IND_GSM	O		
79	[6UL]LCD_DATA14	O	+3.3V	LCD data 14	LCD_DATA14	O		
80	GND	-	-	Ground	GND	-		
81	[6UL]LCD_DATA15	O	+3.3V	LCD data 15	LCD_DATA15	O		
82	I2C_SCL_GSM[4]	OD-IO	+1.8V	GSM audio codec I2C serial clock.	I2C_SCL_GSM	OD-IO		
83	[6UL]LCD_DATA16	O	+3.3V	LCD data 16	LCD_DATA16	O		
84	I2C_SDA_GSM[4]	OD-IO	+1.8V	GSM audio codec I2C serial data	I2C_SDA_GSM	OD-IO		
85	[6UL]LCD_DATA17	O	+3.3V	LCD data 17	LCD_DATA17	O		
86	GND	-	-	Ground	GND	-		
87	[6UL]LCD_DATA18	O	+3.3V	LCD data 18	LCD_DATA18	O	SD2_CMD[5]	O
88	SIM_PRESENCE[4]	I	+1.8V	GSM SIM card insertion detection	SIM_PRESENCE	I		
89	[6UL]LCD_DATA19	O	+3.3V	LCD data 19	LCD_DATA19	O	SD2_CLK[5]	O
90	SIM_VDD[4]	PO	+3V or +1.8V	GSM Power supply of SIM card	SIM_VDD	PO		
91	[6UL]LCD_DATA20	O	+3.3V	LCD data 20	LCD_DATA20	O	SD2_DATA0[5]	IO
92	SIM_RST[4]	O	+3V or +1.8V	GSM Reset signal of SIM card	SIM_RST	O		
93	[6UL]LCD_DATA21	O	+3.3V	LCD data 21	LCD_DATA21	O	SD2_DATA1[5]	IO
94	SIM_DATA[4]	IO	+3V or +1.8V	GSM Data signal of SIM card	SIM_DATA	IO		
95	[6UL]LCD_DATA22	O	+3.3V	LCD data 22	LCD_DATA22	O	SD2_DATA2[5]	IO
96	SIM_CLK[4]	O	+3V or +1.8V	GSM Clock signal of SIM card	SIM_CLK	O		
97	[6UL]LCD_DATA23	O	+3.3V	LCD data 23	LCD_DATA23	O	SD2_DATA3[5]	IO
98	SIM_GND[4]	-	-	GSM Ground of SIM card	SIM_GND	-		-
99	GND	-	-	Ground	GND	-		
100	GND	-	-	Ground	GND	-		

Notes :

[1] These signals are used by Wifi/BL module. If Wifi/BL module is not assembled on the SOM, these signals can be used as given in the carrier board options. Otherwise these pins should be left open.

[2] If Wifi/BL module is assembled on the SOM, these signals have the given function. Otherwise the pin has no function.

[3] These signals are used by 4G/2G/GNSS module. If 4G/2G/GNSS module is not assembled on the SOM, these signals can be used as given in the carrier board options. Otherwise these pins should be left open.

[4] If 4G/2G/GNSS module is assembled on the SOM, these signals have the given function. Otherwise the pin has no function.

[5] These signals are used by e-MMC. If e-MMC is not assembled on the SOM, these signals can be used as given in the carrier board options. Otherwise these pins should be left open.

Table 4 – CON1300 pin definitions

4.3 Board-to-Board Connector CON1200 Pin Definitions

Pin No	Pin Name	Signal Type	Power Domain	Description	Carrier Board Opt-1	Signal Type Opt-1	Carrier Board Opt-2	Signal Type Opt-2
101	[6UL]BOOT_MODE1	I	SNVS	Boot mode input 1	BOOT_MODE1	I		
102	[6UL]BOOT_MODE0	I	SNVS	Boot mode input 0	BOOT_MODE0	I		
103	[6UL]CCM_PMIC_STBY_REQ	O	SNVS	PMIC Standby Request	PMIC_STBY REQ	O		
104	[6UL]GPIO1_IO05	IO	+3.3V	GPIO1_5	USB_OTG2_UID	I		
105	[6UL]SNVS_PMIC_ON_REQ	O	SNVS	PMIC On Request	PMIC_ON_REQ	O		
106	[6UL]GPIO1_IO03	IO	+3.3V	GPIO1_3	ENET1_nINT	I		
107	[6UL]ONOFF	I	SNVS	i.MX6UL ONOFF Button signal	ONOFF	I		
108	[6UL]GPIO1_IO02	IO	+3.3V	GPIO1_2	GPIO expander interrupt	I		
109	[6UL]POR_B	O	SNVS	i.MX6UL Reset input	POR_B	O		
110	[6UL]GPIO1_IO09	IO	+3.3V	GPIO1_9	ADC or PWM or GPIO	IO		
111	[6UL]SNVS_TAMPER0[6]	IO	SNVS or +3.3V	Tamper detection pin 0	TAMPER0	IO	GPIO5_IO00	IO
112	[6UL]USB_OTG2_VBUS	PI	+5V	USB OTG2 VBUS input	USB_OTG2_VBUS	PI		
113	[6UL]SNVS_TAMPER1[6]	IO	SNVS or +3.3V	Tamper detection pin 1	TAMPER1	IO	GPIO5_IO01	IO
114	GND	-	-	Ground	GND	-		
115	[6UL]SNVS_TAMPER2[6]	IO	SNVS or +3.3V	Tamper detection pin 2	TAMPER2	IO	GPIO5_IO02	IO
116	[6UL]USB_OTG1_VBUS	PI	+5V	USB OTG1 VBUS input	USB_OTG1_VBUS	PI		
117	[6UL]SNVS_TAMPER3[6]	IO	SNVS or +3.3V	Tamper detection pin 3	TAMPER3	IO	GPIO5_IO03	IO
118	GND	-	-	Ground	GND	-		
119	[6UL]SNVS_TAMPER4[6]	IO	SNVS or +3.3V	Tamper detection pin 4	TAMPER4	IO	GPIO5_IO04	IO
120	[6UL]USB_OTG1_D_N	DIF P	-	USB OTG1 data-	USB_OTG1_D_N	DIF P		
121	[6UL]SNVS_TAMPER5[6]	IO	SNVS or +3.3V	Tamper detection pin 5	TAMPER5	IO	GPIO5_IO05	IO
122	[6UL]USB_OTG1_D_P	DIF P	-	USB OTG1 data+	USB_OTG1_D_P	DIF P		
123	[6UL]SNVS_TAMPER6[6]	IO	SNVS or +3.3V	Tamper detection pin 6	TAMPER6	IO	GPIO5_IO06	IO
124	GND	-	-	Ground	GND	-		
125	[6UL]SNVS_TAMPER7[6]	IO	SNVS or +3.3V	Tamper detection pin 7	TAMPER7	IO	GPIO5_IO07	IO
126	[6UL]USB_OTG2_D_N	DIF P	-	USB OTG2 data-	USB_OTG2_D_N	DIF P		
127	[6UL]SNVS_TAMPER8[6]	IO	+3.3V	Tamper detection pin 8	TAMPER8	IO	GPIO5_IO08	IO
128	[6UL]USB_OTG2_D_P	DIF P	-	USB OTG2 data+	USB_OTG2_D_P	DIF P		
129	[6UL]SNVS_TAMPER9[6]	IO	SNVS or +3.3V	Tamper detection pin 9	TAMPER9	IO	GPIO5_IO09	IO
130	[6UL]VDDA_ADC_3P3	PI	+3.3V	ADC reference power input	+3V3_ADC	PI		

131	GND	-	-	Ground	GND	-		
132	[6UL]UART3_CTS	O	+3.3V	UART3 serial clear to send	CAN1_TX	O		
133	[6UL]JTAG_TMS	I	+3.3V	JTAG TMS	SAI2_MCLK	O	JTAG_TMS	I
134	[6UL]UART3_RTS	I	+3.3V	UART3 serial request to send	CAN2_RX	I		
135	[6UL]JTAG_MOD	I	+3.3V	JTAG MOD	-	-	JTAG_MOD	I
136	[6UL]UART2_CTS	O	+3.3V	UART2 serial clear to send	CAN2_TX	O		
137	[6UL]JTAG_TRST_B	I	+3.3V	JTAG TRST	SAI2_TX	O	JTAG_TRST_B	I
138	[6UL]UART2_RTS	I	+3.3V	UART2 serial request to send	CAN2_RX	I		
139	[6UL]JTAG_TDO	O	+3.3V	JTAG TDO	SAI2_SYNC	IO	JTAG_TDO	O
140	[6UL]GPIO1_IO06	IO	+3.3V	GPIO1_6	ENET1_MDIO	IO		
141	[6UL]JTAG_TDI	I	+3.3V	JTAG TDI	SAI2_BCLK	IO	JTAG_TDI	I
142	[6UL]GPIO1_IO07	IO	+3.3V	GPIO1_7	ENET1_MDC	O		
143	[6UL]JTAG_TCK	I	+3.3V	JTAG TCK	SAI2_RX	I	JTAG_TCK	I
144	PCM_CLK_GSM[7]	O	+1.8V	GSM PCM clock output	PCM_CLK_GSM	O		
145	[6UL]UART5_RXD	I	+3.3V	UART5 serial data receive	UART5_RXD	I		
146	PCM_SYNC_GSM[7]	O	+1.8V	GSM PCM frame sync output	PCM_SYNC_GSM	O		
147	[6UL]UART5_TXD	O	+3.3V	UART5 serial data transmit	UART5_TXD	O		
148	PCM_IN_GSM[7]	I	+1.8V	GSM PCM data input	PCM_IN_GSM	I		
149	[6UL]UART3_RXD	I	+3.3V	UART3 serial data receive	UART3_RXD	I		
150	PCM_OUT_GSM[7]	O	+1.8V	GSM PCM data output	PCM_OUT_GSM	O		
151	[6UL]UART3_TXD	O	+3.3V	UART3 serial data transmit	UART3_TXD	O		
152	GND	-	-	Ground	GND	-		
153	GSM_APRDY[7]	I	+3.3V	GSM application processor sleep state detection	GSM_APRDY	I		
154	[6UL]ENET2_TXCLK	O	+3.3V	ETH2 RMII reference clock	SIM2_0_RST	O	SPI4_MISO /I2C_LCD_SDA	IO/ OD-IO
155	[6UL]UART2_RXD[8]	I	+3.3V	UART2 serial data receive	UART2_RXD	I		
156	[6UL]ENET2_RXD1	I	+3.3V	ETH2 RMII receive data 1	UART6_RXD/ I2C3_SDA	I/ OD-IO		
157	GSM_CTS[7]	O	+3.3V	GSM clear to send	GSM_CTS	O		
158	[6UL]ENET2_RXD0	I	+3.3V	ETH2 RMII receive data 0	UART6_TXD/ I2C3_SCL	O/ OD-IO		
159	[6UL]UART2_TXD[8]	O	+3.3V	UART2 serial data transmit	UART2_TXD	O		
160	[6UL]ENET2_CRS_DV	I	+3.3V	ETH2 RMII receive enable	UART7_TXD/ I2C4_SCL	O/ OD-IO	IO2_10	IO
161	GSM_RTS[7]	I	+3.3V	GSM request to send	GSM_RTS	I		
162	[6UL]ENET2_RXER	I	+3.3V	ETH2 RMII receive	SIM2_0_SVEN	O	SPI4_SS	IO

				error				
163	[6UL]UART4_TXD[8]	O	+3.3V	UART4 serial data transmit	UART4_TXD	O		
164	[6UL]ENET2_TXEN	O	+3.3V	ETH2 RMII transmit enable	SIM2_0_CLK	O	SPI4_MOSI /I2C_LCD_ SCL	IO/ OD-IO
165	[6UL]UART4_RXD[8]	I	+3.3V	UART4 serial data receive	UART4_RXD	I		
166	[6UL]ENET2_TXD0	O	+3.3V	ETH2 RMII transmit data 0	UART7_RXD/ I2C4_SDA	IO/ OD-IO	CTP_INT	I
167	GSM_DTR[7]	I	+3.3V	GSM data terminal ready(sleep mode control)	GSM_DTR	I		
168	[6UL]ENET2_TXD1	O	+3.3V	ETH2 RMII transmit data 1	SIM2_0_TRXD	IO	SPI4_SCLK	O
169	GSM_RI[7]	O	+3.3V	GSM ring indicator	GSM_RI	O		
170	GND	-	-	Ground	GND	-		
171	GND	-	-	Ground	GND	-		
172	[6UL]ENET1_TXCLK	O	+3.3V	ETH1 RMII reference clock	ENET1_TXCLK	O		
173	GND	-	-	Ground	GND	-		
174	[6UL]ENET1_RXD1	I	+3.3V	ETH1 RMII receive data 1	ENET1_RXD1	I		
175	GND	-	-	Ground	GND	-		
176	[6UL]ENET1_RXD0	I	+3.3V	ETH1 RMII receive data 0	ENET1_RXD0	I		
177	GND	-	-	Ground	GND	-		
178	[6UL]ENET1_CRS_DV	I	+3.3V	ETH1 RMII receive enable	ENET1_RXEN	I		
179	GND	-	-	Ground	GND	-		
180	[6UL]ENET1_RXER	I	+3.3V	ETH1 RMII receive error	ENET1_RXER	I		
181	GND	-	-	Ground	GND	-		
182	[6UL]ENET1_TXEN	O	+3.3V	ETH1 RMII transmit enable	ENET1_TXEN	O		
183	GND	-	-	Ground	GND	-		
184	[6UL]ENET1_TXD0	O	+3.3V	ETH1 RMII transmit data 0	ENET1_TXD0	O		
185	GND	-	-	Ground	GND	-		
186	[6UL]ENET1_TXD1	O	+3.3V	ETH1 RMII transmit data 1	ENET1_TXD1	O		
187	GND	-	-	Ground	GND	-		
188	GND	-	-	Ground	GND	-		-
189	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
190	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
191	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
192	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
193	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
194	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
195	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
196	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
197	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		

198	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
199	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		
200	+VMAIN	PI	+VDD	SOM Power supply	+VMAIN	PI		

Notes :

[6] SNVS_TAMPER0 to SNVS_TAMPER9 can be configured as GPIO or tamper detection pin only on G3 version, it is depending on the fuse setting TAMPER_PIN_DISABLE[1:0]. G0,G1,G2 versions does not support tamper detection function and those pins can only work as GPIO.

[7] If 4G/2G/GNSS module is assembled on the SOM, these signals have the given function. Otherwise the pin has no function.

[8] These signals are used by 4G/2G/GNSS module. If 4G/2G/GNSS module is not assembled on the SOM, these signals can be used as given in the carrier board options. Otherwise these pins should be left open.

Table 5 – CON1200 pin definitions

5 Hardware

5.1 Power Supply

INVENSOM-6UL power management circuit works from a single supply voltage +VMAIN and generates all necessary voltages for the SOM. 4G/2G/GNSS module is directly supplied from the +VMAIN supply so when the 4G/2G/GNSS module is assembled, +VMAIN is limited to the maximum supply voltage of the 4G/2G/GNSS module which is +4.2V. When 4G/2G/GNSS module option is not assembled, +VMAIN is limited to +5V.

Parameter		I/O	Min	Typ	Max	Unit
+VMAIN	SOM without 4G/2G/GNSS module	PI	3.6		5	V
	SOM with 4G/2G/GNSS module		3.6	3.8	4.2	V
GND				0		V
+3.3V_OUT	SOM Internal supply voltage	PO		+3.3		V
	output current				50	mA
[6UL]VDDA_ADC_3P3	iMX6UL ADC supply voltage	PI	3		3.6	V
+3V_COIN	iMX6UL SNVS Back-up supply voltage	PI	2.7		3.6	V
	Input current @ +VMAIN is not present			20		uA
	Input current @ +VMAIN is not present			0.1		uA

Table 6 – Power Supply Electrical Characteristics

+3.3V_OUT is generated by the INVENTRON-6UL's internal buck converter. This voltage can be used to supply low current (<50mA) external peripherals. (CAUTION: exceeding the maximum current may harm the SOM) +3.3V_ADC is the supply voltage for the iMX6UL's internal ADC circuit. +3.3V_ADC must be powered when chip is in RUN mode, IDLE mode, or SUSPEND mode, even if the ADC is not used. +3.3V_ADC should not be powered when iMX6UL is in SNVS mode.

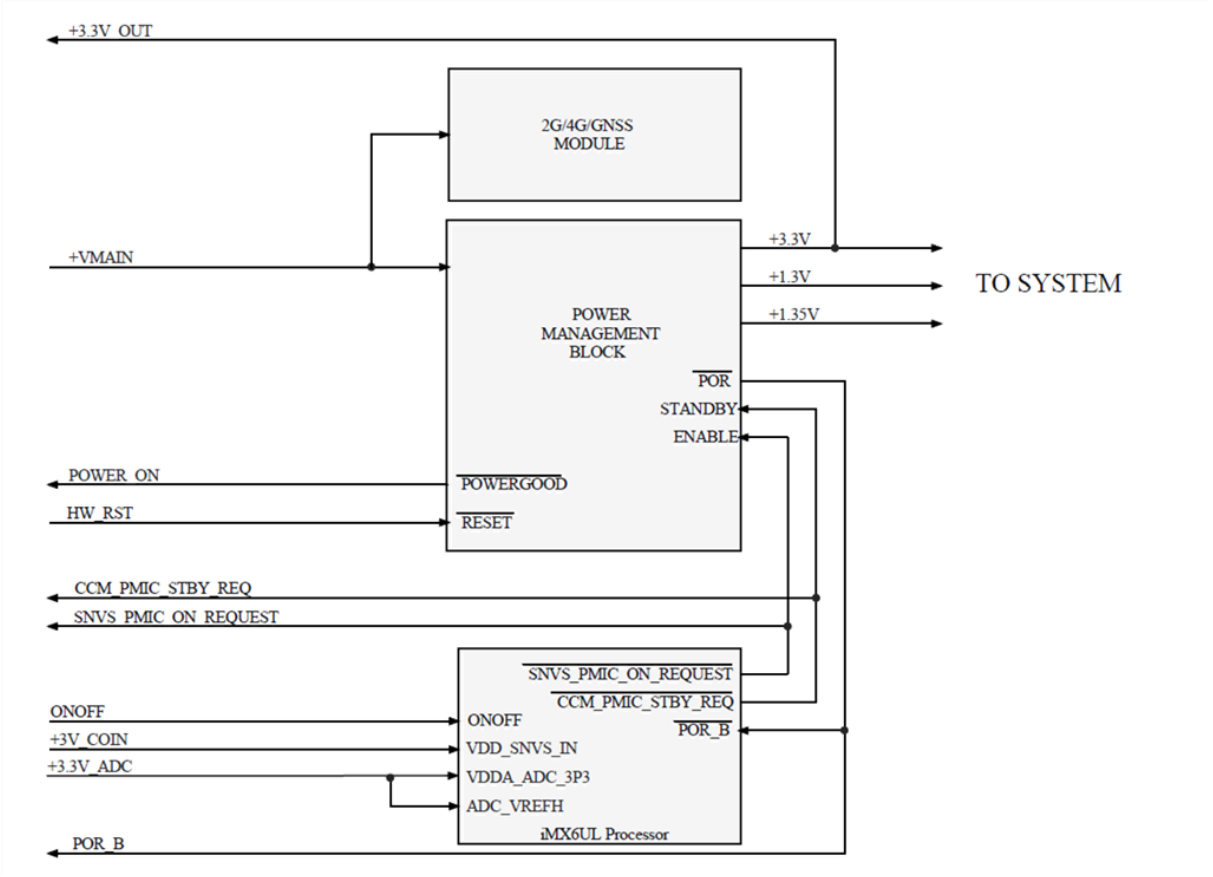


Figure 4 - Power Management Diagram

+3V_COIN is the supply voltage for iMX6UL SNVS (Secure Non-Volatile Storage) block which includes Secure Real Time Clock, Security State Machine, Master Key Control, Violation/Tamper Detection and reporting. +3V_COIN supplies all SNVS block even when +VMAIN is not present and ensure that +3V_COIN is connected before any other supply is switched on. If the system does not require SNVS functions like keeping real time and other data on OFF state (when +VMAIN is not present), +3V_COIN can be left unconnected. SNVS is powered by the power management block when +VMAIN is present and no current is drawn from +3V_COIN supply.

Pin No	Name	Signal Type	Power Domain	Description	Comment
14	HW_RST	I	+3.3V	Hardware Reset	This pin resets all SOM hardware. A low signal (0V) on this pin for 100msn will reset the SOM.
16	POWER_ON	O	+5V	Power on	A high signal (>2.0V) on this pin indicates that SOM power supply is completely ON. This signal can be used for power sequencing on customer's carrier board.
103	[6UL]CCM_PMIC_STBY_ REQ	O	+3.3V or SNVS'	PMIC Standby Request	This signal can be used to switch the peripherals of the carrier board to stand-by mode.
105	[6UL]SNVS_PMIC_ON_ REQ	O	+3.3V or SNVS'	PMIC On Request	This signal can be used to power-on or to shutdown the peripherals of the carrier board.
107	[6UL]ONOFF	I	+3.3V or SNVS'	i.MX6UL ONOFF Button signal	While the SOM is ON state, a low signal (0V) on this pin for a configurable period of time (refer

					to iMX6UL datasheet) will turn off the SOM where minimum current drawn from the +VMAIN. While the SOM is OFF state, a low signal (0V) on this pin for a configurable period of time (refer to iMX6UL datasheet) will turn on the SOM.
109	[6UL]POR_B	O	+3.3V or SNVS[1]	i.MX6UL Reset input	This signal is the power on reset signal of the iMX6UL processor generated by the power management block. This signal can be used to reset carrier board peripherals simultaneously with the processor

Notes :

[1]These pins are connected to the +3.3V power domain when +VMAIN is present. When +VMAIN is not present and +3V_COIN is connected, these pins are switched to SNVS power domain.

Table 7

5.2 Application Processor

The module supports multiple compatible options of G0, G1, G2, G3 sub family of iMX6UL. The complete block diagram of iMX6UL is shown on Figure-5. The additional functions of the G0, G1, G2, G3 sub families are shown on Table-8. G1 and G2 models can reach up to the maximum family speed of 696MHz and G3 model is the only model which supports all security functions including tamper detection.

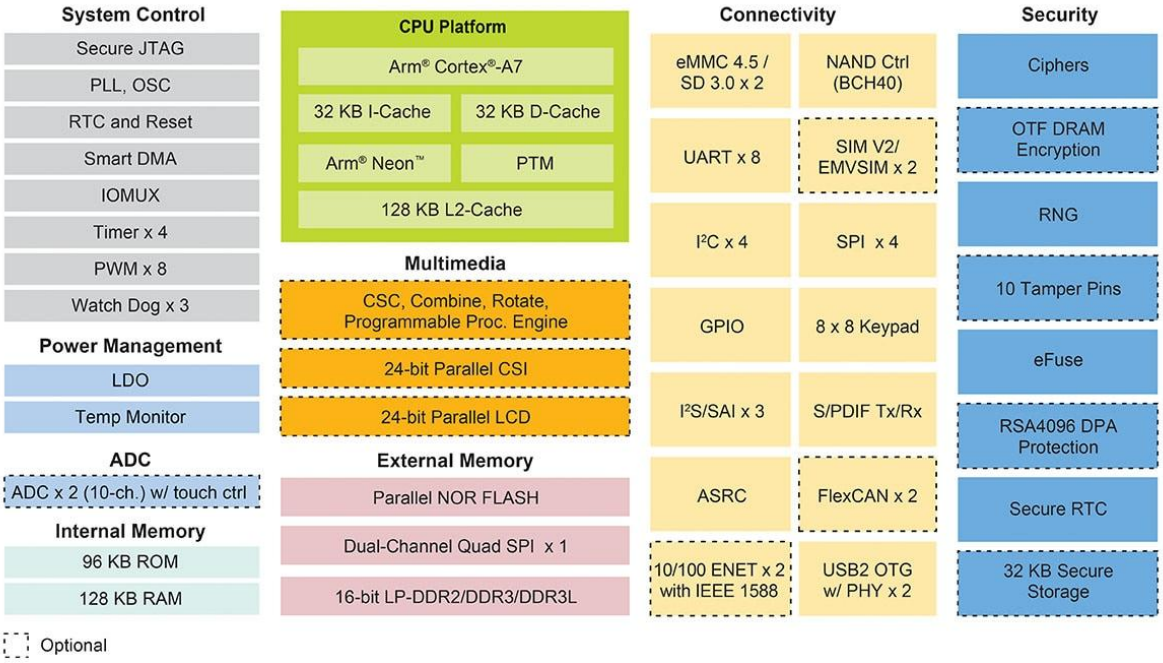


Figure 5 – iMX6UL Block Diagram

Feature	G0	G1	G2	G3
Sub Family	6UL Base	6UL General Purpose 1	6UL General Purpose 2	6UL Security
Core	ARM Cortex-A7	ARM Cortex-A7	ARM Cortex-A7	ARM Cortex-A7
Speed	528 MHz	528 and 696 MHz	528 and 696 MHz	528 MHz
Cache	32 KB-I, 32KB-D	32 KB-I, 32KB-D 128 KB L2	32 KB-I, 32KB-D 128 KB L2	32 KB-I, 32KB-D 128 KB L2
OCRAM	128 KB	128 KB	128 KB	128 KB
DRAM	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L
eFuse	512-bit	1024-bit	1536-bit	2048-bit
NAND (BCH40)	Yes	Yes	Yes	Yes
Parallel Nor/EBI	Yes	Yes	Yes	Yes
Ethernet	10/100 MB x 1	10/100 MB x 1	10/100 MB x 2	10/100 MB x 2
USB with PHY	OTG, HS/FS x 1	OTG, HS/FS x 2	OTG, HS/FS x 2	OTG, HS/FS x 2
CAN	0	1	2	2
Security	None	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot	TRNG, Crypto Engine (AES/TDES/SHA/RSA with DPA), Secure Boot, Tamper Monitor, PCI4.0 pre-certification, OTF DRAM Encryption
Graphic	None	None	PxP	PxP
CSI	None	None	16-bit Parallel CSI	16-bit Parallel CSI
LCD	None	None	24-bit Parallel LCD	24-bit Parallel LCD
QSPI	1	1	1	1
SDIO	2	2	2	2
UART	4	8	8	8
ISO7816-3	0	2	2	2
IIC	2	4	4	4
SPI	2	4	4	4
I^2S/SAI	1	3	3	3
S/PDIF	1	1	1	1
Timer/PWM	Timer x2, PWM x4	Timer x4, PWM x8	Timer x4, PWM x8	Timer x4, PWM x8
12-bit ADC	1 x 8ch	1 x 8ch	2 x 8ch	2 x 8ch
Keyboard (8 x 8)	Yes	Yes	Yes	Yes
Temperature	0°C to 70°C (Tj)	-40°C to 105°C (Tj)	-40°C to 105°C (Tj)	-40°C to 105°C (Tj)

Table 8

5.3 Memory

5.3.1 DDR SDRAM

The module supports 256MB to 1GB DDR3 SDRAM.

5.3.2 NAND Flash / e-MMC

The module supports 256MB to 512MB NAND Flash or 4GB to 64GB e-MMC. Only one storage option can be supported at a time.

5.3.3 QSPI NOR Flash

The module supports 32MB to 128MB QSPI NOR Flash.

5.4 Wi-Fi & Bluetooth Connectivity

INVENSOM-6UL contains an onboard 2.4GHZ IEEE802.11b/g/n W-LAN and Bluetooth®v5.1 (BR/EDR/BLE) module. Wi-Fi and Bluetooth transceivers share the same single antenna For RF characteristics please refer to Murata LBEE5KL1DX datasheet.

Pin No	Name	Signal Type	Power Domain	Description	Comment
4	32K_OSC	I	+3.3V	WiFi/BL external 32.768kHz sleep clock	This signal should be connected to SOM for proper Wi-Fi/BL operation.
29	BT_PCM_SYNC	IO	+3.3V	Bluetooth PCM sync can be master (output) or slave (input)	Supports PCM Timing Short Frame Sync(Master or Slave Mode) and PCM Timing Long Frame Sync, (Master or Slave Mode)
31	BT_PCM_OUT	O	+3.3V	Bluetooth PCM data output	
33	BT_PCM_CLK	IO	+3.3V	Bluetooth PCM clock can be master (output) or slave (input)	
35	BT_PCM_IN	I	+3.3V	Bluetooth PCM data input	
37	BT_HOST_WAKE	IO	+3.3V	Bluetooth host wake signal	
60	WL_HOST_WAKE	IO	+3.3V	W-LAN host wake signal	
62	BT_DEV_WAKE	IO	+3.3V	Bluetooth device wake signal	

Table 9

5.4.1 Wi-Fi / Bluetooth Antenna

Antenna	Impedance	Designator	Connector Type
Wi-Fi / Bluetooth	50Ω	CON900	u.FL (UMCC)

Table 10

5.5 4G/2G/GNSS Connectivity

INVENSOM-6UL contains an onboard 4G/2G/GNSS module. The following table shows the frequency bands of 4G/2G/GNSS module. For RF characteristics please refer to Quectel BG96 datasheet.

LTE Bands[1]	GSM[2]	GNSS
Cat M1 & NB1: LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19 /B20/B26/B28 LTE-TDD: B39 (for Cat M1only)	GSM850/EGSM900/ DCS1800/PCS1900	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS

[1] *VoLTE (Voice over LTE) is only supported under LTE Cat M1 network.*
[2] *only supports Packet Switch.*

Table 11

Pin No	Name	Signal Type	Power Domain	Description	Comment
1	VDD_GNSS	PI	-	GNSS active antenna power supply	If the GNSS antenna is active, this pin can be used to supply the LNA. Leave this pin open if the antenna is passive type.
3					
70	W_DISABLE#	I	+1.8V	GSM airplane mode	Apply logic low to this pin to

				control	enter into airplane mode. If unused, leave this pin open.
72	GSM_NETLIGHT	O	+1.8V	GSM network activity status	Flicker slowly (200ms High/1800ms Low) →Network searching Flicker slowly (1800ms High/200ms Low) → Idle Flicker quickly (125ms high/125ms Low)→ Data transfer is ongoing Always high→ Voice calling
76	GSM_RST	I	+3.3V	GSM reset	This pin can be used to reset the module. The module can be reset by driving this pin to a logic low level for time between 150ms and 460ms.
78	PSM_IND_GSM	O	+1.8V	GSM power saving mode (PSM) indicator	This pin outputs a high logic level when the module is in normal operation state, and outputs a low level voltage when the module enters into PSM
82	I2C_SCL_GSM	OD-IO	+1.8V	GSM I2C serial clock.	This pin is used for external audio codec. External pull-up resistor is required.
84	I2C_SDA_GSM	OD-IO	+1.8V	GSM I2C serial data.	This pin is used for external audio codec. External pull-up resistor is required.
88	SIM_PRESENCE	I	+1.8V	GSM SIM card insertion detection	SIM card hot-plug is detected via this pin. The function supports low level and high level detections and is disabled by default.
90	SIM_VDD	O	+3V or +1.8V	GSM Power supply of SIM card	Either 1.8V or 3.0V is supported by the module automatically.
92	SIM_RST	O	+3V or +1.8V	GSM Reset signal of SIM card	SIM card interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8V and 3.0V SIM cards are supported.
94	SIM_DATA	IO	+3V or +1.8V	GSM Data signal of SIM card	
96	SIM_CLK	O	+3V or +1.8V	GSM Clock signal of SIM card	
98	SIM_GND	-	-	GSM Ground of SIM card	
144	PCM_CLK_GSM	O	+1.8V	GSM PCM clock output	One Pulse Code Modulation (PCM) digital interface and one I2C interface for audio codec connection is provided. If unused, leave these pins open.
146	PCM_SYNC_GSM	O	+1.8V	GSM PCM frame sync output	
148	PCM_IN_GSM	I	+1.8V	GSM PCM data input	
150	PCM_OUT_GSM	O	+1.8V	GSM PCM data output	
153	GSM_APRDY	I	+3.3V	GSM application processor sleep state detection	This pin will detect the sleep state of the host (can be configured to high level or low level detection). If unused, leave these pins open.
157	GSM_CTS	O	+3.3V	GSM clear to send	Additional UART signals. This signals can be externally connected between 4G/2G/GNSS module and the iMX6UL. If unused, leave these pins open.
161	GSM_RTS	I	+3.3V	GSM request to send	
167	GSM_DTR	I	+3.3V	GSM data terminal ready(sleep mode control)	

169	GSM_RI	O	+3.3V	GSM ring indicator	

Table 12

The power supply (+VMAIN) range of the 4G/2G/GNSS module is from 3.6V to 4.2V. Please make sure that the input voltage will never drop below 3.6V during burst transmission in 2G network. The voltage drop will be less in LTE Cat M1 and LTE Cat NB1 networks.

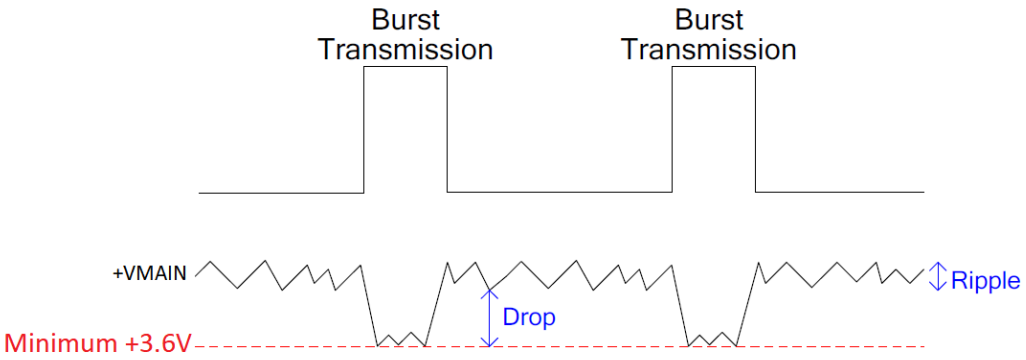


Figure 6

To decrease voltage drop, a bypass capacitor of about 220µF low esr aluminum electrolytic capacitor plus a multi-layer ceramic chip capacitor (MLCC) array should also be used. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to +VMAIN with the low esr aluminum electrolytic capacitor.

5.5.1 4G/2G/GNSS Antenna

Antenna Connector	Impedance	Designator	Connector
4G Cat M1&NB1/2G	50Ω	CON800	u.FL (UMCC)
GNSS	50Ω	CON801	u.FL (UMCC)
Antenna Type	Requirements		
GNSS [1]	Frequency range: 1559MHz -1609MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: < 1.5dB Active antenna gain: > 0dBi Active antenna embedded LNA gain: < 17dB		
LTE/GSM	VSWR: ≤ 2 Efficiency: > 30% Max Input Power (W): 50 Input Impedance (Ω): 50 Cable Insertion Loss: < 1dB (LTE B5/B8/B12/B13/B18/B19/B20/B26/B28, GSM850/EGSM900) Cable Insertion Loss: < 1.5dB (LTE B1/B2/B3/B4/B39, DCS1800/PCS1900)		

[1] *It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.*

Table 13

5.6 External Connectors

INVENSOM-6UL exposes two 100-pin Hirose DF40C-100DP-0.4V board-to-board connectors. The mating connector for these two connectors are given below.

SOM	Mating Connector	Stacked Height
without 4G/2G/GNSS module	Hirose DF40C-100DS-0.4V	1.5mm
with 4G/2G/GNSS module	Hirose DF40HC(3.0)-100DS-0.4V	3.0mm

Table 14

6 Software Features

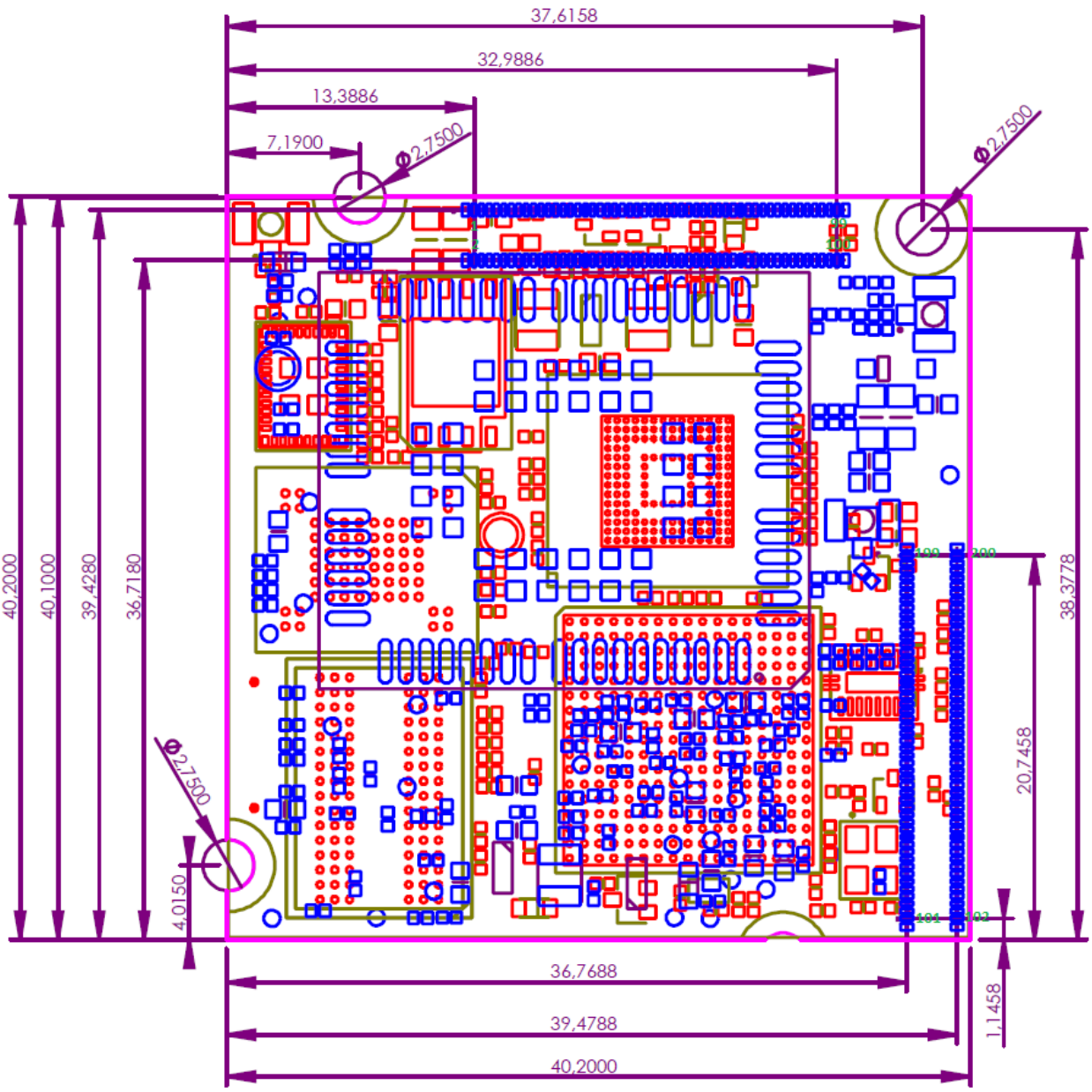
Inventron provides Yocto based board support package (BSP) with all required libraries and drivers included which can be used with its default carrier board. This customized Linux distribution is based on NXP's officially tested distribution. You can always use the standard drivers that are supported in the mainline kernel. Besides this, Inventron provides customized drivers for the INVENSOM-6UL peripherals.

Category	Feature	Description / Version
Bootloader Firmware	U-Boot	U-Boot 2020.04
Operating System	Kernel	Linux 5.4.47 (Forked from NXP Official Kernel)
	Configuration	Default Kernel Config and Standard Linux Drivers Included
Linux Drivers	USB	HOST and OTG Driver
	Ethernet	Ethernet Driver
	MMC/SD	MMC/SD Card Driver
	Nand Flash	Nand Flash Driver
	eMMC	eMMC Driver
	UART	UART Driver
	LCD Controller	480x272 4.3" TFT LCD Driver
	RTC	Secure RTC Driver
	Touch Panel	FT5426 Capacitive Touch Driver
	GPIO Button	Button Driver
	GPIO LED	LED Driver
	WiFi	WiFi Module Driver
	4G/2G GSM	Quectel BG96 GPRS support (2G, 4G Cat M1 or NBIoT)
	Audio	Audio (SGTL5000) Driver (MIC, Headphone, Line-out)
	SPI	SPI Driver

	Security	CAAM Kernel Driver, Secure Memory, Tamper Protection, Secure Boot, eFuse Drivers
	SAM/SIM Card	EMV Compliant SIM Driver
	Bluetooth	Bluetooth Driver
	Camera	Camera Driver (OV05640)
	Keypad	Keypad option 4x3 or 4x4
	I2C	I2C Driver
	EEPROM	24C64 Driver
	CAN	CAN Driver
	Battery	BQ27531 & BQ24296 Driver
Build System	Yocto (Openembedded)	Zeus (3.0.4)
Compiler Toolchain	MetaToolchain	Built by Yocto, GCC 9.2
	Application Toolchain	Built by Yocto, GCC 9.2
Applications	QT	Version 5.15
	Java	OpenJDK 8-15
	Swupdate	Version 2020.11
	Python	Python2 and Python3
Windowing System	Desktop Environment	Wayland (Weston)
Programming Languages	Runtime	C/C++, Java, Python, Perl, Shell Scripting, Node.JS
Package Manager	Default Package Manager	Rpm

Table 15

7 Mechanics



[1] *Dimensions are in mm.*
[2] *Please check www.inventron.com.tr for 2D and 3D data of the SOM*
[3] *Check the mating height of the board-to-board connector before placing any component under the SOM.*

Figure 7

8 Ordering Information

INVENSOM	-	6UL	-	CPU	-	SPEED	-	RAM	-	STORAGE	-	WiFi BL	-	GSM GNSS	-	TEMP
INVENSOM	-	6UL	-	G3	-	528	-	R1024	-	E4GB	-	W01	-	G01	-	CT

	Selection	Description
CPU	G0	Minumum feature
	G1	Intermediate feature
	G2	Extra Security
	G3	Full Security
SPEED	528	528MHz Clock Freq
	696	696MHz Clock Freq
RAM	R0128	128MB DDR3
	R0256	256MB DR3
	R0512	512MB DR3
	R1024	1024MB DR3
STORAGE	0128	128MB QSPI NOR Flash
	N128	128MB NAND Flash
	N256	256MB NAND Flash
	N512	512MB NAND Flash
	E4GB	4GB eMMC
	E8GB	8GB eMMC
	E16GB	16GB eMMC
WiFi/BL	W00	No Wi-Fi/BL
	W01	IEEE802.11b/g/n Bluetooth®v5.1 (BR/EDR/BLE)
4G/2G/GNSS	G00	No 4G/2G/GNSS
	G01	LTE Cat M1 & Cat NB1 & EGPRS+GNSS
TEMP	CT	Consumer Grade : 0 to 70°C
	IT	Industrial Grade : -40 to 85°C

Table 16