

OP07x Precision Operational Amplifiers

1 Features

- Low Noise
- No External Components Required
- Replace Chopper Amplifiers at a Lower Cost
- Wide Input-Voltage Range: 0 to ± 14 V (Typ)
- Wide Supply-Voltage Range: ± 3 V to ± 18 V

2 Applications

- Wireless Base Station Control Circuits
- Optical Network Control Circuits
- Instrumentation
- Sensors and Controls
- Precision Filters

3 Description

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

Device Information(1)

| PART NUMBER | PACKAGE (PIN) | BODY SIZE |
|-------------|---------------|-------------------|
| OP07x | SO (8) | 6.20 mm x 5.30 mm |
| | SOIC (8) | 4.90 mm x 3.91 mm |
| | PDIP (8) | 9.81 mm x 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

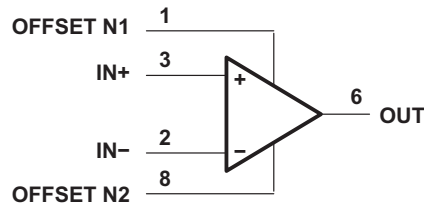


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5 Revision History

Changes from Revision F (January 2014) to Revision G

Page

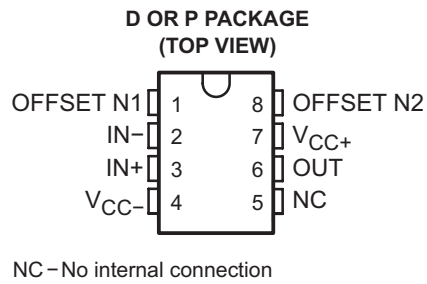
- Added *Applications*, *Device Information* table, *Pin Functions* table, *Handling Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. **1**

Changes from Revision E (May 2004) to Revision F

Page

- Deleted *Ordering Information* table. **1**

6 Pin Functions



Pin Functions

| PIN | | TYPE | DESCRIPTION |
|------------------|-----|------|--|
| NAME | NO. | | |
| IN+ | 3 | I | Noninverting input |
| IN- | 2 | I | Inverting input |
| NC | 5 | — | Do not connect |
| OFFSET N1 | 1 | I | External input offset voltage adjustment |
| OFFSET N2 | 8 | I | External input offset voltage adjustment |
| OUT | 6 | O | Output |
| V _{CC+} | 7 | — | Positive supply |
| V _{CC-} | 4 | — | Negative supply |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--|---|-----------|-----|------|
| $V_{CC+}^{(2)}$ | Supply voltage | 0 | 22 | V |
| $V_{CC-}^{(2)}$ | | -22 | 0 | |
| Differential input voltage ⁽³⁾ | | ±30 | | V |
| V_I | Input voltage range (either input) ⁽⁴⁾ | ±22 | | V |
| Duration of output short circuit ⁽⁵⁾ | | Unlimited | | |
| T_J | Operating virtual-junction temperature | 150 | | °C |
| Lead temperature 1.6 mm (1/16 in) from case for 10 s | | 260 | | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- (5) The output may be shorted to ground or to either power supply.

7.2 Handling Ratings

| PARAMETER | DEFINITION | | MIN | MAX | UNIT |
|-------------|---------------------------|--|-----|------|------|
| T_{STG} | Storage temperature range | | -65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic Discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 0 | 1000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------|--------------------------------|-----|-----|------|
| V_{CC+} | Supply voltage | 3 | 18 | V |
| V_{CC-} | | -3 | -18 | |
| V_{IC} | Common-mode input voltage | -13 | 13 | |
| T_A | Operating free-air temperature | 0 | 70 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | D | P | UNIT |
|-------------------------------|--|----|----|------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 97 | 85 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

7.5 Electrical Characteristics

 at specified free-air temperature, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | T_A ⁽²⁾ | OP07C | | | OP07D | | | UNIT | |
|----------------|--|--|-------------|-------------|------------|------------|------------|------------------------|------------------------------|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| V_{IO} | Input offset voltage | $V_O = 0\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 60 | | | 150 | | | μV |
| | | | 0°C to 70°C | 85 | | | 250 | | | |
| α_{VIO} | Temperature coefficient of input offset voltage | $V_O = 0\text{ V}$, $R_S = 50\ \Omega$ | 0.5 | | | 2.5 | | | $\mu\text{V}/^\circ\text{C}$ | |
| | Long-term drift of input offset voltage | See | 0.4 | | | | | | $\mu\text{V}/\text{mo}$ | |
| | Offset adjustment range | $R_S = 20\ \text{k}\Omega$, See Figure 2 | ± 4 | | | | | | mV | |
| I_{IO} | Input offset current | | 25°C | 0.8 | | | 6 | | | nA |
| | | | 0°C to 70°C | 1.6 | | | 8 | | | |
| α_{IIO} | Temperature coefficient of input offset current | | 12 | | | 50 | | | $\text{pA}/^\circ\text{C}$ | |
| I_{IB} | Input bias current | | 25°C | ± 1.8 | | | ± 12 | | | nA |
| | | | 0°C to 70°C | ± 2.2 | | | ± 14 | | | |
| α_{IIB} | Temperature coefficient of input bias current | | 18 | | | 50 | | | $\text{pA}/^\circ\text{C}$ | |
| | | | 0°C to 70°C | | | | | | | |
| V_{ICR} | Common-mode input voltage range | | 25°C | ± 13 | ± 14 | ± 13 | ± 14 | V | | |
| | | | 0°C to 70°C | ± 13 | ± 13.5 | ± 13 | ± 13.5 | | | |
| V_{OM} | Peak output voltage | $R_L \geq 10\ \text{k}\Omega$ | 25°C | ± 12 | ± 13 | ± 12 | ± 13 | V | | |
| | | $R_L \geq 2\ \text{k}\Omega$ | | ± 11.5 | ± 12.8 | ± 11.5 | ± 12.8 | | | |
| | | $R_L \geq 1\ \text{k}\Omega$ | | ± 12 | | ± 12 | | | | |
| | | $R_L \geq 2\ \text{k}\Omega$ | | 0°C to 70°C | ± 11 | ± 12.6 | ± 11 | | | ± 12.6 |
| A_{VD} | Large-signal differential voltage amplification | $V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V to } 11.4\text{ V}$, $R_L \geq 500\ \text{k}\Omega$ | 25°C | 100 | 400 | 400 | | V/mV | | |
| | | $V_O = \pm 10$, $R_L = 2\ \text{k}\Omega$ | 25°C | 120 | 400 | 120 | 400 | | | |
| | | | 0°C to 70°C | 100 | 400 | 100 | 400 | | | |
| B_1 | Unity-gain bandwidth | | 25°C | 0.4 | 0.6 | 0.4 | 0.6 | MHz | | |
| r_i | Input resistance | | 25°C | 8 | 33 | 7 | 31 | M Ω | | |
| CMRR | Common-mode rejection ratio | $V_{IC} = \pm 13\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 100 | 120 | 94 | 110 | dB | | |
| | | | 0°C to 70°C | 97 | 120 | 94 | 106 | | | |
| k_{SVS} | Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) | $V_{CC\pm} = \pm 3\text{ V to } \pm 18\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 7 | 32 | 7 | 32 | $\mu\text{V}/\text{V}$ | | |
| | | | 0°C to 70°C | 10 | 51 | 10 | 51 | | | |
| P_D | Power dissipation | $V_O = 0$, No load | 25°C | 80 | 150 | 80 | 150 | mW | | |
| | | $V_{CC\pm} = \pm 3\text{ V}$, $V_O = 0$, No load | | 4 | 8 | 4 | 8 | | | |

- (1) Because long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first 30 days of operation.
- (2) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

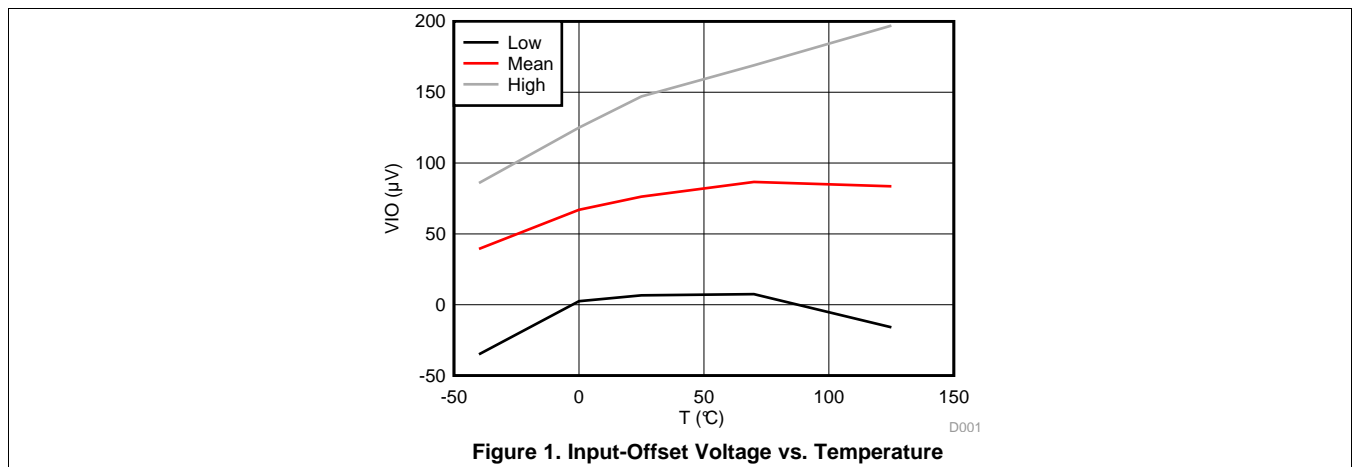
7.6 Operating Characteristics

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | OP07C | OP07D | UNIT |
|---|--------------------------------|-------|-------|------------------------------|
| | | TYP | TYP | |
| V_n Input offset voltage | f = 10 Hz | 10.5 | 10.5 | $\text{nV}/\sqrt{\text{Hz}}$ |
| | f = 100 Hz | 10.2 | 10.3 | |
| | f = 1 kHz | 9.8 | 9.8 | |
| $V_{N(PP)}$ Peak-to-peak equivalent input noise voltage | f = 0.1 Hz to 10 Hz | 0.38 | 0.38 | μV |
| I_n Equivalent input noise current | f = 10 Hz | 0.35 | 0.35 | $\text{nV}/\sqrt{\text{Hz}}$ |
| | f = 100 Hz | 0.15 | 0.15 | |
| | f = 1 kHz | 0.13 | 0.13 | |
| $I_{N(PP)}$ Peak-to-peak equivalent input noise current | f = 0.1 Hz to 10 Hz | 15 | 15 | μA |
| SR Slew rate | $R_L \geq 2\text{ k}\Omega$ | 0.3 | 0.3 | $\text{V}/\mu\text{s}$ |

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise noted.

8 Typical Characteristics



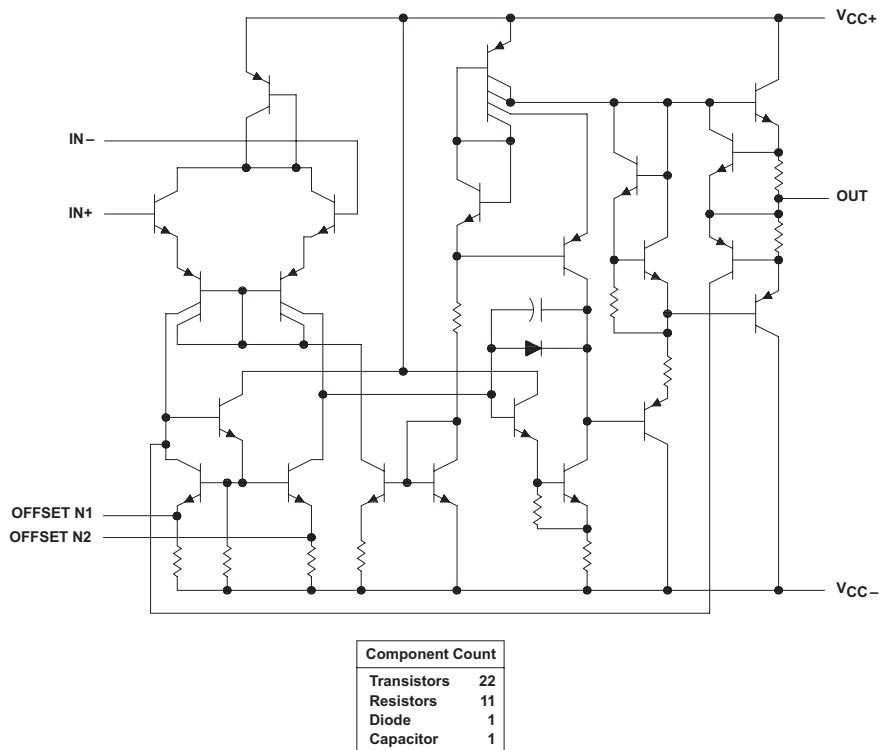
9 Detailed Description

9.1 Overview

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

These devices are characterized for operation from 0°C to 70°C.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Offset-Voltage Null Capability

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, et cetera. The input offset pins allow the designer to adjust for these mismatches by external circuitry. See the [Application and Implementation](#) section for more details on design techniques.

9.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The OP07 has a 0.3-V/ μ s slew rate.

9.4 Device Functional Modes

The OP07 is powered on when the supply is connected. It can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

10 Application and Implementation

10.1 General Application

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, etc. The input offset pins allow the designer to adjust for these mismatches by external circuitry. These input mismatches can be adjusted by putting resistors or a potentiometer between the inputs as shown in [Figure 2](#). A potentiometer can be used to fine tune the circuit during testing or for applications which require precision offset control. More information about designing using the input-offset pins, see [Nulling Input Offset Voltage of Operational Amplifiers \(SLOA045\)](#).

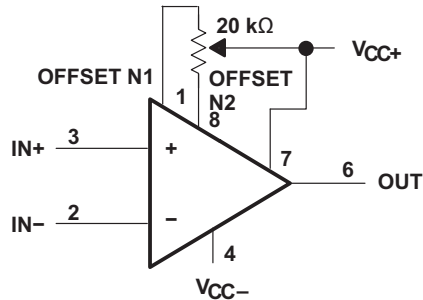


Figure 2. Input Offset-Voltage Null Circuit

10.2 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so it can provide as much current as necessary to the output load.

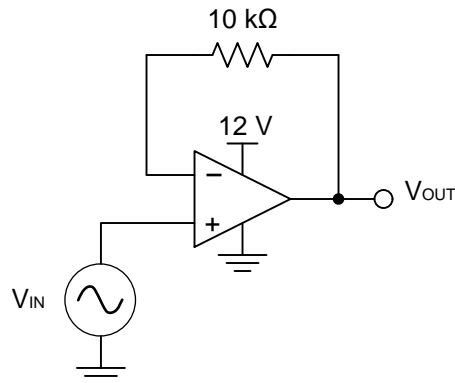


Figure 3. Voltage Follower Schematic

Typical Application (continued)

10.2.1 Design Requirements

- Output range of 2 V to 11 V
- Input range of 2 V to 11 V

10.2.2 Detailed Design Procedure

10.2.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by its internal circuitry to some level below the supply rails. For this amplifier, the output voltage swing is within ± 12 V, which accommodates the input and output voltage requirements.

10.2.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The chosen amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail, rather than ground, allows the amplifier to maintain linearity for inputs below 2 V.

10.2.3 Application Curves for Output Characteristics

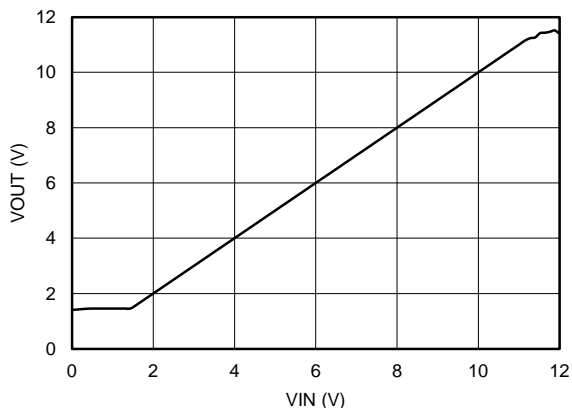


Figure 4. Output Voltage vs Input Voltage

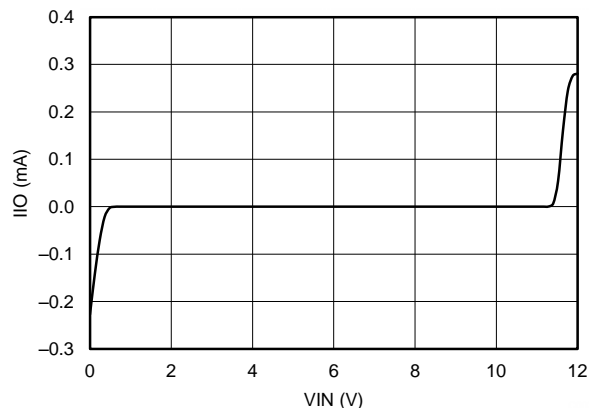


Figure 5. Current Drawn by the Input of the Voltage Follower (I_{IO}) vs the Input Voltage

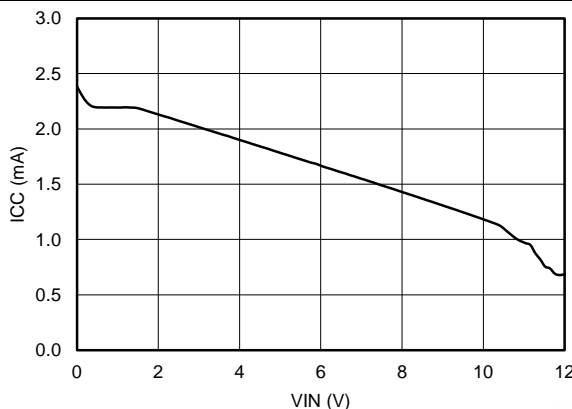


Figure 6. Current Drawn from Supply (I_{CC}) vs the Input Voltage

11 Power Supply Recommendations

The OP07 is specified for operation from ± 3 to ± 18 V; many specifications apply from 0°C to 70°C.

CAUTION

Supply voltages larger than ± 22 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#).

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. On multilayer PCBs, one or more layers are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicularly, as opposed to in parallel, with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

12.2 Layout Example

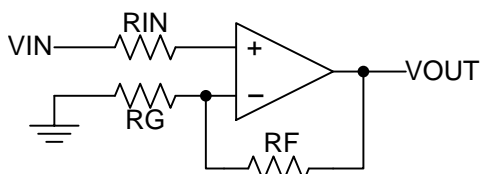


Figure 7. Operational Amplifier Schematic for Noninverting Configuration

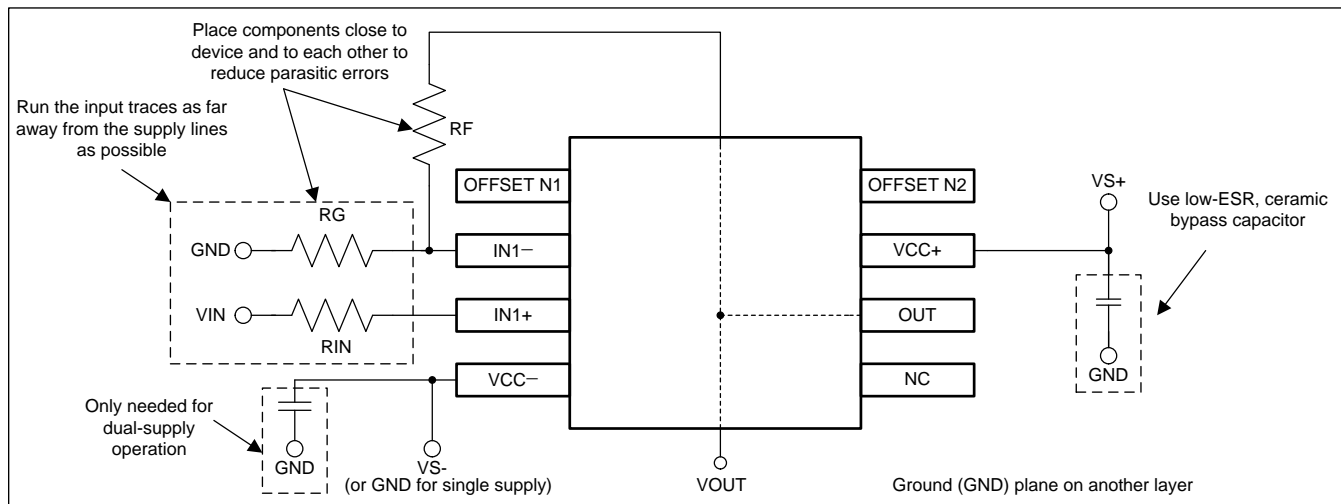


Figure 8. Operational Amplifier Board Layout for Noninverting Configuration

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

| Parts | Product Folder | Sample & Buy | Technical Documents | Tools & Software | Support & Community |
|-------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| OP07C | Click here | Click here | Click here | Click here | Click here |
| OP07D | Click here | Click here | Click here | Click here | Click here |

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| OP-07DPSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP-07D | Samples |
| OP-07DPSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP-07D | Samples |
| OP07CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP07C | Samples |
| OP07CDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP07C | Samples |
| OP07CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP07C | Samples |
| OP07CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | 0 to 70 | OP07C | Samples |
| OP07CDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP07C | Samples |
| OP07CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP07C | Samples |
| OP07CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | OP07CP | Samples |
| OP07CPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | OP07CP | Samples |
| OP07DD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP07D | Samples |
| OP07DDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP07D | Samples |
| OP07DDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP07D | Samples |
| OP07DDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | OP07D | Samples |
| OP07DP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | OP07DP | Samples |
| OP07DPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | OP07DP | Samples |

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OP-07DPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| OP07CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OP07CDR | SOIC | D | 8 | 2500 | 330.0 | 12.8 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OP07CDRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OP07DDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| OP-07DPSR | SO | PS | 8 | 2000 | 367.0 | 367.0 | 38.0 |
| OP07CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| OP07CDR | SOIC | D | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| OP07CDRG4 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| OP07DDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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