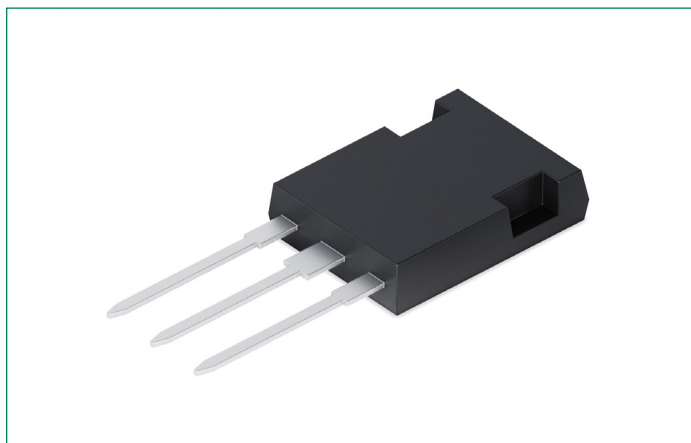


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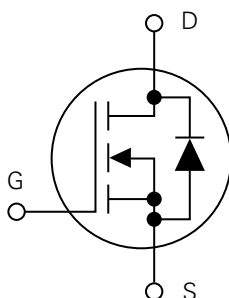
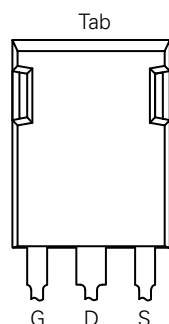
1200 V, 550 mΩ Polar™ HiPerFET™ Power MOSFET

N-Channel Enhancement Mode

E153432



Pinout Diagram (ISOPLUS247)



G: Gate; **D:** Drain; **S:** Source; **Tab:** Isolated

Features:

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- Low Intrinsic Gate Resistance
- 2500 V~ Electrical Isolation
- International Standard Package
- Fast Recovery Rectifier
- Avalanche Rated
- Low Package Inductance

Advantages:

- Easy to Mount
- Space Savings
- High Power Density

Applications:

- High Voltage Switch-mode and Resonant-Mode Power Supplies
- High Voltage Pulse Power Applications
- High Voltage Discharge Circuits in Lasers Pulsers, Spark Igniters, RF Generators
- High Voltage DC-DC Converters
- High Voltage DC-AC Inverters

Product Summary

Characteristic	Value	Unit
V_{DS}	1200	V
I_{D25}	15	A
$R_{DS(on)}$	≤ 550	mΩ
t_{rr}	≤ 300	ns

Maximum Ratings

Symbol	Characteristics	Conditions	Value	Units
V_{DSS}	Drain-Source Voltage	$T_J = 25^\circ\text{C}$ to 150°C	1200	V
V_{DGR}	Drain-Gate Voltage	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1\text{ M}\Omega$	1200	V
V_{GSS}	Gate-Source Voltage	Continuous	± 30	V
V_{GSM}		Transient	± 40	
I_{D25}	Drain Current	$T_C = 25^\circ\text{C}$	15	A
I_{DM}	Peak Drain Current	$T_C = 25^\circ\text{C}$, Pulse width limited by T_{JM}	60	
I_A	Avalanche Current	$T_C = 25^\circ\text{C}$	13	A
E_{AS}	Avalanche Energy	$T_C = 25^\circ\text{C}$	500	mJ
dv/dt	Reverse Diode dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$	15	V/ns
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	320	W
T_J	Operating Junction Temperature	–	-55 to +150	$^\circ\text{C}$
T_{JM}	Maximum Junction Temperature	–	150	
T_{stg}	Storage Temperature	–	-55 to +150	
T_L	Maximum Lead Temperature for Soldering	–	300	$^\circ\text{C}$
V_{ISOL}	Isolation Voltage	50/60 Hz, $t = 1\text{ min}$	2500	V~
F_C	Mounting Force	–	20..120/4.5..27	N/lb
W	Weight	–	5	g

Thermal Characteristics

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$R_{th, JC}$	Thermal Resistance, junction-to-case	–	–	0.39	$^\circ\text{C}/\text{W}$
$R_{th, CS}$	Thermal Resistance, case-to-sink	–	0.15	–	$^\circ\text{C}/\text{W}$

Electrical Characteristics – Static ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 3\text{ mA}$, $V_{GS} = 0\text{ V}$	1200	–	–	V
$V_{GS(th)}$	Gate Threshold Voltage	$I_D = 1\text{ mA}$, $V_{DS} = V_{GS}$	3.5	–	6.5	V
I_{GSS}	Gate-Source Leakage Current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$	–	–	± 200	nA
I_{DSS}	Drain-Source Current	$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{ V}$	–	–	50	μA
		$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$	–	–	5	mA
$R_{DS(on)}$	Drain-Source On-Resistance ¹	$V_{GS} = 10\text{ V}$, $I_D = 13\text{ A}$	–	–	550	m Ω

Note 1: Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle, $d \leq 2\%$

Electrical Characteristics – Dynamic ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
g_{fs}	Transconductance ¹	$V_{DS} = 20\text{ V}, I_D = 13\text{ A}$	13	21	–	S
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	–	14	–	nF
C_{oss}	Output Capacitance		–	725	–	pF
C_{rss}	Reverse Transfer Capacitance		–	50	–	pF
R_{Gi}	Gate Input Resistance	–	–	1.5	–	Ω
$Q_{g(on)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \times V_{DSS},$ $I_D = 13\text{ A}$	–	225	–	nC
Q_{gs}	Gate-Source Charge		–	87	–	
Q_{gd}	Gate-Drain Charge		–	98	–	
$t_{d(on)}$	Turn-on Delay Time	Resistive Switching $V_{GS} = 10\text{ V}, V_{DS} = 0.5 \times V_{DSS},$ $I_D = 13\text{ A}, R_{G(ext)} = 1\text{ }\Omega$	–	56	–	ns
t_r	Rise Time		–	55	–	
$t_{d(off)}$	Turn-off Delay Time		–	76	–	
t_f	Fall Time		–	58	–	

Source-Drain Diode Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
I_S	Continuous Diode Forward Current	$V_{GS} = 0\text{ V}$	–	–	26	A
I_{SM}	Diode Pulse Current	Repetitive, Pulse width limited by T_{JM}	–	–	104	A
V_{SD}	Diode Forward Voltage ¹	$I_F = I_S, V_{GS} = 0\text{ V}$	–	–	1.5	V
t_{rr}	Reverse Recovery Time	$I_F = 13\text{ A}, -di/dt = 100\text{ A}/\mu\text{s},$ $V_R = 100\text{ V}, V_{GS} = 0\text{ V}$	–	–	300	ns
I_{rm}	Reverse Recovery Charge		–	12.0	–	A
Q_{rm}	Reverse Recovery Current		–	1.3	–	μC

Note 1: Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle, $d \leq 2\%$

Characteristic Curves

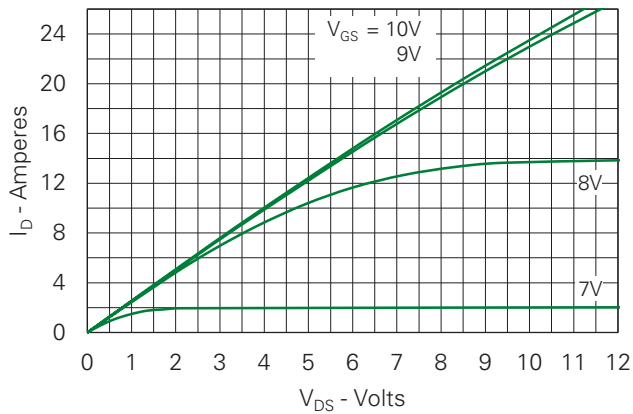
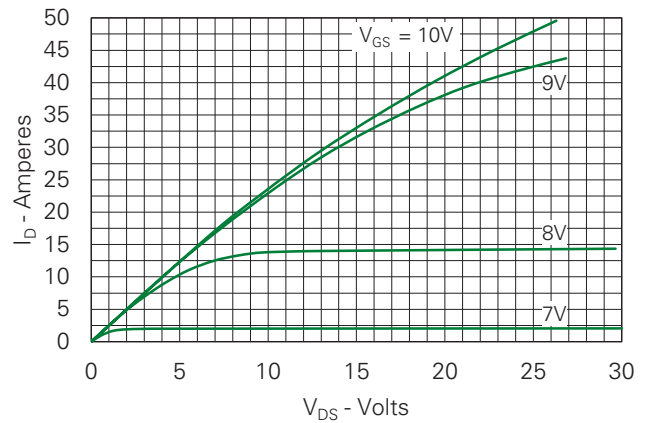
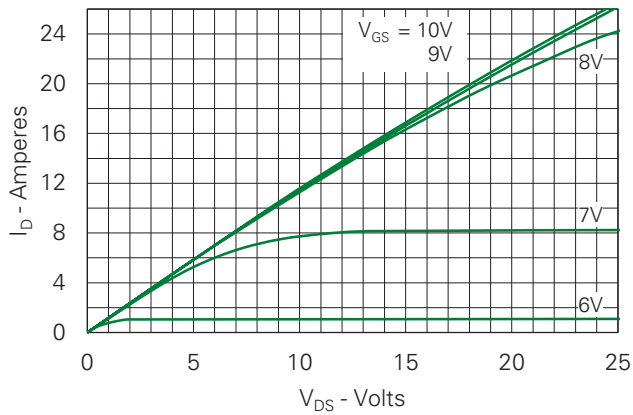
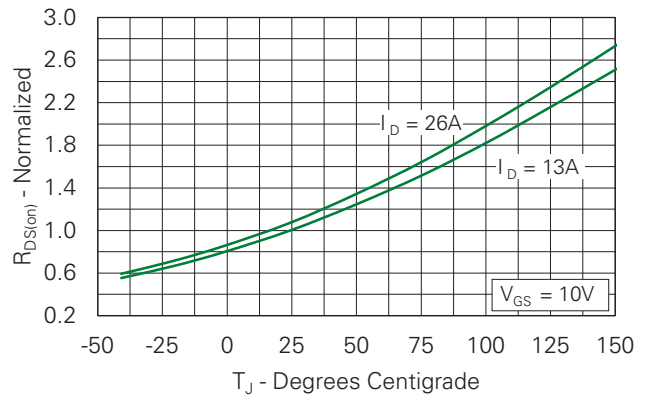
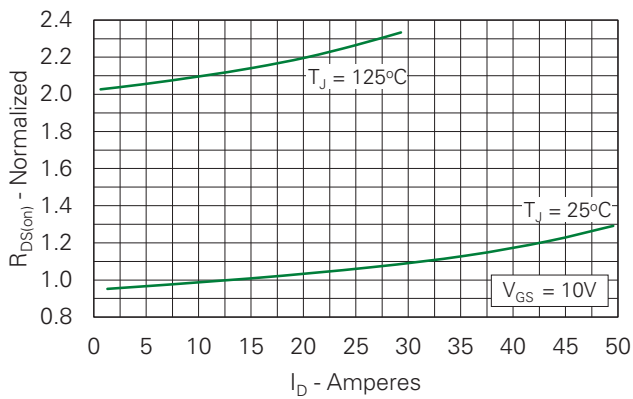
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$ Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$ Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$ Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 13\text{A}$ Value vs. Junction TemperatureFig. 5. $R_{DS(on)}$ Normalized to $I_D = 13\text{A}$ Value vs. Drain Current

Fig. 6. Maximum Drain Current vs. Case Temperature

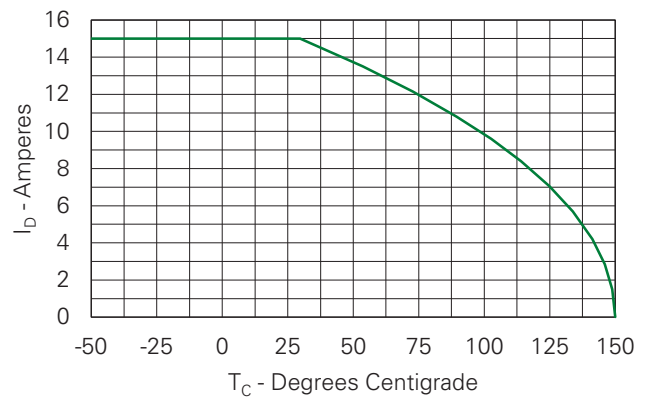


Fig. 7. Input Admittance

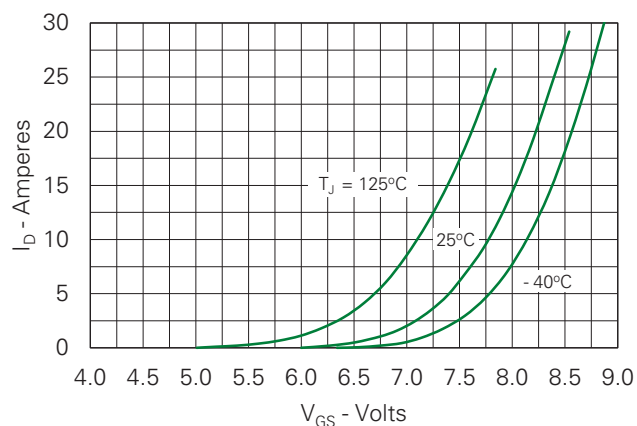


Fig. 8. Transconductance

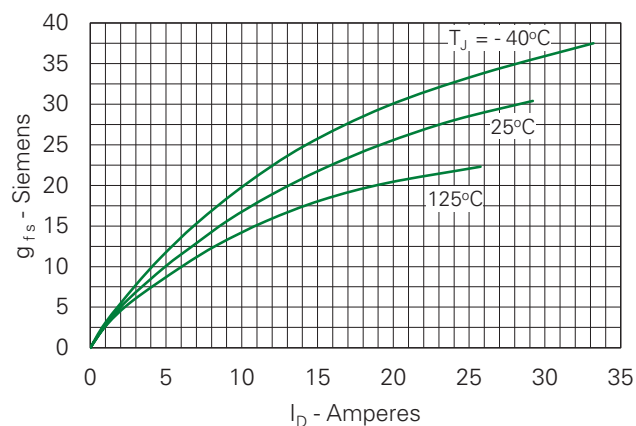


Fig. 9. Forward Voltage Drop of Intrinsic Diode

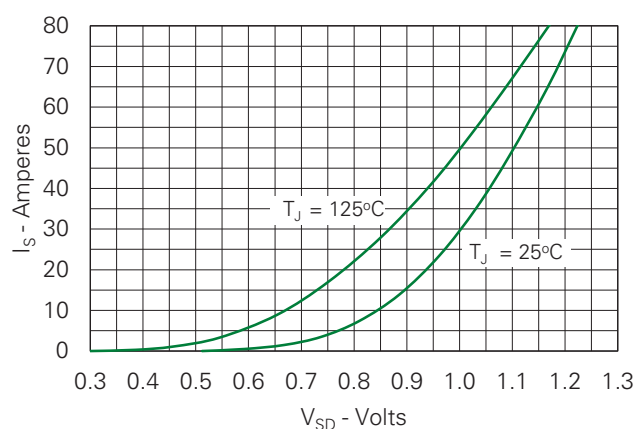


Fig. 10. Gate Charge

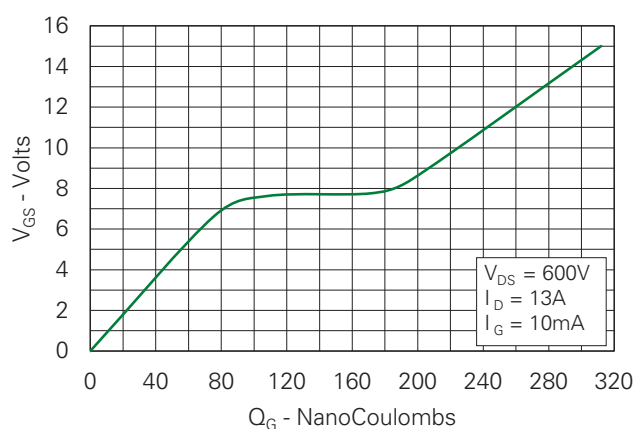


Fig. 11. Capacitance

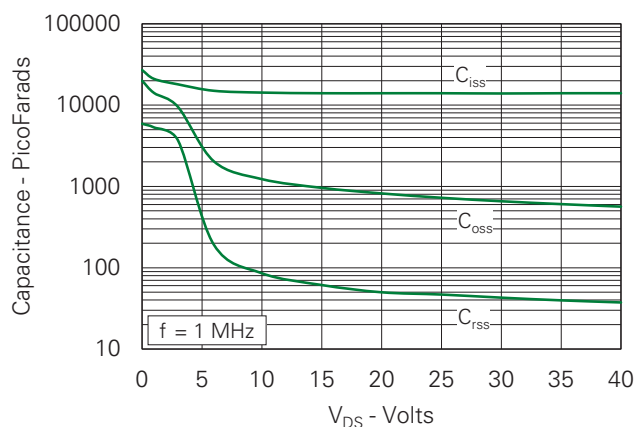
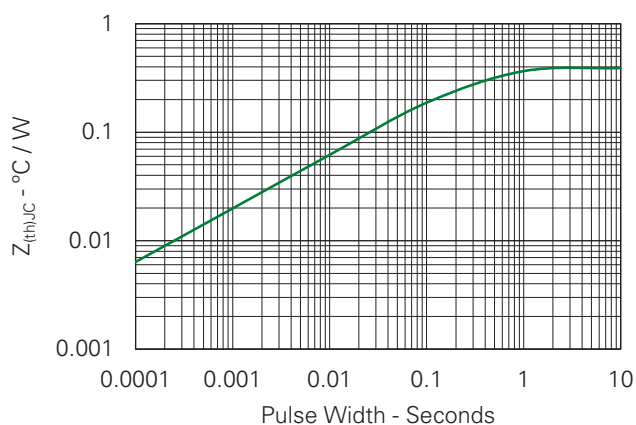
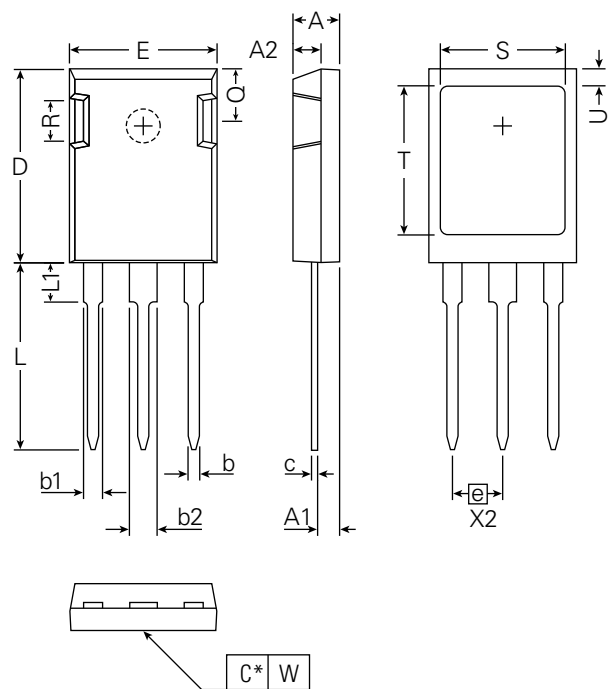


Fig. 12. Maximum Transient Thermal Impedance



Part Outline Drawing (ISOPLUS247)



Symbol	Inches			Millimeters		
	Min.	Typical	Max.	Min.	Typical	Max
A	0.190	–	0.205	4.83	–	5.21
A1	0.090	–	0.100	2.29	–	2.54
A2	0.075	–	0.085	1.91	–	2.16
b	0.045	–	0.055	1.14	–	1.40
b1	0.075	–	0.085	1.91	–	2.15
b2	0.115	–	0.126	2.92	–	3.20
C	0.024	–	0.033	0.61	–	0.83
D	0.819	–	0.840	20.80	–	21.34
E	0.620	–	0.635	15.75	–	16.13
e	0.215 BSC			5.45 BSC		
L	0.780	–	0.811	19.81	–	20.60
L1	0.150	–	0.172	3.81	–	4.38
Q	0.220	–	0.244	5.59	–	6.20
R	0.170	–	0.191	4.32	–	4.85
S	0.520	–	0.540	13.21	–	13.72
T	0.620	–	0.640	15.75	–	16.26
U	0.065	–	0.080	1.65	–	2.03
W	0	–	0.004	0	–	0.10

Note This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

C* Convex bow of substrate is typ<0.04mm over plastic surface level of device bottom side.

Lead Finish External leads are Pb free solder dip

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Part of:

