

# P80FG6EAL

Power MOSFETs  
60V, 80A, N-channel

### Feature

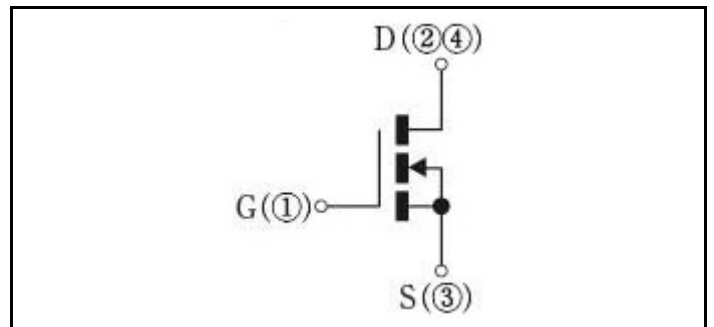
- N-channel
- SMD
- Low Ron
- 4.5V Gate Drive
- Low Capacitance
- Pb free terminal
- RoHS:Yes

### OUTLINE

Package (House Name): FG  
Package (JEDEC Code): TO-263AB



### Equivalent circuit



### Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	T <sub>stg</sub>		-55 to 150	°C
Channel temperature	T <sub>ch</sub>		150	°C
Drain-source voltage	V <sub>DSS</sub>		60	V
Gate-source voltage	V <sub>GSS</sub>		±20	V
Continuous drain current(DC)	I <sub>D</sub>		80	A
Continuous drain current(Peak)	I <sub>DP</sub>	Pulse width 10μs, duty=1/100	320	A
Total power dissipation	P <sub>T</sub>		128	W
Single avalanche current	I <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	52	A
Single avalanche energy	E <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	344	mJ

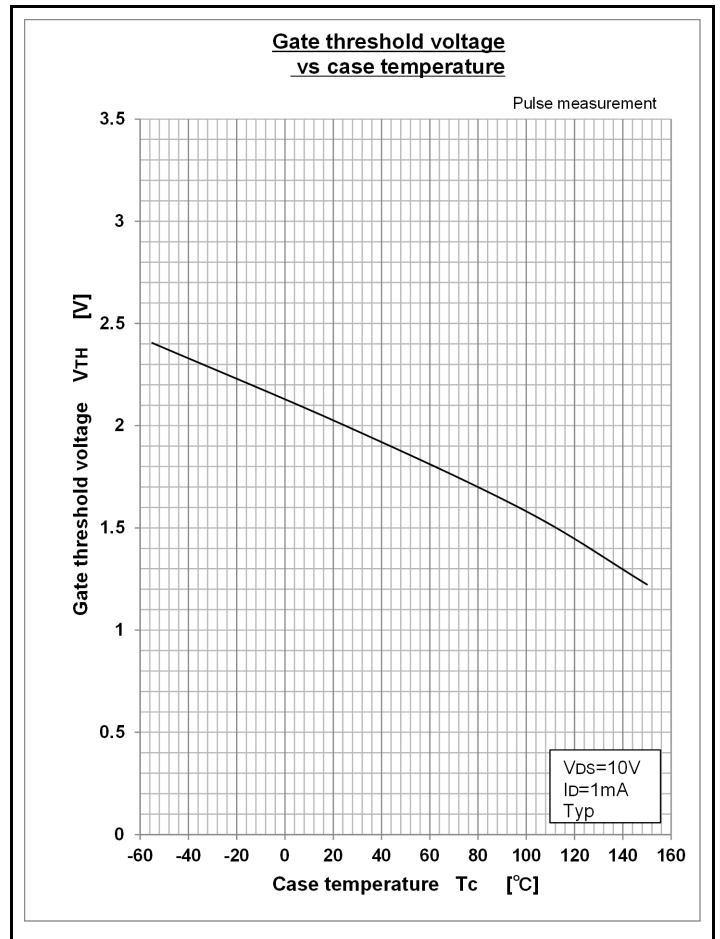
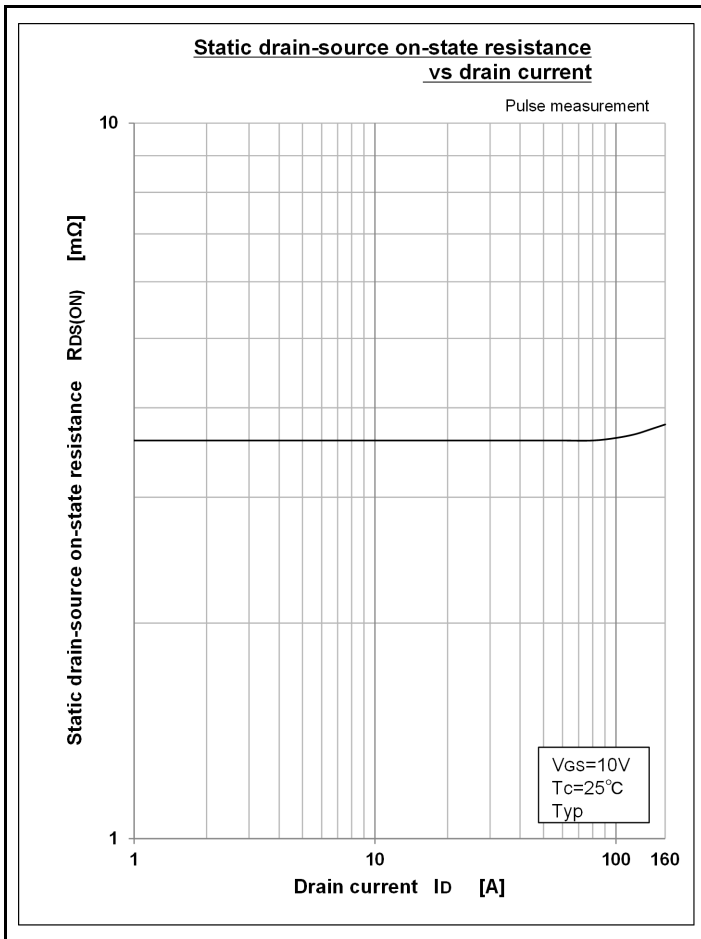
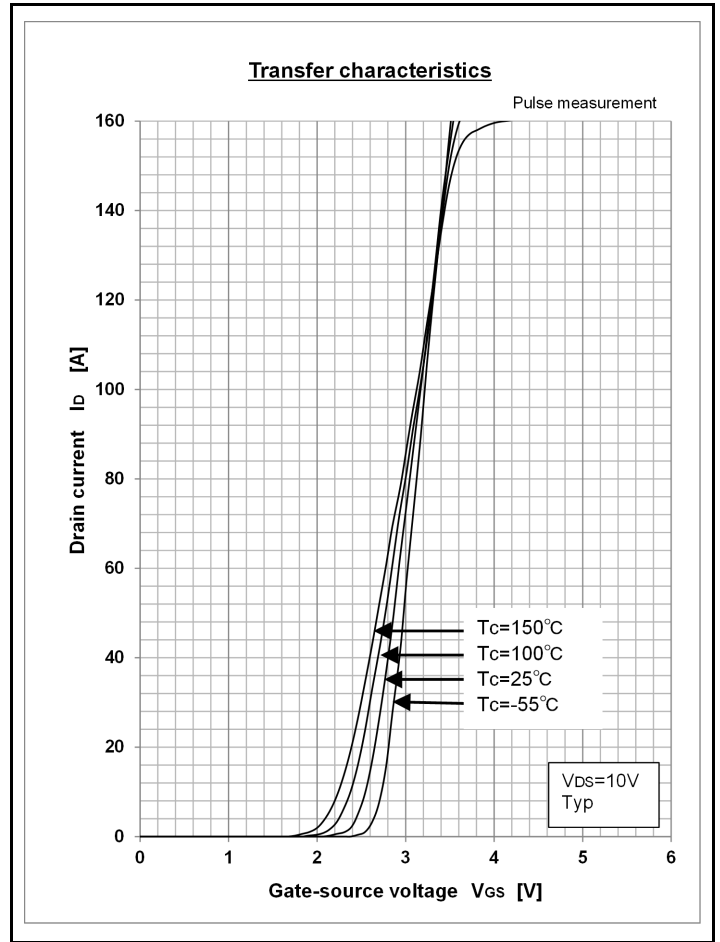
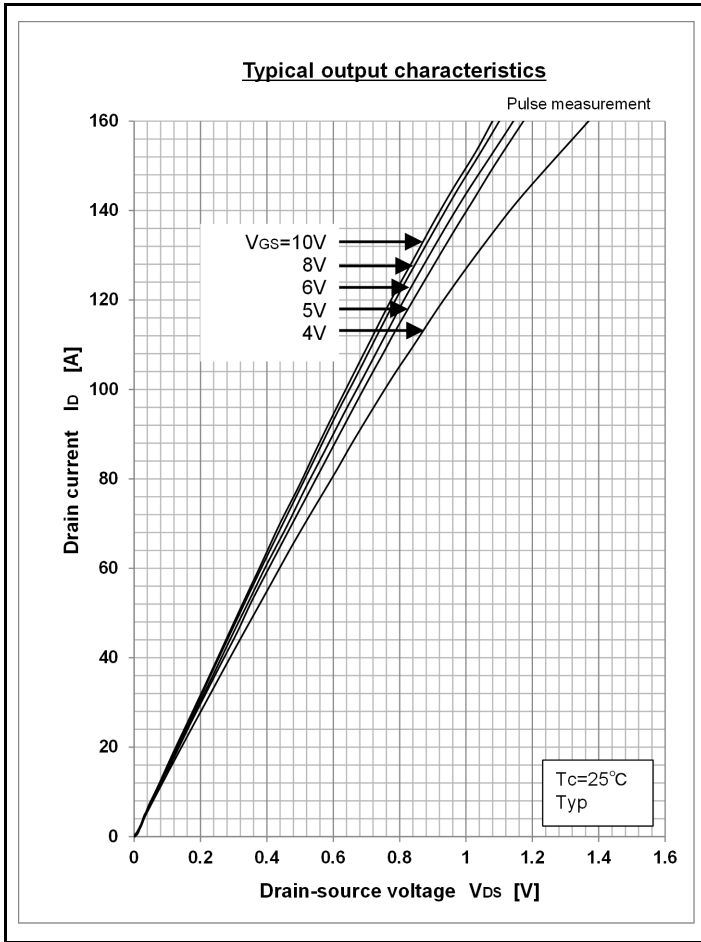
\* :See the original Specifications

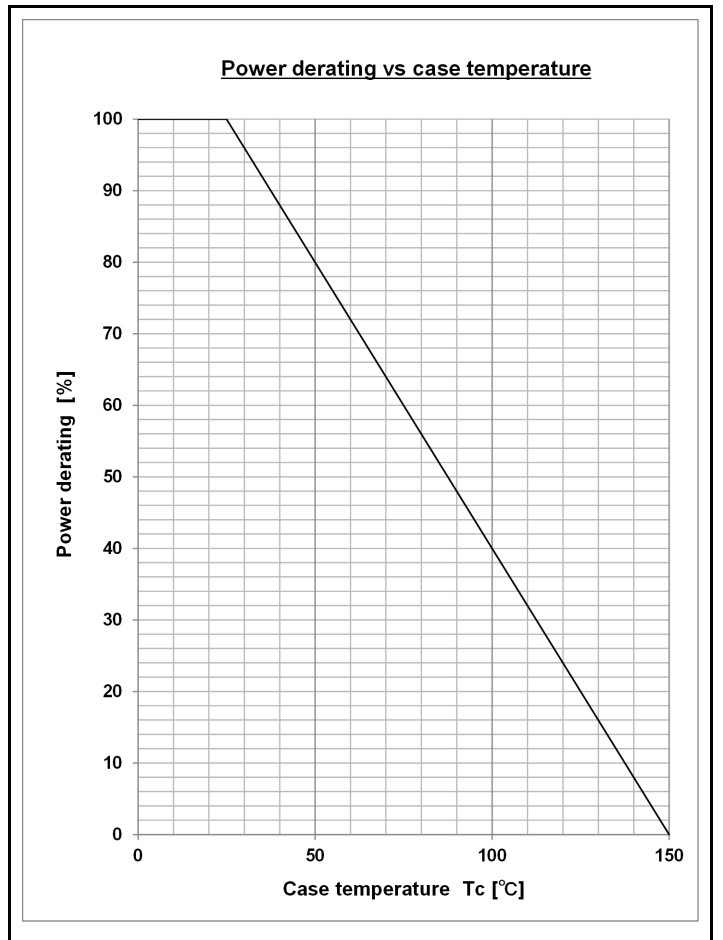
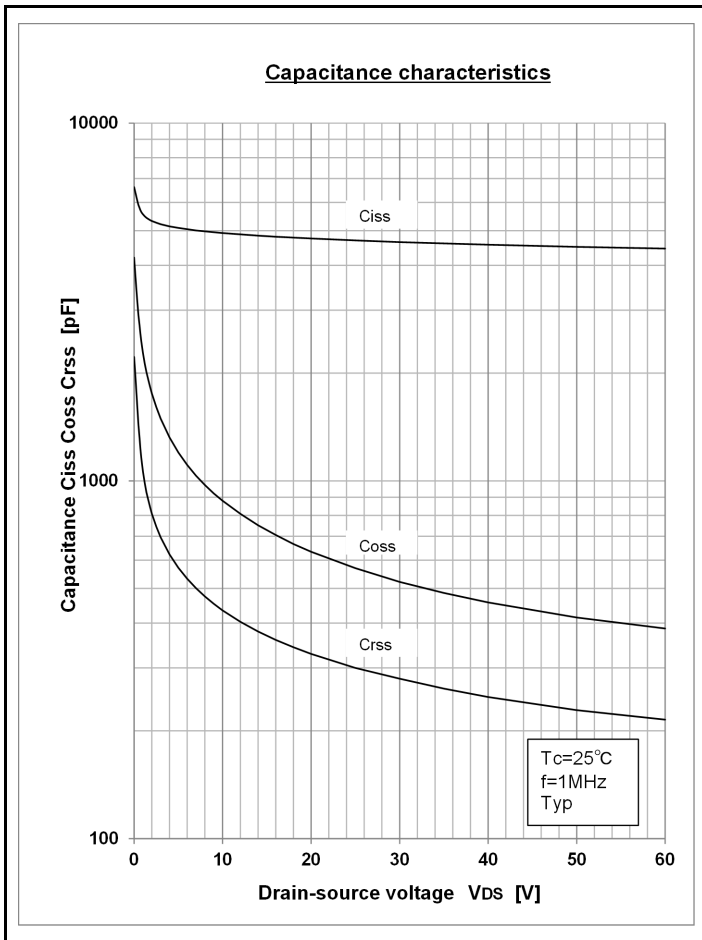
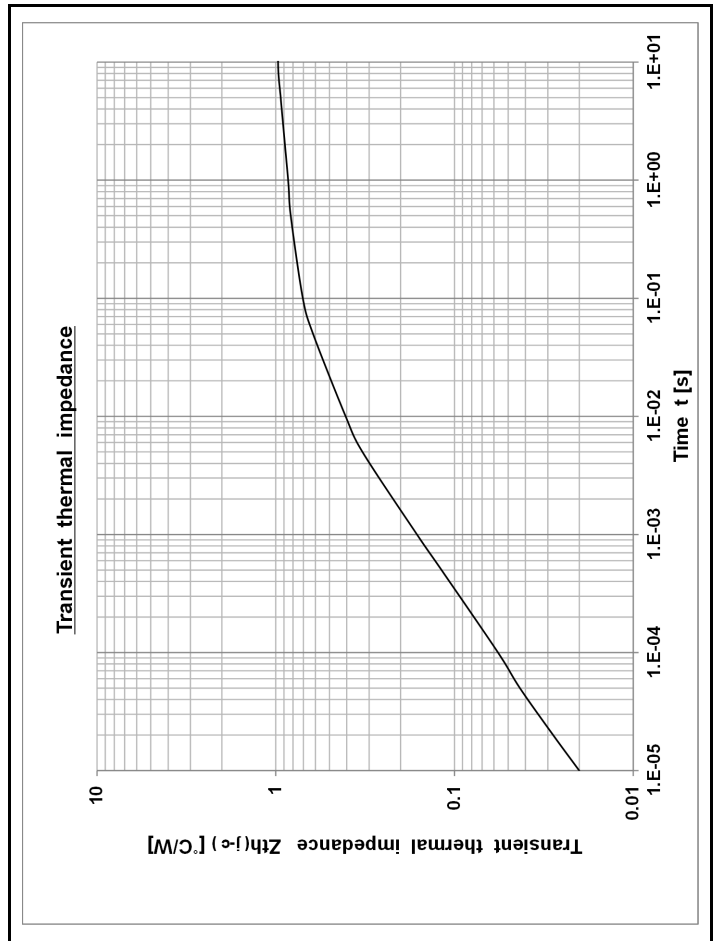
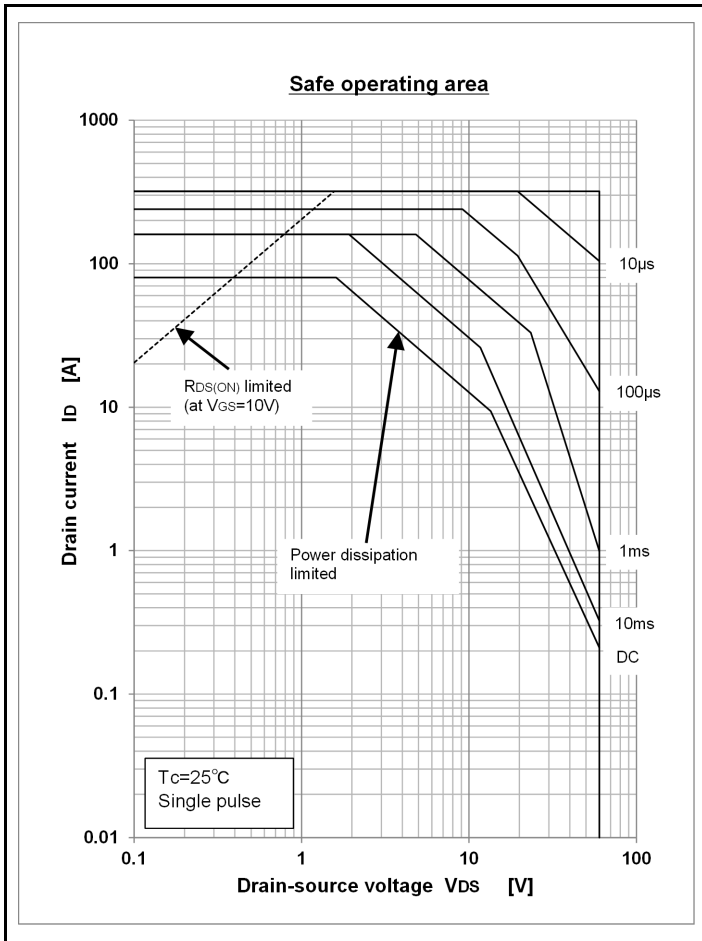
**Electrical Characteristics** (unless otherwise specified : Tc=25°C)

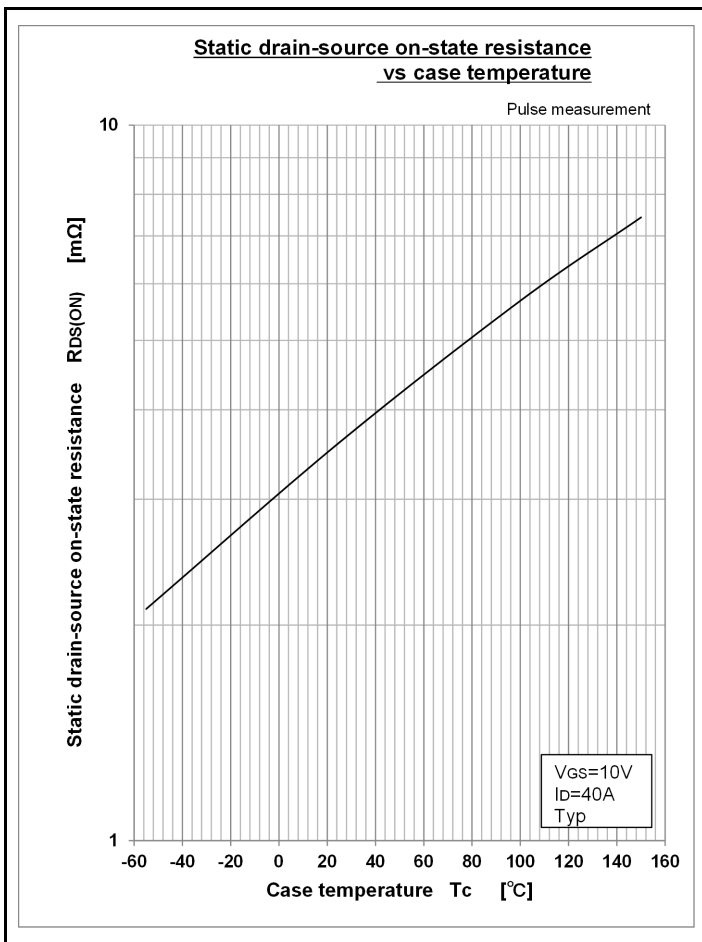
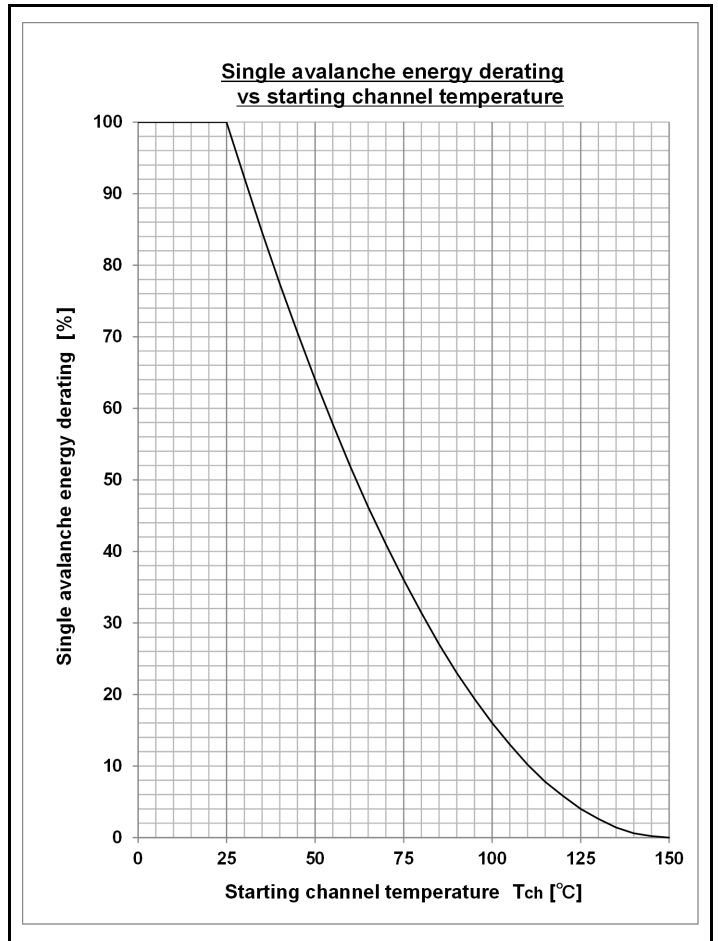
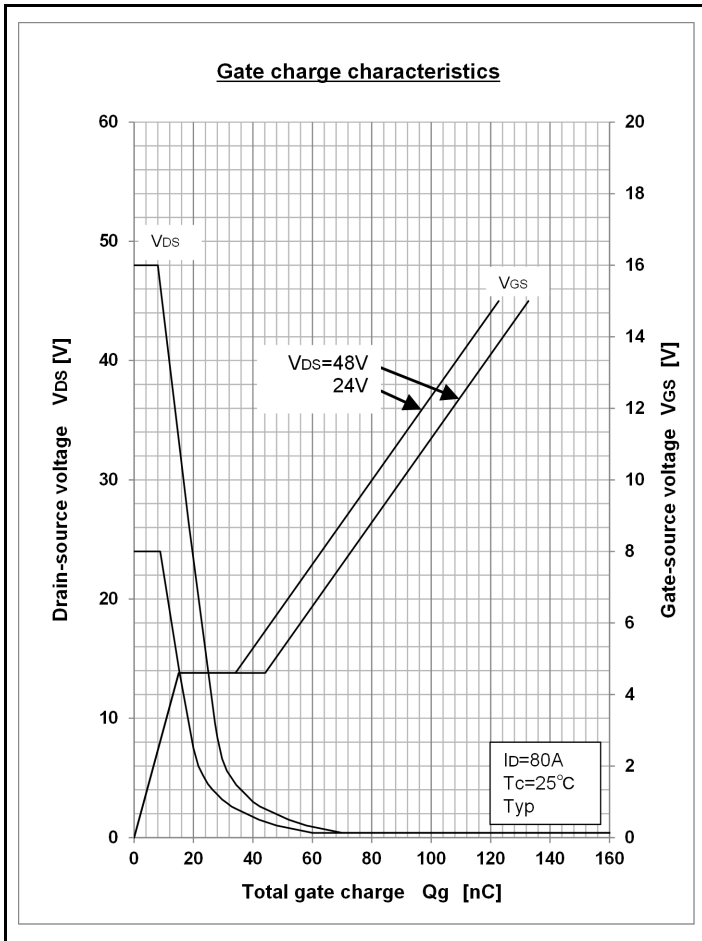
Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	60			V
Zero gate voltage drain current	$I_{DSS}$	VDS=60V, VGS=0V			1	μA
Gate-source leakage current	$I_{GSS}$	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	$g_{fs}$	ID=40A, VDS=10V	25	60		S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=40A, VGS=10V		0.0036	0.0049	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=40A, VGS=4.5V		0.0046	0.0065	Ω
Gate threshold voltage	$V_{th}$	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	$V_{SD}$	IS=80A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case			0.97	°C/W
Total gate charge	$Q_g$	VDD=48V, VGS=10V, ID=80A		90		nC
Gate to source charge	$Q_{gs}$	VDD=48V, VGS=10V, ID=80A		15		nC
Gate to drain charge	$Q_{gd}$	VDD=48V, VGS=10V, ID=80A		27		nC
Input capacitance	$C_{iss}$	VDS=25V, VGS=0V, f=1MHz		4700		pF
Reverse transfer capacitance	$C_{rss}$	VDS=25V, VGS=0V, f=1MHz		300		pF
Output capacitance	$C_{oss}$	VDS=25V, VGS=0V, f=1MHz		570		pF
Turn-on delay time	$t_{d(on)}$	ID=40A, RL=0.75Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		70		ns
Rise time	$t_r$	ID=40A, RL=0.75Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		325		ns
Turn-off delay time	$t_{d(off)}$	ID=40A, RL=0.75Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		380		ns
Fall time	$t_f$	ID=40A, RL=0.75Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		330		ns

※ : See the original Specifications

# CHARACTERISTIC DIAGRAMS

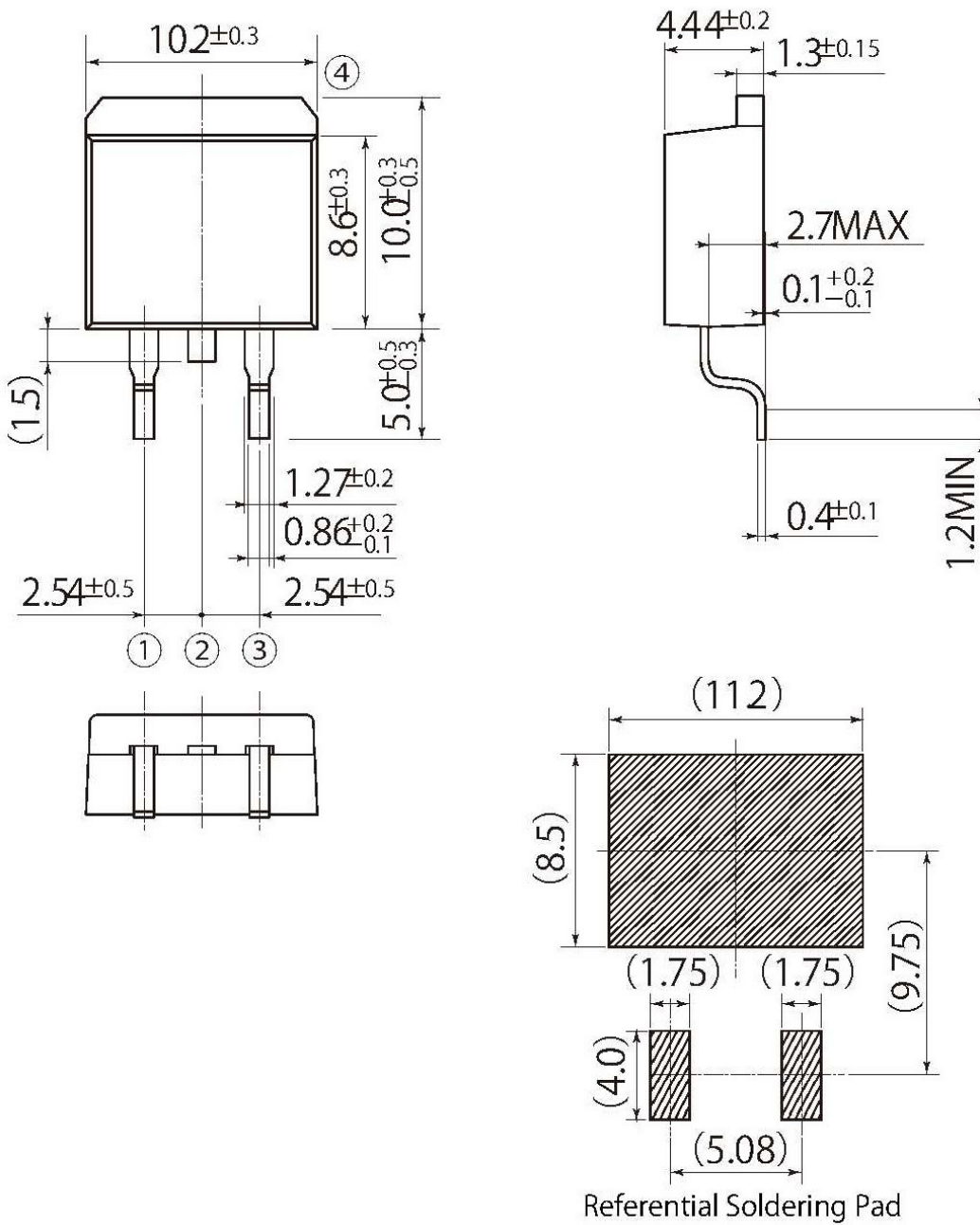






H4

JEDEC Code	TO-263AB
JEITA Code	-
House Name	FG



• Optimize soldering pad to the board design and soldering condition.

## Notes

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