ShinDengen

P175FP4SNK
Power MOSFETs
40V, 175A, N-channel

Feature

- N-channel
- SMD
- Large Current
- Low Ron
- 10V Gate Drive
- Low Capacitance
- Based on AEC-Q107
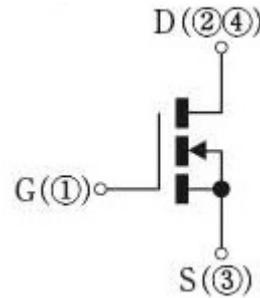- Halogen free
- Pb free terminal
- RoHS:Yes

OUTLINE

Package (House Name): FP
Package (JEITA Code): SC-83 similar

Equivalent circuit

Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	°C
Channel tempertature	Tch		175	°C
Drain-source voltage	V_{DSS}		40	V
Gate-source voltage	V_{GSS}		±20	V
Continuous drain current(DC)	I_D		175	A
Continuous drain current(Peak)	I_{DP}	Pulse width 10μs, duty=1/100	700	A
Total power dissipation	P_T		178	W
Single avalanche current	I_{AS}	Starting Tch=25°C Tch≦150°C	73	A
Single avalanche energy	E_{AS}	Starting Tch=25°C Tch≦150°C	598	mJ

※：See the original Specifications

Electrical Characteristics (unless otherwise specified : Tc=25°C)

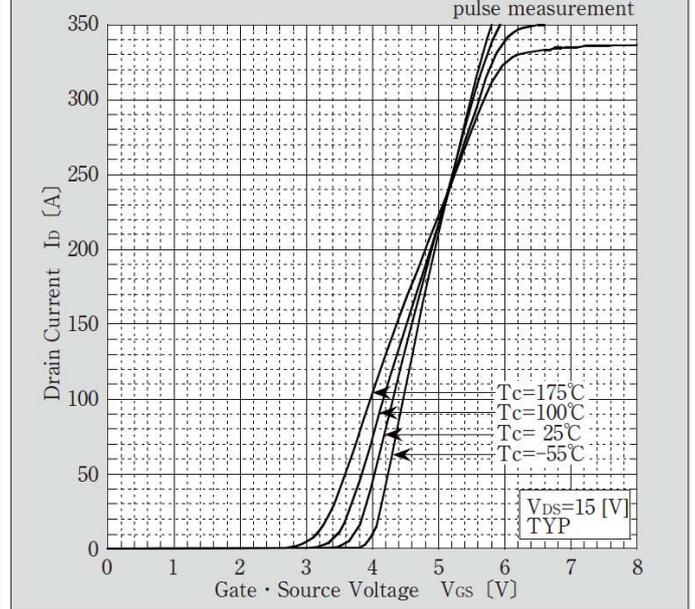| Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	40			V
Zero gate voltage drain current	I_{DSS}	VDS=40V, VGS=0V			1	µA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	µA
Forward transconductance	g_{fs}	ID=87.5A, VDS=10V	30			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=87.5A, VGS=10V		0.0013	0.0016	Ω
Gate threshold voltage	Vth	ID=1mA, VDS=10V	2	3	4	V
Source-drain diode forward voltage	V_{SD}	IS=175A, VGS=0V			1.5	V
Thermal resistance	Rth(j-c)	Junction to case			0.84	°C/W
Total gate charge	Qg	VDD=32V, VGS=10V, ID=175A		116		nC
Gate to source charge	Qgs	VDD=32V, VGS=10V, ID=175A		30		nC
Gate to drain charge	Qgd	VDD=32V, VGS=10V, ID=175A		47		nC
Input capacitance	Ciss	VDS=25V, VGS=0V, f=1MHz		5900		pF
Reverce transfer capacitnce	Crss	VDS=25V, VGS=0V, f=1MHz		590		pF
Output capacitance	Coss	VDS=25V, VGS=0V, f=1MHz		1100		pF
Turn-on delay time	td(on)	ID=87.5A, RL=0.23Ω, VDD=20V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		12		ns
Rise time	tr	ID=87.5A, RL=0.23Ω, VDD=20V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		117		ns
Turn-off delay time	td(off)	ID=87.5A, RL=0.23Ω, VDD=20V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		52		ns
Fall time	tf	ID=87.5A, RL=0.23Ω, VDD=20V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		32		ns
Diode reverse recovery time	trr	IF=175A, VGS=0V, di/dt=100A/µs		42		ns
Diode reverse recovery charge	Qrr	IF=175A, VGS=0V, di/dt=100A/µs		50		nC

※ : See the original Specifications
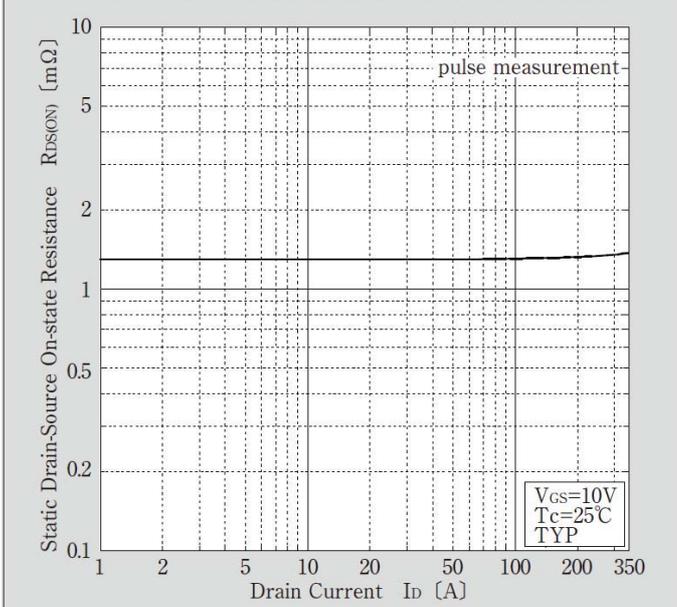
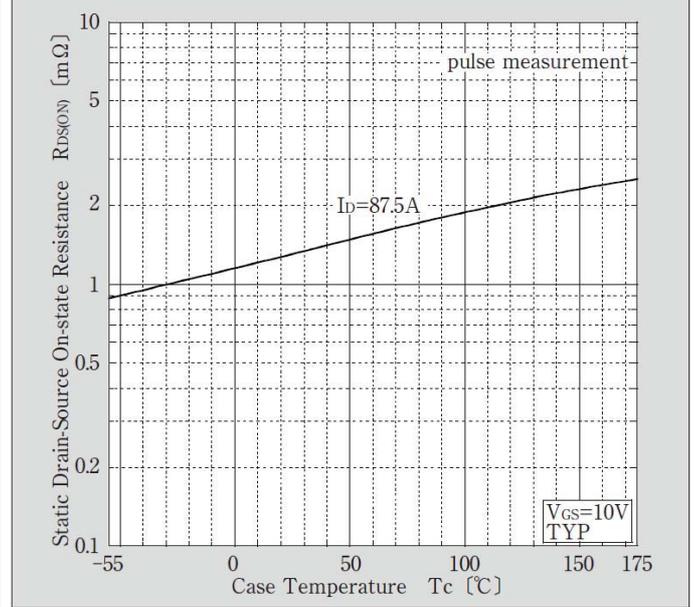## CHARACTERISTIC DIAGRAMS

Typical Output Characteristics

pulse measurement

Drain Current I_D [A] vs Drain・Source Voltage V_{DS} [V]

V_{GS}= 10V
8V
6V
V_{GS}= 5V

Tc=25℃
TYP
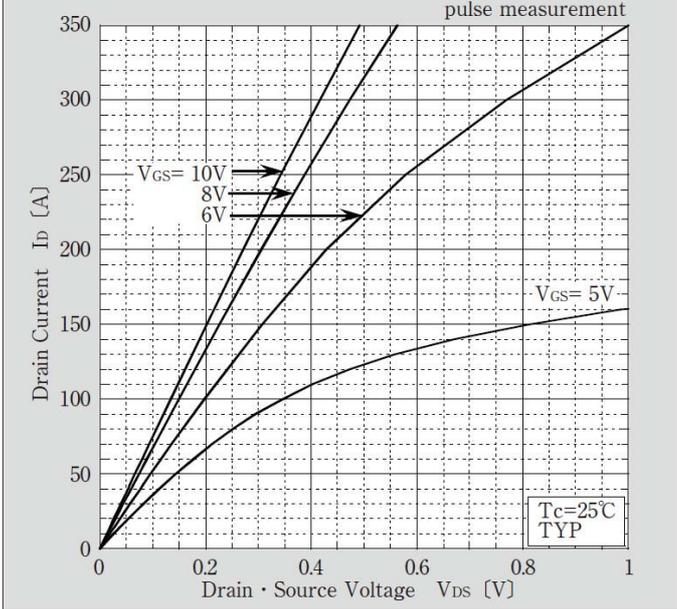
Transfer Characteristics

pulse measurement

Drain Current I_D [A] vs Gate・Source Voltage V_{GS} [V]

Tc=175℃
Tc=100℃
Tc= 25℃
Tc=−55℃

V_{DS}=15 [V]
TYP

Static Drain-Source On-state Resistance vs Drain Current

Static Drain-Source On-state Resistance $R_{DS(ON)}$ [mΩ] vs Drain Current I_D [A]

pulse measurement

V_{GS}=10V
Tc=25℃
TYP

Static Drain-Source On-state Resistance vs Case Temperature

Static Drain-Source On-state Resistance $R_{DS(ON)}$ [mΩ] vs Case Temperature Tc [℃]

pulse measurement

I_D=87.5A

V_{GS}=10V
TYP

Gate Threshold Voltage vs Case Temperature

Gate Threshold Voltage V_{TH} [V] vs Case Temperature T_c [°C]

pulse measurement

$V_{DS}=10V$
$I_D=1mA$
TYP

Safe Operating Area

Drain Current I_D [A] vs Drain · Source Voltage V_{DS} [V]

$R_{DS(ON)}$ Limited (at $V_{GS}=10V$)

Power Dissipation Limited

10 μs
100 μs
1ms
10ms
DC

$T_c=25°C$
single pulse

Transient Thermal Impedance
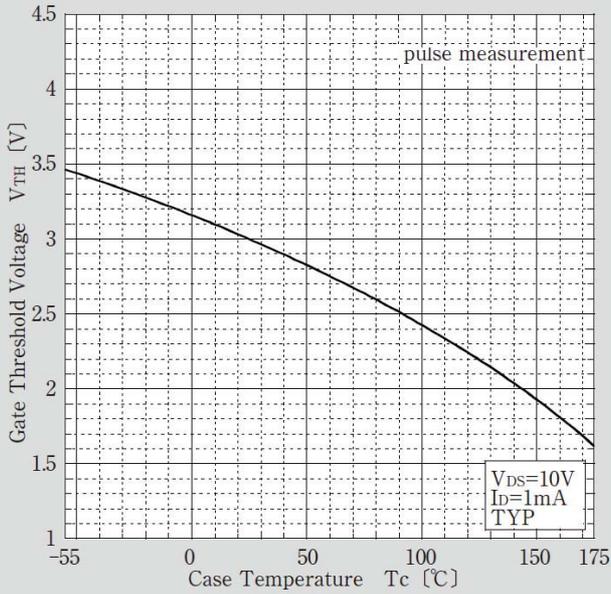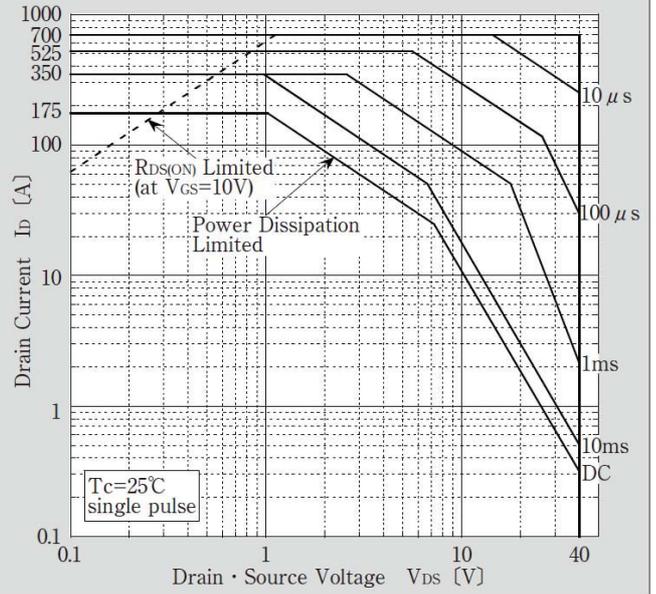
Transient Thermal Impedance θjc [°C／W] vs Time t [s]
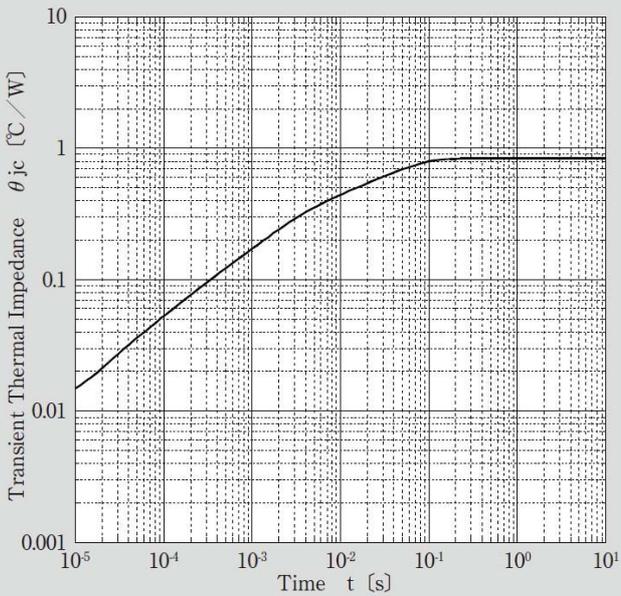
Capacitance Characteristics

Capacitance Ciss Coss Crss [pF] vs Drain · Source Voltage V_{DS} [V]

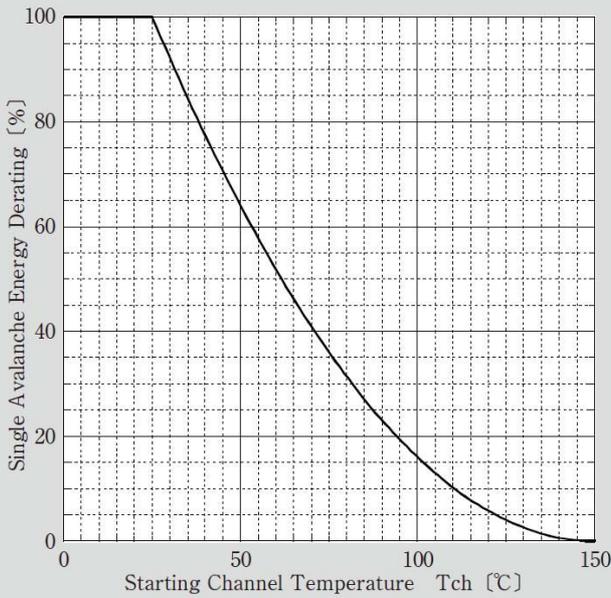Ciss
Coss
Crss

$T_c=25°C$
f=1MHz
TYP
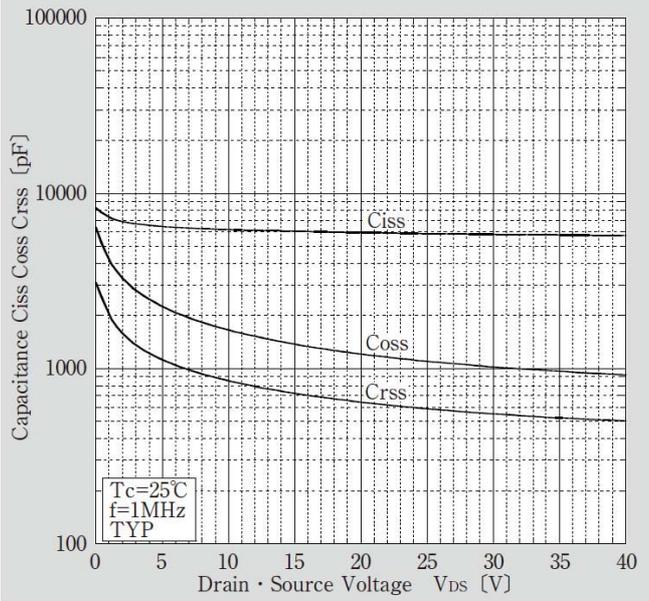
Power Derating - Case Temperature
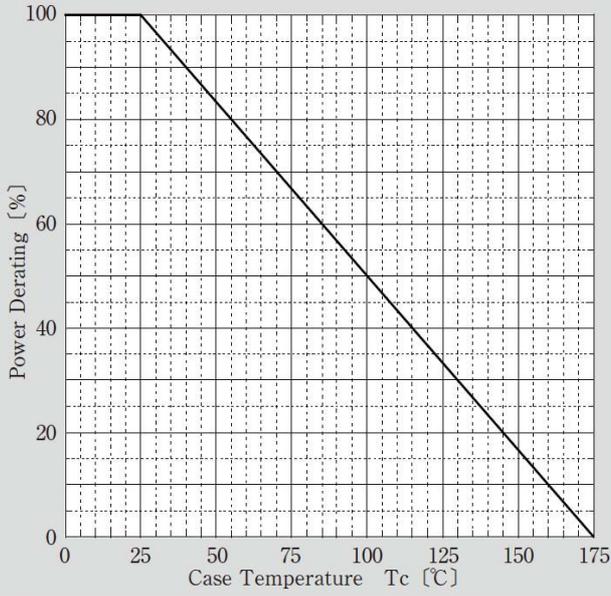
Gate Charge Characteristics
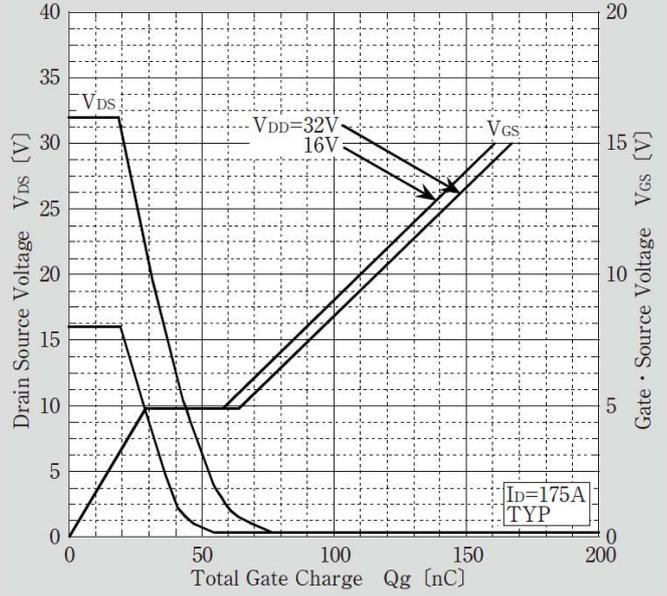
Single Avalanche Energy Derating vs Channel Temperature

unit:mm

scale: 3/1

H5

JEDEC Code	–
JEITA Code	SC-83 similar
House Name	FP

$10.2^{\pm0.2}$

④

$0.8^{\pm0.2}$

$9.3^{\pm0.2}$

$10.2^{\pm0.2}$

$1.3^{\pm0.2}$

$0.7^{\pm0.2}$

$2.2^{\pm0.2}$

$2.54^{\pm0.5}$

$2.34^{\pm0.5}$

① ② ③

$4.6^{\pm0.2}$

$0.5^{\pm0.2}$

$2.4^{\pm0.3}$

$0.1^{\pm0.1}$

$13.3^{\pm0.5}$

$\boxed{0.25}$

$0.60^{+0.3}_{0.1}$

$1.3^{\pm0.3}$

(11.2)

(8.5)

(2.1)

(9.0)

(1.75)

(2.75)

(2.54)

(2.34)
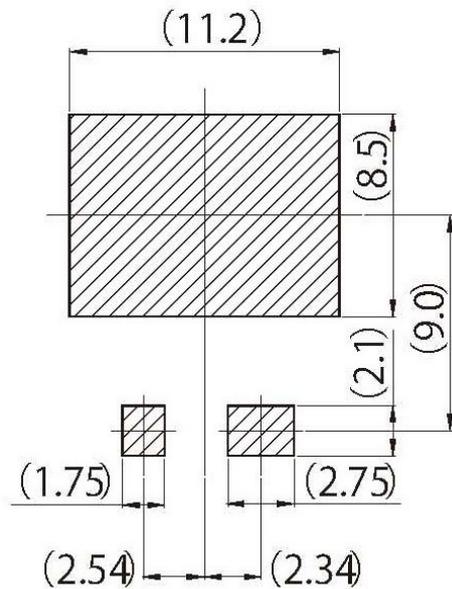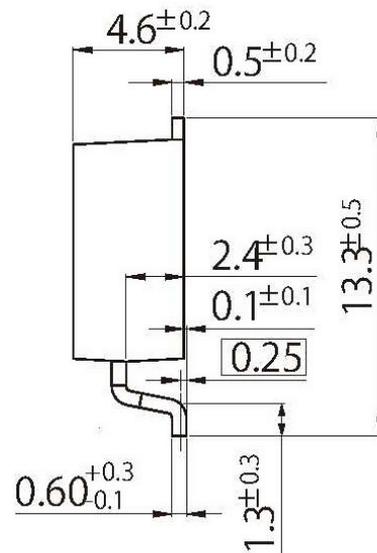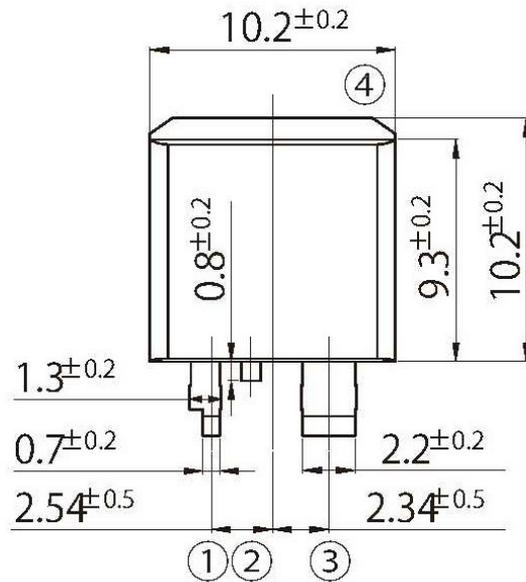
· Optimize soldering pad to the board design and soldering condition.

Notes

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