IXYS
INTEGRATED CIRCUITS DIVISION

IX4351NE
9A Low Side SiC MOSFET & IGBT Driver

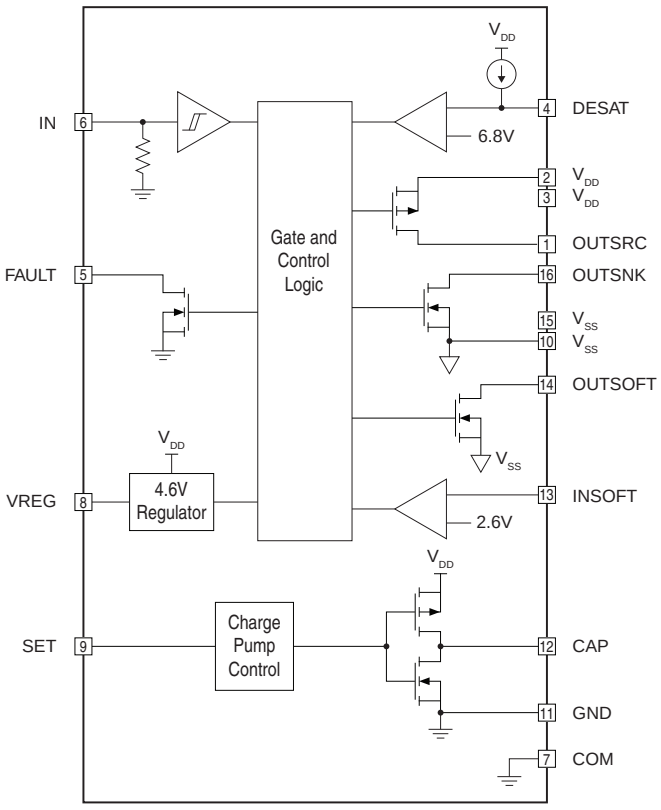
Features

- Separate 9A peak source and sink outputs
- Operating Voltage Range: -10V to +25V
- Internal charge pump regulator for selectable negative gate drive bias
- Desaturation detection with soft shutdown sink driver
- TTL and CMOS compatible input
- Under Voltage lockout (UVLO)
- Thermal shutdown
- Open drain FAULT output

Applications

- Driving SiC MOSFETs and IGBTs
- On-board charger and DC charging station
- Industrial inverters
- PFC, AC/DC and DC/DC converters

IX4351 Functional Block Diagram



Description

The IX4351NE is designed specifically to drive SiC MOSFETs and high power IGBTs. Separate 9A source and sink outputs allow for tailored turn-on and turn-off timing while minimizing switching losses. An internal negative charge regulator provides a selectable negative gate drive bias for improved dV/dt immunity and faster turn-off.

Desaturation detection circuitry detects an over current condition of the SiC MOSFET and initiates a soft turn off, thus preventing a potentially damaging dV/dt event. The logic input, IN, is TTL and CMOS compatible; this input does not need to be level shifted even with a negative gate drive bias voltage. Protection features include UVLO and thermal shutdown detection. An open drain FAULT output signals a fault condition to the microcontroller.

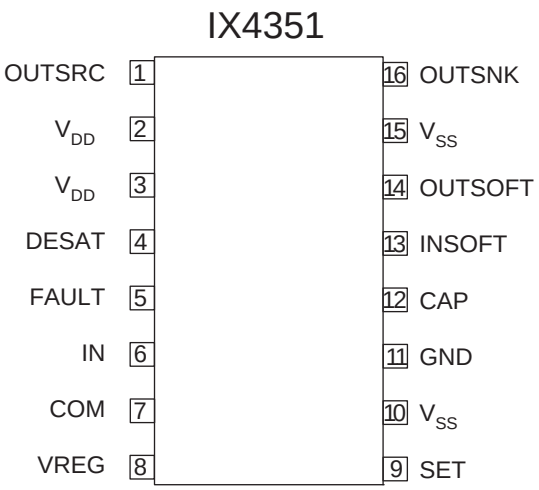
The IX4351NE is rated for an operational temperature range of -40°C to +125°C, and is available in a thermally enhanced 16-pin power SOIC package.

Ordering Information

Part	Description
IX4351NE	16-Pin power SOIC with exposed thermal pad. In tubes (50/Tube)
IX4351NETR	16-Pin power SOIC with exposed thermal pad. In Tape & Reel (2000/Reel)

1 Specifications

1.1 Package Pinout



1.2 Pin Description

Pin#	Name	Description
1	OUTSRC	Gate driver source output
2	V_{DD}	Positive supply voltage for gate driver outputs and logic circuitry
3	V_{DD}	Positive supply voltage for gate driver outputs and logic circuitry
4	DESAT	Sense input for the desaturation detection comparator
5	FAULT	Open-Drain Fault status output
6	IN	Logic input
7	COM	Common ground connection
8	VREG	4.6V regulator output
9	SET	Negative bias voltage set input
10	V_{SS}	Negative drive voltage supply
11	GND	Charge pump ground connection
12	CAP	Flying charge pump capacitor connection
13	INSOFT	Soft shutdown comparator input
14	OUTSOFT	Soft shutdown sink driver output
15	V_{SS}	Negative drive voltage supply
16	OUTSNK	Gate driver sink output

1.3 Absolute Maximum Ratings

With respect to V_{COM} unless otherwise specified.

Parameter	Symbol	Minimum	Maximum	Units
Positive Supply Voltage	V_{DD}	-0.3	32	V
Negative Supply Voltage	V_{SS}	-10	0	V
Supply Voltage Range	V_{DD} - V_{SS}	-0.3	40	V
Gate Drive Output Voltages	V_{OUTSRC} , V_{OUTSNK} , $V_{OUTSOFT}$	V_{SS} - 0.3	V_{DD} + 0.3	V
Gate Drive Output Current	I_{OUTSRC} , I_{OUTSNK}	-	±9	A
Logic Input Voltage	V_{IN}	-0.3	7	V
DESAT Input Voltage	V_{DESAT}	-0.3	V_{DD} + 0.3	V
SET Input Voltage	V_{SET}	- 1	7	V
FAULT Output Voltage	V_{FAULT}	-0.3	V_{DD} + 0.3	V
VREG Output Voltage	V_{VREG}	-0.3	7	V
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-55	+150	°C

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Positive Supply Voltage	V_{DD}	13	25	V
Negative Supply Voltage	V_{SS}	-10	0	V
Input Voltage	V_{IN}	0	5.5	V
Operating Ambient Temperature	T_A	-40	125	°C

1.5 Electrical Characteristics

(V_{DD}=20V, V_{SS}=-5V, COM=GND=0V, C_{DD}=C_{REG}=4.7µF, C_{SS}=10µF, T_A=-40°C to +125°C, unless otherwise specified.)

1.5.1 V_{DD} Section

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Operating V_{DD} Supply Current	f_{IN}=100kHz, C_{LOAD}=2.2nF	I_{DD}	-	19	28	mA
Quiescent V_{DD} Supply Current	No load	I_{DDQ}	-	2.9	4.4	mA
V_{DD} UVLO Rising Threshold	-	V_{DDUV+}	10	12	13	V
V_{DD} UVLO Hysteresis	-	V_{DDHYS}	-	2	-	V

1.5.2 V_{REG} Section

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Regulator Output Voltage	I_{VREG}=-5mA	V_{VREG}	4.2	4.6	5	V
Line Regulation	15V < V_{DD} < 25V, I_{VREG}=-5mA	ΔV_{VREG}	-	0.1	0.2	V
Load Regulation	I_{VREG}=-1mA to -10mA		-	0.1	0.4	V

1.5.3 Charge Pump Section

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Negative Bias Rail Voltage Range	-	V_{SS}	-8	-	-3.5	V
Maximum V_{SS} Current	C_{FLY}=66nF, R_{FLY}=33Ω	I_{SS}	-	-	50	mA
Charge Pump Frequency	-	f_{OSC}	90	124	160	kHz

1.5.4 Desaturation Section

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
DESAT Source Current	V_{DESAT}=0V	I_{DESAT}	400	570	750	µA
DESAT Threshold Voltage	-	$V_{TH,DESAT}$	6	6.8	8	V
Blanking Time	-	t_{BLANK}	-	250	-	ns
DESAT Pull Down Resistance	-	R_{DESAT}*	-	900	-	Ω

* External component

1.5.5 Thermal Shutdown Section

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Thermal Shutdown Temperature	-	TSD	-	160	-	°C
Thermal Shutdown Hysteresis	-	TSD_{HYS}	-	20	-	°C

1.5.6 Logic Input Section

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
High Level Input Voltage	-	V_{INH}	2.2	-	-	V
Low Level Input Voltage	-	V_{INL}	-	-	1	V
Input Hysteresis	-	V_{INHYS}	0.2	0.4	-	V
High Level Input Current	V_{IN}=5V	I_{INH}	-	-	70	µA
Low Level Input Current	V_{IN}=0V	I_{INL}	-	-	-10	µA
Input Pull-Down Resistance	-	R_{IN}	-	100	-	kΩ

1.5.7 FAULT Section

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Output Low Voltage	I_{FAULT}=20mA	V_{FAULTL}	-	-	0.8	V
Output Leakage Current	V_{FAULT}=20V	I_{FAULT}	-	0.1	10	µA
DESAT Detect to FAULT Delay	-	$t_{FAULTDLY}$	-	150	-	ns

1.5.8 Soft Shutdown Section

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Soft Shutdown Threshold Voltage	-	$V_{TH,INSOFT}$	2.3	2.6	3	V
Soft Shutdown Hysteresis	-	$V_{INSOFTHYS}$	-	0.4	-	V
OUTSOFT Peak Sink Current	-	$I_{OUTSOFT}$	-	900	-	mA
OUTSOFT On-Resistance	$I_{OUTSOFT}$=100mA	$R_{OUTSOFT}$	-	6	15	Ω
DESAT Detect to OUTSOFT Delay	-	$t_{OUTSOFTDLY}$	-	125	-	ns

1.5.9 Gate Driver Section

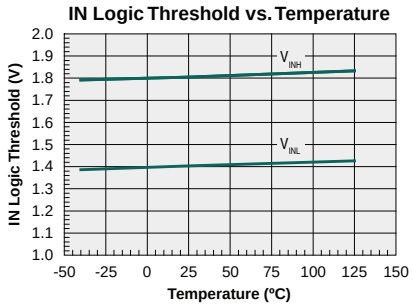
Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
High Level Output Voltage	I_{OUTSRC}=-100mA	V_{OUTSRC}	V_{DD}- 0.25	-	-	V
Low Level Output Voltage	I_{OUTSNK}=100mA	V_{OUTSNK}	-	-	0.25	V
OUTSRC ON-Resistance	I_{OUTSRC}=-100mA	R_{OUTSRC}	-	1.16	2	Ω
OUTSNK ON-Resistance	I_{OUTSNK}=100mA	R_{OUTSNK}	-	0.8	1.5	Ω
Turn-On Propagation Delay Time	C_{LOAD}=1nF	t_{ON}	-	75	125	ns
Turn-Off Propagation Delay Time	C_{LOAD}=1nF	t_{OFF}	-	65	125	ns
Turn-On Rise Time	C_{LOAD}=1nF	t_R	-	10	20	ns
Turn-Off Fall Time	C_{LOAD}=1nF	t_F	-	10	20	ns

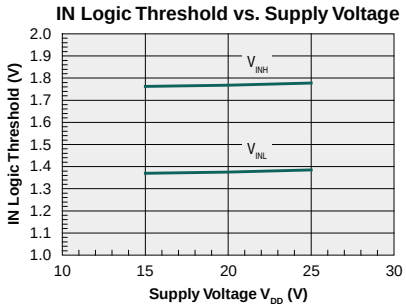
1.6 Thermal Characteristics

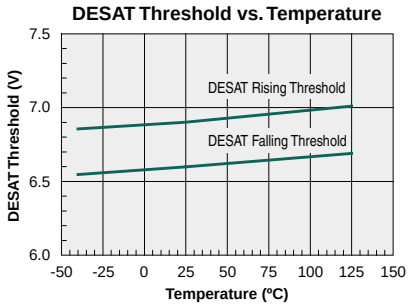
Parameter	Symbol	Rating	Units
Thermal Impedance, Junction to Ambient	θ_{JA}	60	°C/W
Thermal Impedance, Junction to Case	θ_{JC}	28	°C/W

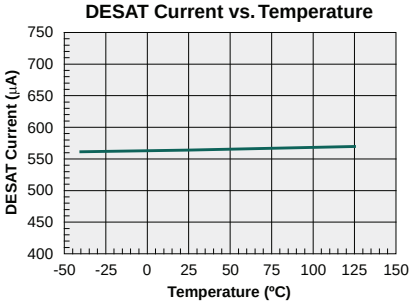
2 Performance Data

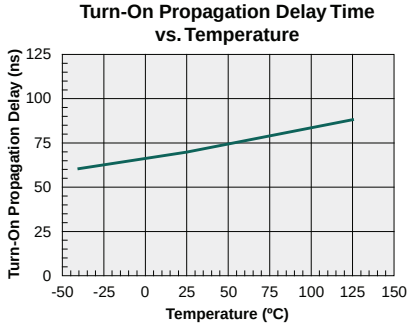
At 25°C and V_{DD}=20V unless otherwise noted.

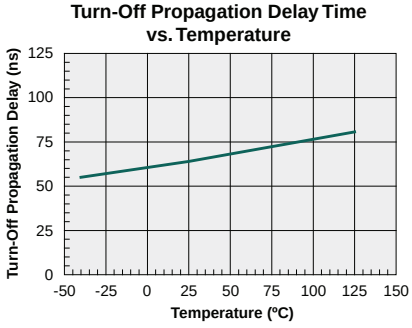


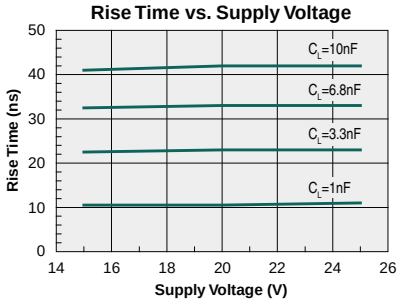


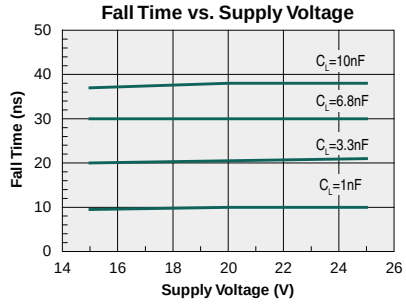


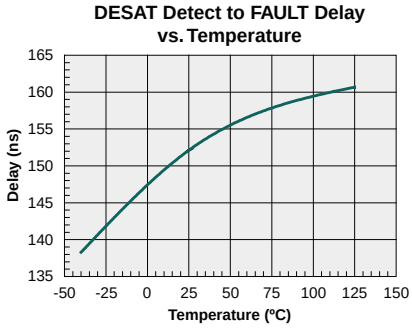


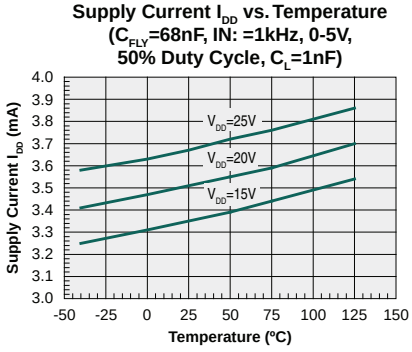


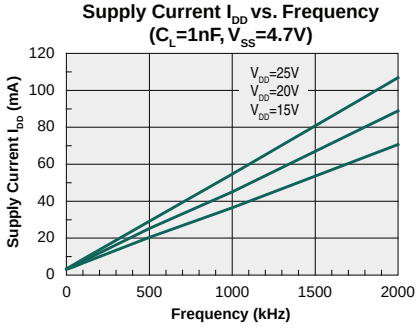








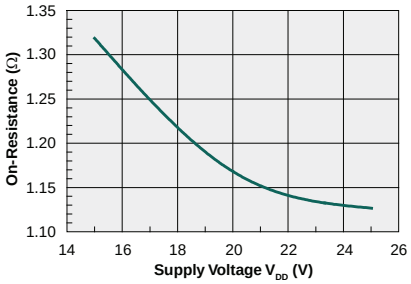




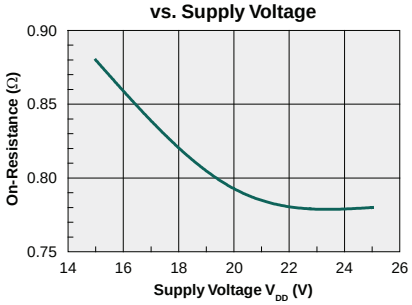
3 Performance Data (Cont.)

At 25°C and V_{DD}=20V unless otherwise noted.

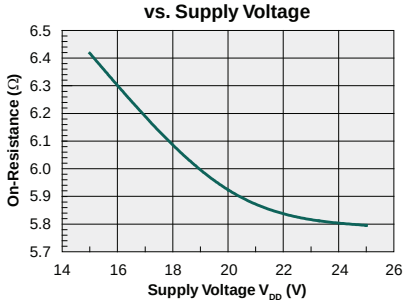
OUTSRC On-Resistance vs. Supply Voltage



OUTSNK On-Resistance vs. Supply Voltage



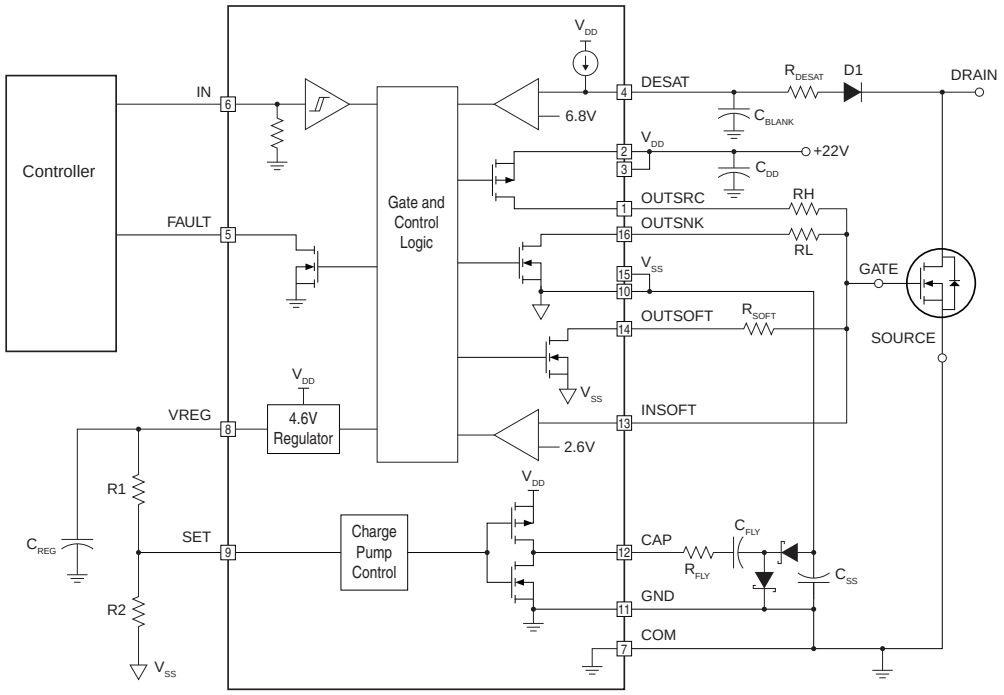
OUTSOFT On-Resistance vs. Supply Voltage



4 Functional Description

The IX4351NE is designed to provide the gate drive for high power SiC MOSFETs and IGBTs.

Figure 1. IX4351NE Typical Application Circuit



4.1 Logic Input (IN)

The logic input IN controls the state of the high current source driver output (OUTSRC), high current sink driver output (OUTSNK), and the lower current sink driver output (OUTSOFT). The IN input is a high-speed Schmitt trigger buffer with 0.4V hysteresis. The IN logic thresholds are TTL and CMOS compatible, and are referenced to COM. When V_{DD} is greater than the V_{DD} UVLO rising threshold (V_{DDUV+}), typically 12V, IN controls the state of the gate driver outputs according to Table 1:

4.1.1 Table 1

IN	V_{DD}	OUTSRC	OUTSNK	OUTSOFT
X	< V_{DDUV+}	Off	Low	Low
0	> V_{DDUV+}	Off	Low	Low
1	> V_{DDUV+}	High	Off	Off

4.2 Gate Drive Outputs (OUTSRC and OUTSNK)

The IX4351NE power outputs are rated for 9A peak current capability. Separate source and sink outputs allow independent adjustment of the discrete SiC MOSFET or IGBT turn-on and turn-off transactions with a single resistor. An internal dead time prevents cross conduction of the source and sink outputs.

4.3 Internal 4.6V Regulator (VREG)

The internal 4.6V regulator provides power for the low voltage control circuitry. An external 4.7µF bypass capacitor (C_{REG}) is required. VREG can source up to 10mA, that can be used to set the negative bias voltage and power an external logic optocoupler.

4.4 Negative V_{SS} Charge Pump Regulator

The IX4351NE has an inverting charge pump regulator that produces a negative regulated V_{SS} output. The charge pump operates in a closed-loop mode creating V_{SS} from V_{DD}. Charge pump output regulation is achieved by sensing the V_{SS} voltage through resistor divider R1 and R2. The charge pump requires an external flying capacitor (C_{FLY}), two discrete Schottky diodes, a storage capacitor (C_{SS}), and a peak current limiting resistor (R_{FLY}). V_{SS} is set by the R1 and R2 resistor divider:

$$V_{SS} = -V_{VREG} \bullet \left(\frac{R2}{R1}\right)$$

4.5 Desaturation Detection and Protection

The desaturation protection circuit ensures the protection of the external SiC MOSFET or IGBT in the event of an over-current situation. The DESAT pin monitors the drain voltage of the power SiC MOSFET or the collector of the power IGBT via R_{DESAT} and D1. If the drain or collector voltage exceeds the DESAT Threshold Voltage ($V_{TH,DESAT}$), typically 6.8V, a controlled turn-off sequence is initiated. OUTSRC is turned off and OUTSOFT is turned on. The 900mA sink capability of OUTSOFT allows an initial slow turn-off of the external SiC MOSFET or IGBT. When the GATE voltage decreases to the Soft Shutdown Threshold Voltage ($V_{TH,INSOFT}$), typically 2.6V, OUTSNK turns on and quickly pulls the GATE to V_{SS}. This two-step turn-off avoids dangerous dV/dt over-voltages across the external SiC MOSFET or IGBT.

The DESAT comparator is disabled for a fixed blanking time (t_{BLANK}) to avoid detecting a false desaturation event during the external SiC MOSFET or IGBT turn-on. The nominal t_{BLANK} is 250ns, which can be increased by adjusting R_{DESAT} and C_{BLANK}. This blanking time starts when IN transitions from low to high.

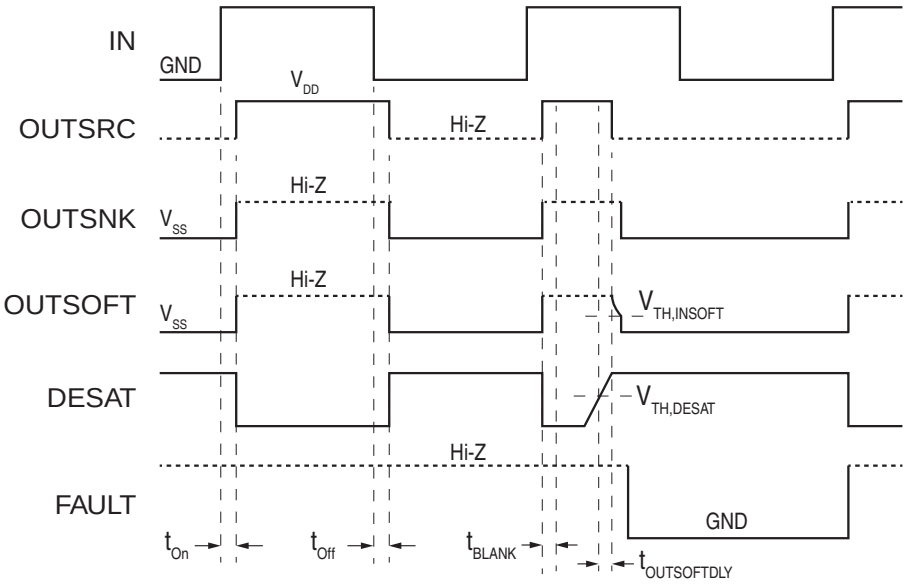
4.6 Thermal Shutdown

Thermal protection circuity turns off OUTSRC and turns on OUTSNK and OUTSOFT when the IX4351NE internal junction temperature reaches a nominal +160°C. OUTSRC is re-enabled when the internal junction temperature cools to approximately +140°C.

4.7 FAULT Output

The FAULT output signals whenever the IX4351NE is undergoing a fault condition. The open-drain NMOS is pulled low when $V_{DD} < V_{DDUV+}$, $T_J \geq TSD$, or desaturation is detected. FAULT is deactivated when the fault condition is remedied.

Figure 2. Timing Diagram



5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX4351NE	MSL 1

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

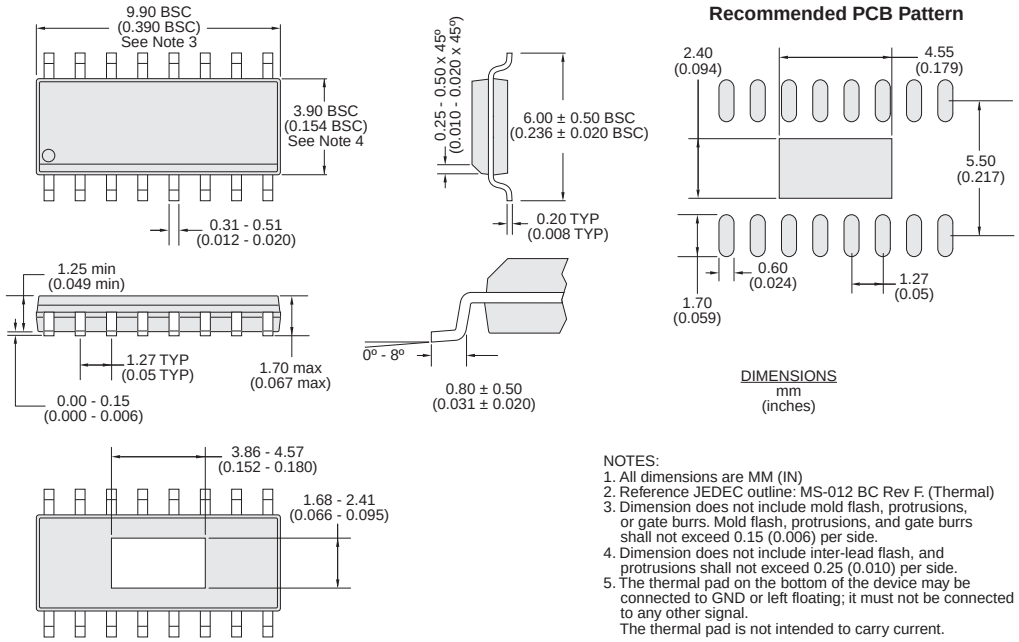
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IX4351NE	260°C	30 seconds	3

5.4 Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

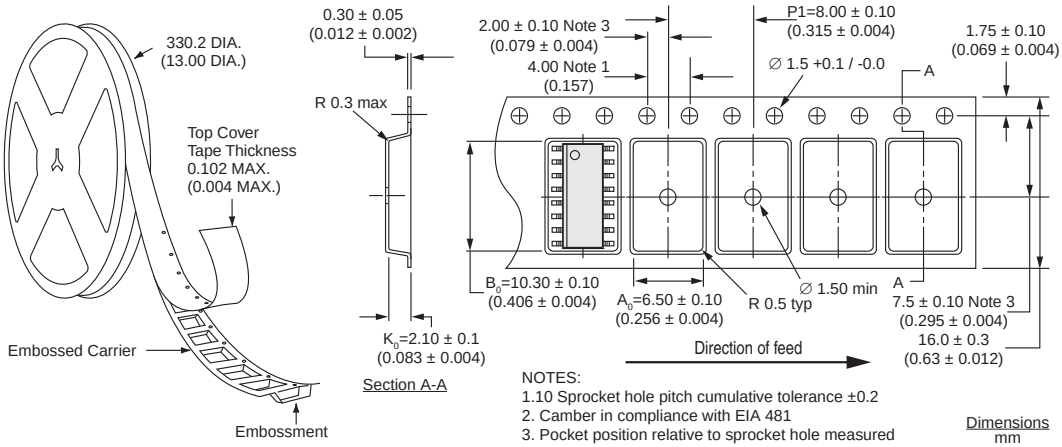
5.5 Mechanical Dimensions

5.5.1 IX4351NE 16-Pin SOIC Package



NOTES:
1. All dimensions are MM (IN)
2. Reference JEDEC outline: MS-012 BC Rev F. (Thermal)
3. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 (0.006) per side.
4. Dimension does not include inter-lead flash, and protrusions shall not exceed 0.25 (0.010) per side.
5. The thermal pad on the bottom of the device may be connected to GND or left floating; it must not be connected to any other signal.
   The thermal pad is not intended to carry current.

5.5.2 IX4351NETR Tape & Reel Packaging for 16-Pin SOIC Package



NOTES:
1.10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions
mm
(inches)

For additional information please visit our website at: www.ixysic.com

IXYS
A Littelfuse Technology

Specification: DS-IX4351NE-R02

2/13/2020