



# UTT50N06

*Power MOSFET*

## 50A, 60V N-CHANNEL POWER MOSFET

■ DESCRIPTION

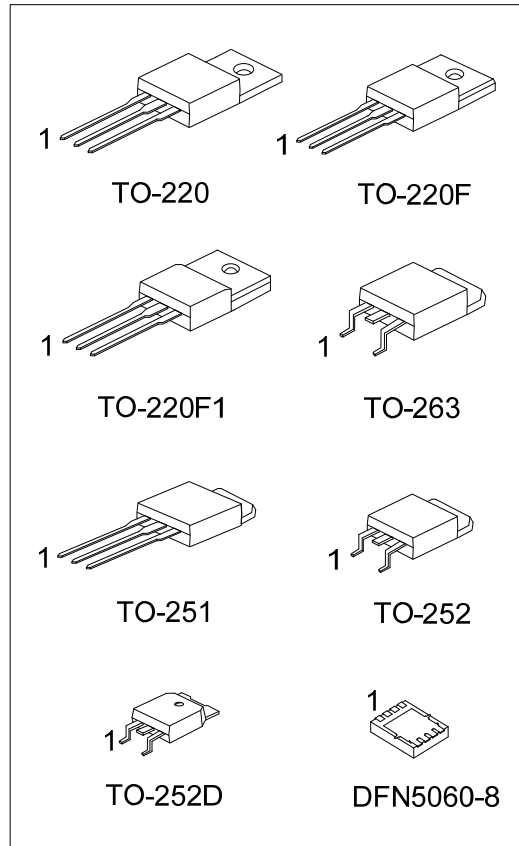
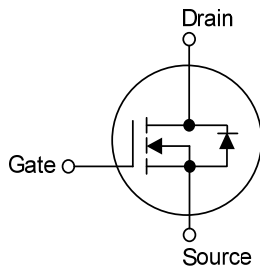
The UTC **UTT50N06** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

The UTC **UTT50N06** is generally applied in low power switching mode power appliances and electronic ballast.

■ FEATURES

- \*  $R_{DS(ON)} \leq 20 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=25\text{A}$
- $R_{DS(ON)} \leq 30 \text{ m}\Omega @ V_{GS}=4.5\text{V}, I_D=25\text{A}$
- \* High Switching Speed
- \* Improved dv/dt capability

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing	
Lead Free	Halogen Free		1	2	3	4	5	6	7	8		
UTT50N06L-TA3-T	UTT50N06G-TA3-T	TO-220	G	D	S	-	-	-	-	-	-	Tube
UTT50N06L-TF3-T	UTT50N06G-TF3-T	TO-220F	G	D	S	-	-	-	-	-	-	Tube
UTT50N06L-TF1-T	UTT50N06G-TF1-T	TO-220F1	G	D	S	-	-	-	-	-	-	Tube
UTT50N06L-TM3-T	UTT50N06G-TM3-T	TO-251	G	D	S	-	-	-	-	-	-	Tube
UTT50N06L-TN3-R	UTT50N06G-TN3-R	TO-252	G	D	S	-	-	-	-	-	-	Tape Reel
UTT50N06L-TND-R	UTT50N06G-TND-R	TO-252D	G	D	S	-	-	-	-	-	-	Tape Reel
UTT50N06L-TQ2-T	UTT50N06G-TQ2-T	TO-263	G	D	S	-	-	-	-	-	-	Tube
UTT50N06L-TQ2-R	UTT50N06G-TQ2-R	TO-263	G	D	S	-	-	-	-	-	-	Tape Reel
UTT50N06L-K08-5060-R	UTT50N06G-K08-5060-R	DFN5060-8	S	S	S	G	D	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UTT50N06G-TA3-T</p>	<p>(1) T: Tube, R: Tape Reel                  (2) TA3: TO-220, TF3: TO-220F, TF1: TO-220F1                  TM3: TO-251, TN3: TO-252, TND: TO-252D,                  TQ2: TO-263, K08-5060: DFN5060-8                  (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING

TO-220 / TO-220F / TO-220F1 / TO-251 TO-252 / TO-252D / TO-263	DFN5060-8

■ ABSOLUTE MAXIMUM RATINGS (( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	60	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Continuous Drain Current		$I_D$	50	A
Pulsed Drain Current (Note 2)		$I_{DM}$	100	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	48	mJ
Peak Diode Recovery dv/dt		dv/dt	10	V/ns
Power Dissipation	TO-220/TO-263	$P_D$	100	W
	TO-220F/TO-220F1		36	W
	TO-251/TO-252		46	W
	TO-252D			
	DFN5060-8		20.8	W
Junction Temperature		$T_J$	+150	$^{\circ}\text{C}$
Operation and Storage Temperature		$T_{STG}$	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3.  $L=0.1\text{mH}$ ,  $I_{AS}=31\text{A}$ ,  $V_{DD}=25\text{V}$ ,  $R_G=20\Omega$ , Starting  $T_J=25^{\circ}\text{C}$

4.  $I_{SD} \leq 30\text{A}$ ,  $V_{DS}=0\text{V}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient	TO-220/TO-220F TO-220F1/TO-263	$\theta_{JA}$	62	$^{\circ}\text{C}/\text{W}$
	TO-251/TO-252 TO-252D		100	$^{\circ}\text{C}/\text{W}$
	DFN5060-8		65	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-220/TO-263	$\theta_{JC}$	1.24	$^{\circ}\text{C}/\text{W}$
	TO-220F/TO-220F1		3.47	$^{\circ}\text{C}/\text{W}$
	TO-251/TO-252 TO-252D		2.7 (Note)	$^{\circ}\text{C}/\text{W}$
	DFN5060-8		6 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate  $P_C$  board, 2oz copper, with 1inch square copper plate.

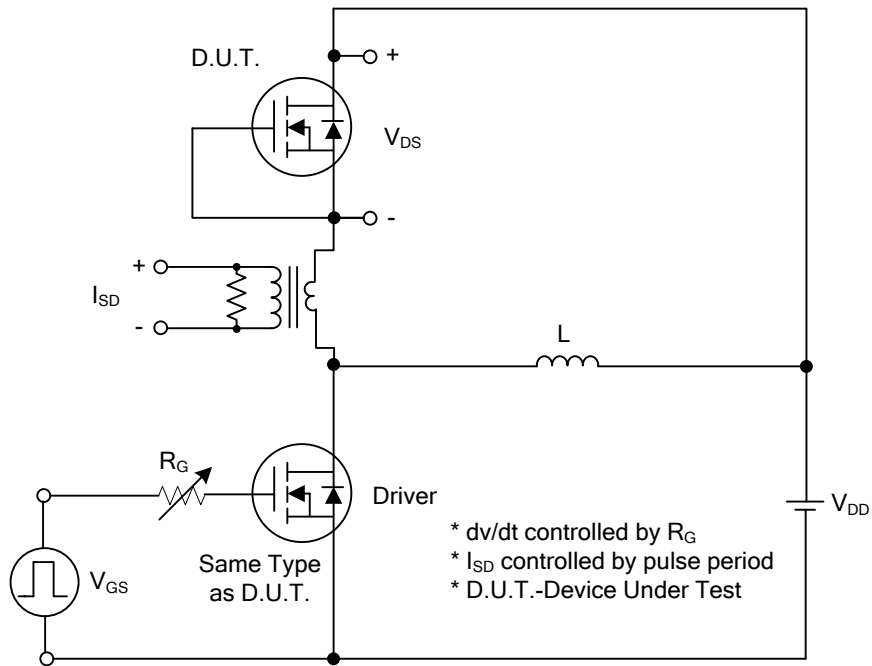
■ ELECTRICAL CHARACTERISTICS (T<sub>J</sub>= 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			10	μA
Gate-Source Leakage Current	Forward	I <sub>GSS</sub> V <sub>GS</sub> =20V, V <sub>DS</sub> =0V			100	nA
	Reverse				-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =25A			20	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =25A			30	mΩ
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz		1256		pF
Output Capacitance	C <sub>OSS</sub>			134		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			112		pF
<b>SWITCHING CHARACTERISTICS</b>						
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> =48V, V <sub>GS</sub> =10V, I <sub>D</sub> =50A I <sub>G</sub> =1mA (Note1,2)		40		nC
Gate-Source Charge	Q <sub>GS</sub>			5		nC
Gate-Drain Charge	Q <sub>GD</sub>			14		nC
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =10V, I <sub>D</sub> =50A, R <sub>G</sub> =4.7Ω (Note1,2)		10		ns
Turn-On Rise Time	t <sub>R</sub>			19		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			33		ns
Turn-Off Fall Time	t <sub>F</sub>			25		ns
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>				50	A
Maximum Pulsed Drain-Source Diode Forward Current	I <sub>SM</sub>				100	A
Drain-Source Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =50A, V <sub>GS</sub> =0V			1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>S</sub> =30A, V <sub>GS</sub> =0V,		40		ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	dI <sub>S</sub> /dt=100A/μs		70		nC

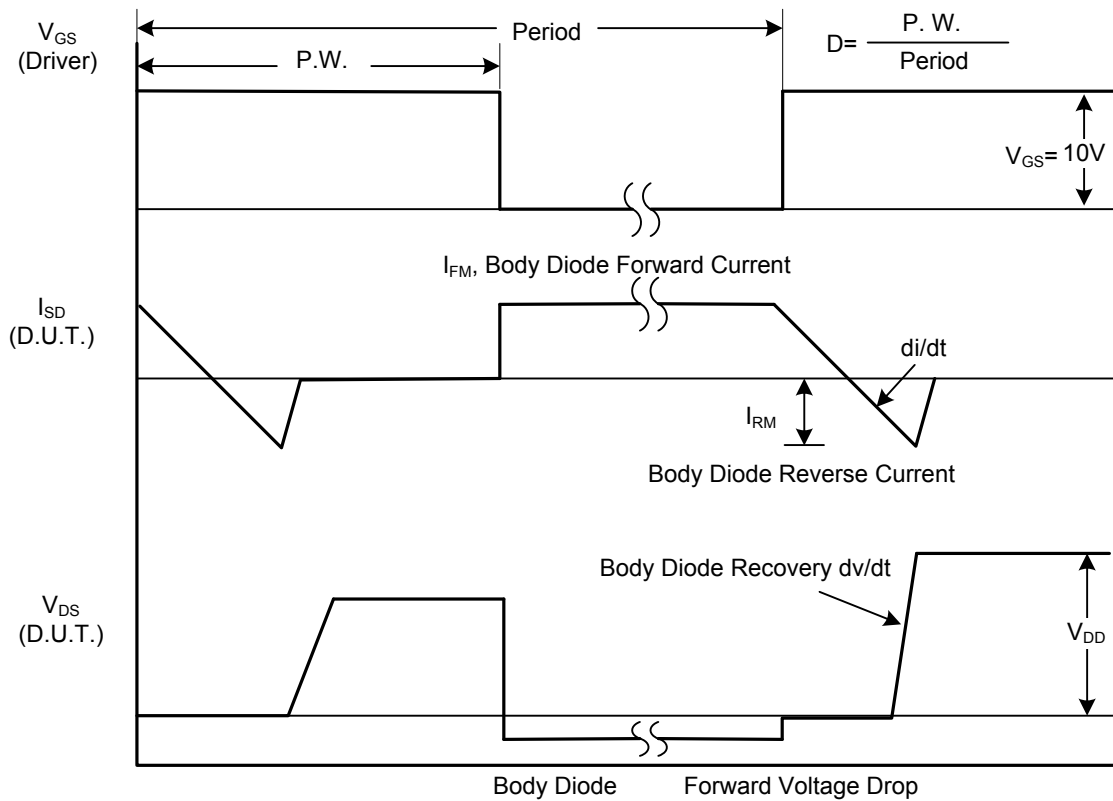
Notes: 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS

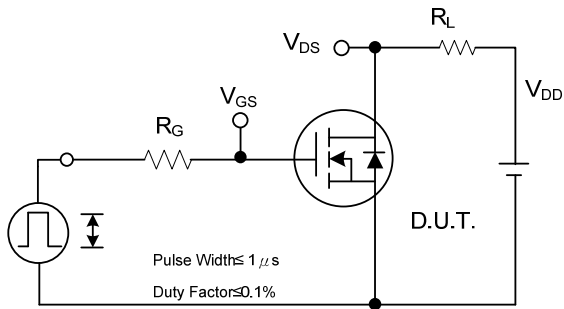


Fig. 2A Switching Test Circuit

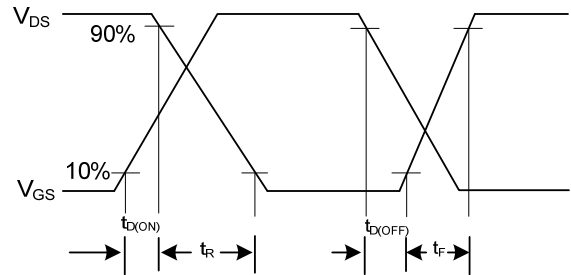


Fig. 2B Switching Waveforms

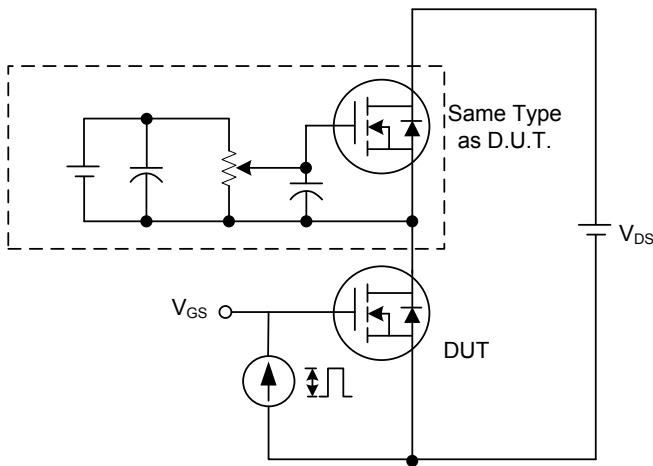


Fig. 3A Gate Charge Test Circuit

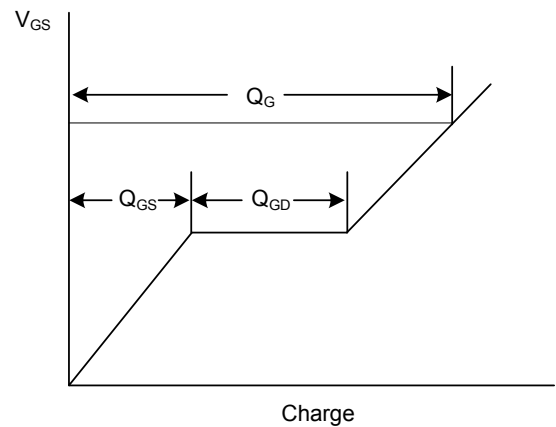


Fig. 3B Gate Charge Waveform

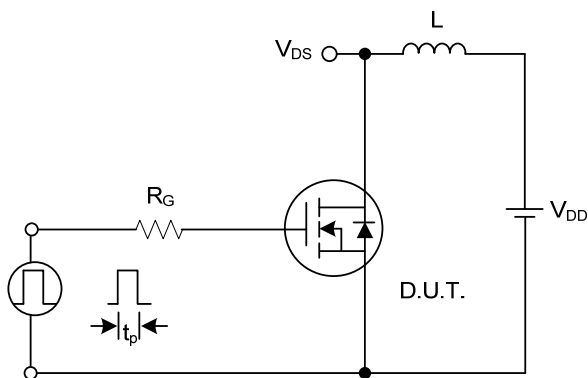


Fig. 4A Unclamped Inductive Switching Test Circuit

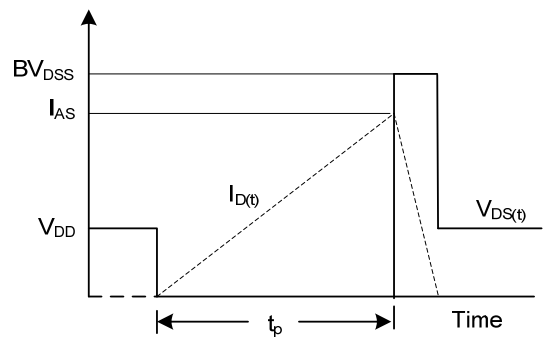
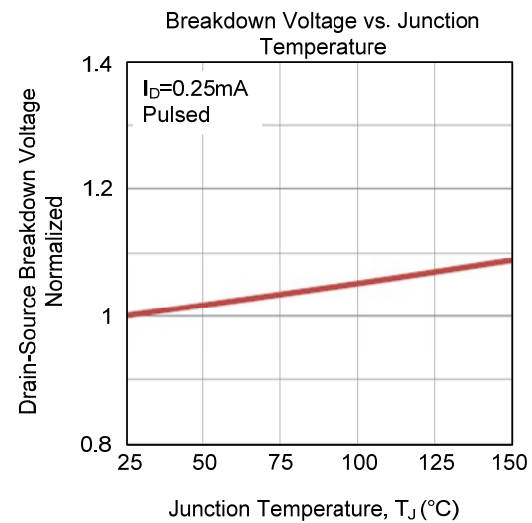
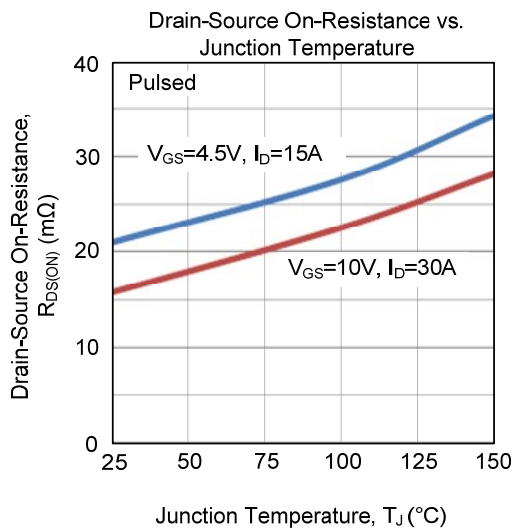
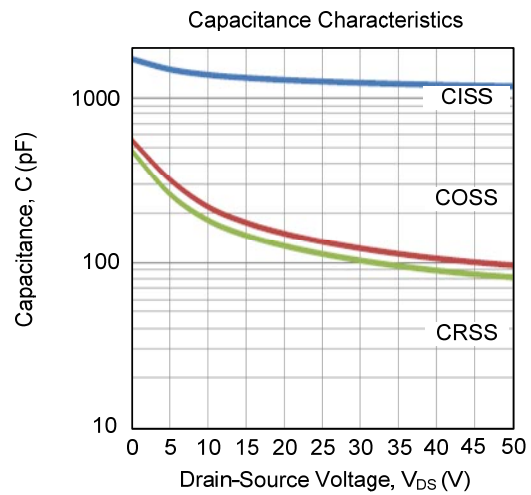
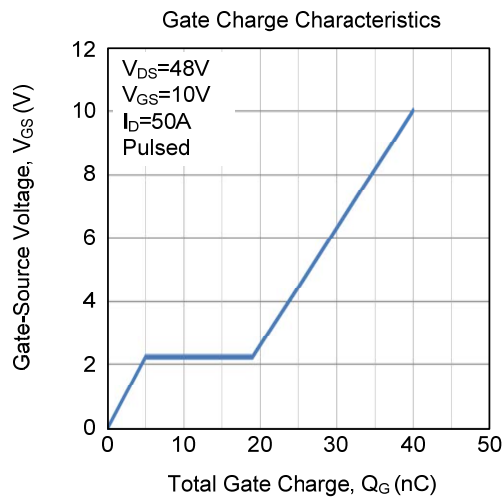
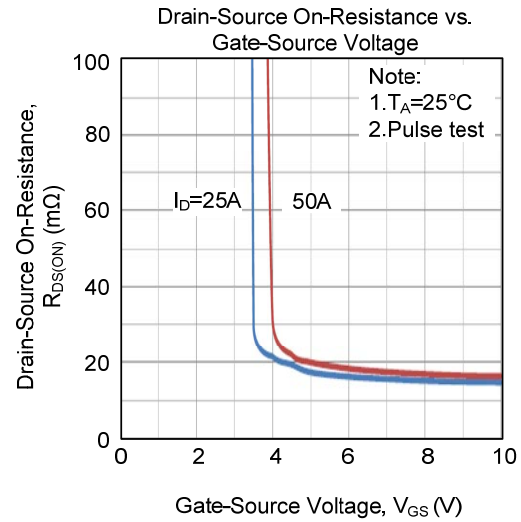
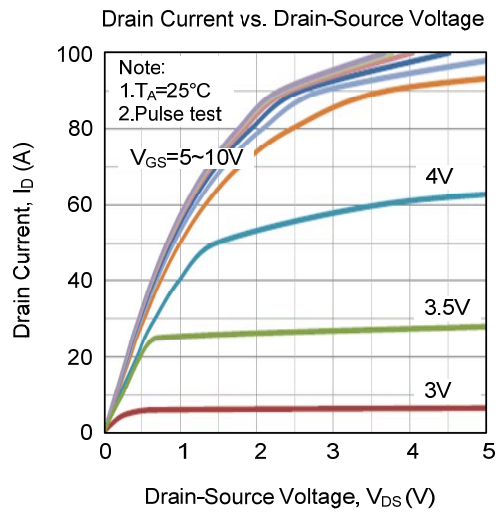
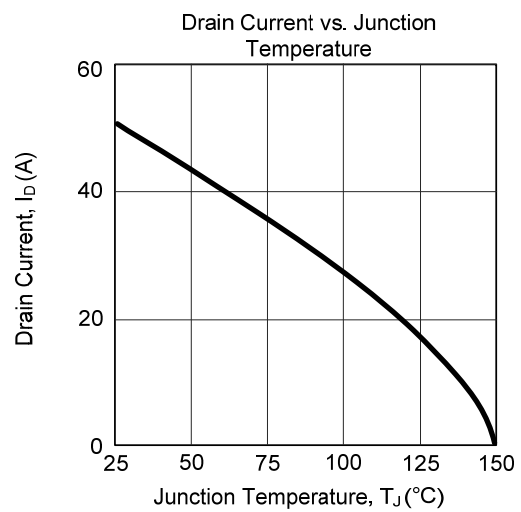
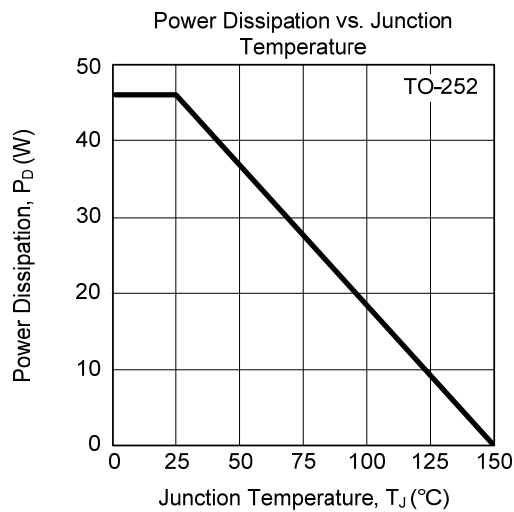
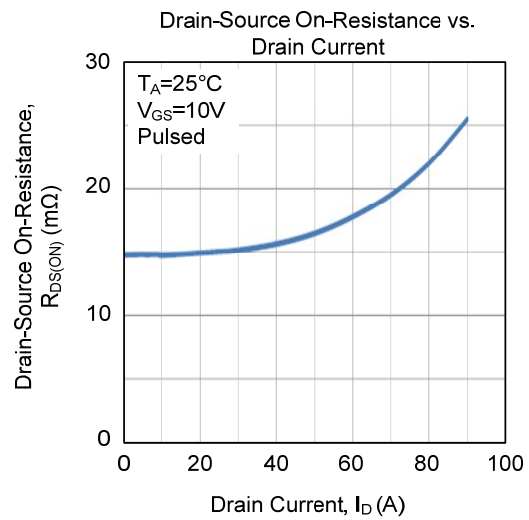
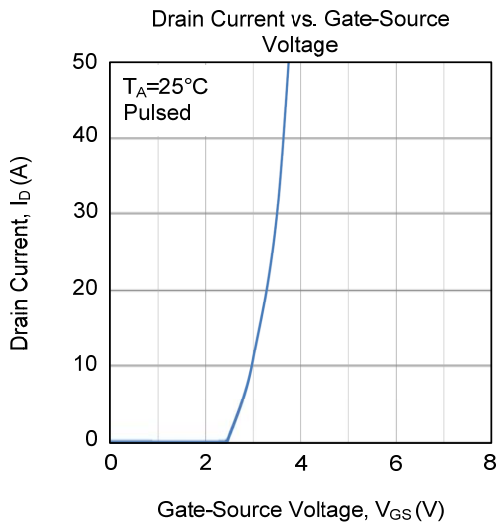
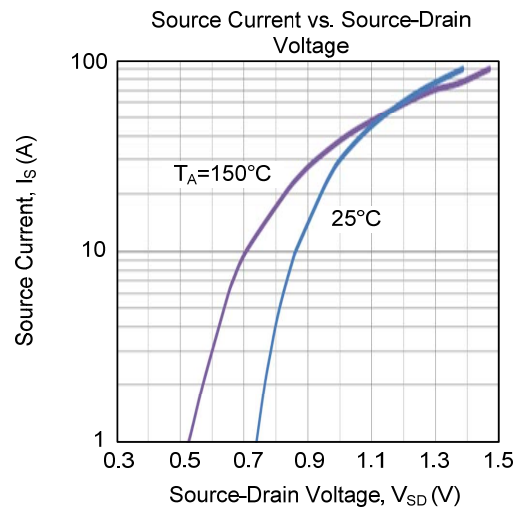
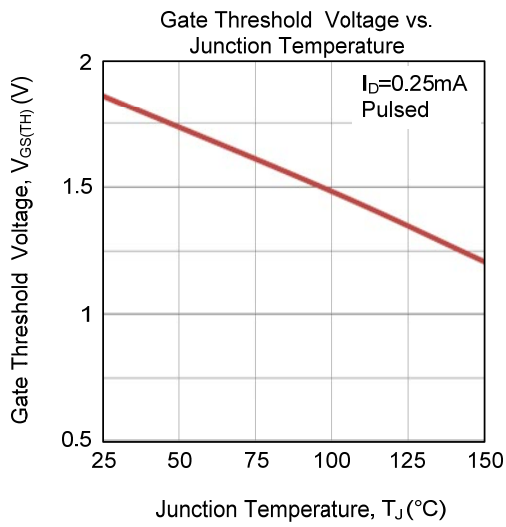


Fig. 4B Unclamped Inductive Switching Waveforms

## TYPICAL CHARACTERISTICS

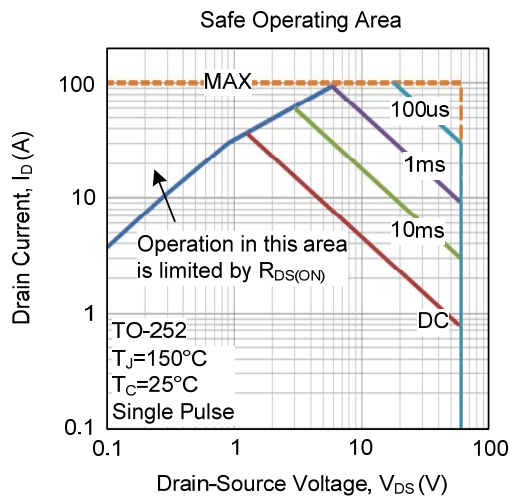


## ■ TYPICAL CHARACTERISTICS (Cont.)





■ TYPICAL CHARACTERISTICS (Cont.)



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