iW-RainboW-G34M/G37M
i.MX 8M Mini or i.MX 8M Nano µQseven System On Module
Hardware User Guide

iWave
Embedding Intelligence

DRAFT VERSION SUBJECT TO CHANGE

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the µQseven SOM based on the NXP's i.MX 8M Mini or i.MX 8M Nano Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8M Mini or i.MX 8M Nano µQseven SOM from a Hardware Systems perspective.

1.2 µQseven SOM Overview

The µQseven is a versatile small form factor computer Module definition, targeting application that require low power, low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE, CAN and LVDS/HDMI display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

NXP's i.MX 8M Mini or i.MX 8M Nano SoC based µQseven System on Module is rich with i.MX 8M Mini or i.MX 8M Nano features along with on SOM LPDDR4, eMMC, Ethernet PHY and comes in compact 40mm x 70mm form factor. The Module PCB has 230 edge fingers that mate with a low profile 230 pin 0.5mm pitch right angle connector.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear to Send
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output

Acronyms	Abbreviations
GPU	Graphics Processing Unit
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
LVDS	Low Voltage Differential Signal
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
OTG	On-The-Go
PCB	Printed Circuit Sheet
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMII	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SOM	System On Module
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface Signal
OD	Open Drain Signal
OC	Open Collector Signal
PCIe	Peripheral Component Interconnect Express Signal
USB	Universal Serial Bus Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- i.MX 8M Mini SoC
  - IMX8MMIEC_Revx.x.pdf
  - IMX_8M_Mini_RM_Revx.x.pdf

- i.MX 8M Nano SoC
  - IMX8MNIEC_Revx.x.pdf
  - IMX_8M_Nano_RM_Revx.x.pdf

1.6 Important Note

In this document, wherever i.MX 8M Mini or i.MX 8M Nano SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET_TXC

  In this signal, ***ENET_TXC*** pad is used for same functionality.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO2_20)

  In this signal, ***BCONFIG_0*** is the GPIO functionality which we are using and ***GPIO2_20*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 8M Mini or i.MX 8M Nano µQseven SOM features and Hardware architecture with high level block diagram.

2.1 i.MX 8M Mini or i.MX 8M Nano µQseven SOM Block Diagram

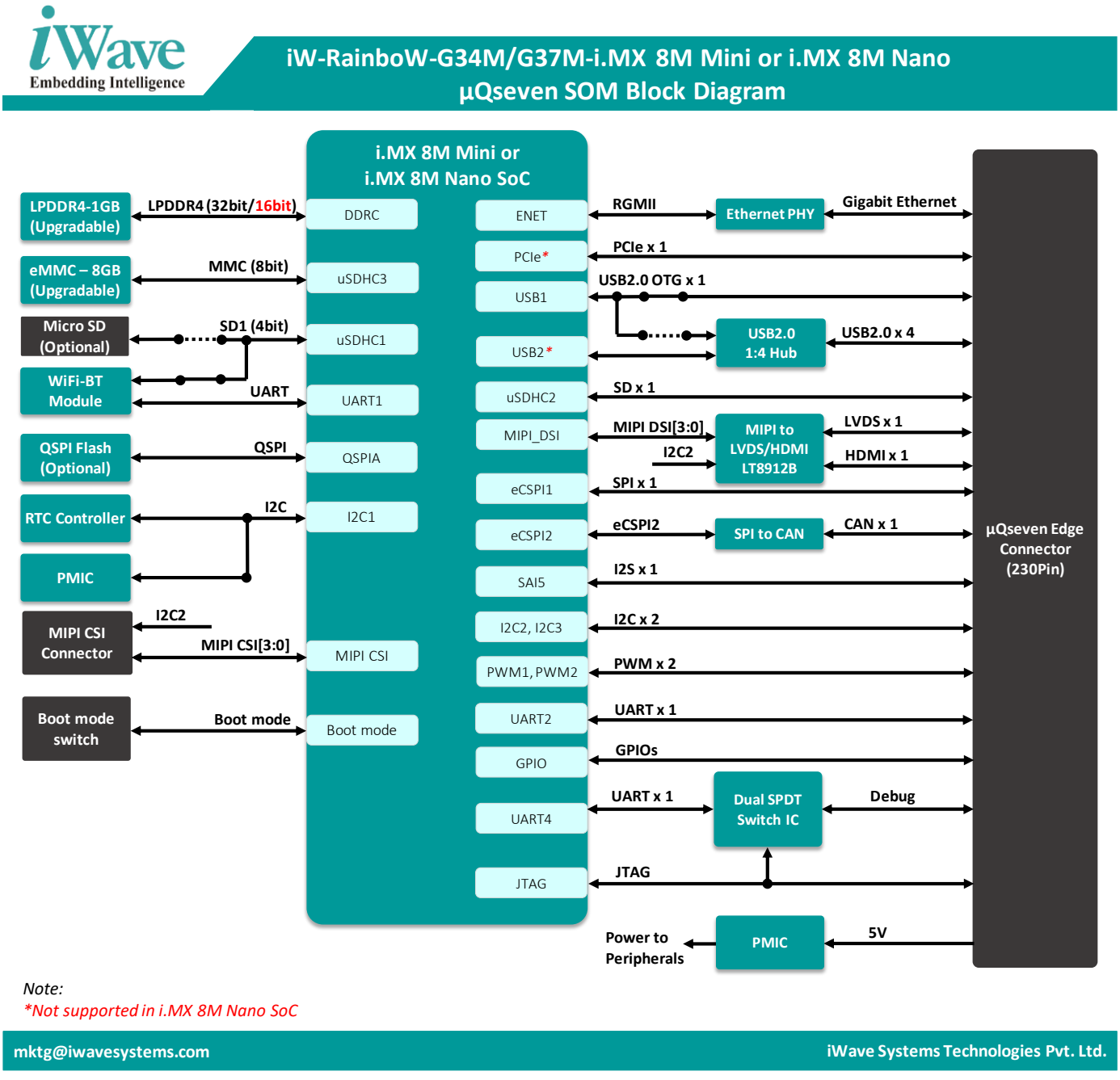

Figure 1: i.MX 8M Mini or i.MX 8M Nano µQseven SOM Block Diagram

2.2 i.MX 8M Mini or i.MX 8M Nano µQseven SOM Features

i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports the following features.

CPU

- i.MX 8M Mini Q/QL/D/DL/S/SLProcessor[1]:
  - i.MX 8M Mini Quad : 4 x Cortex- A53,1 x Cortex-M4
  - i.MX 8M Mini Quad Lite : 4 x Cortex- A53,1 x Cortex-M4(VPU not supported)
  - i.MX 8M Mini Dual : 2 x Cortex- A53,1 x Cortex-M4
  - i.MX 8M Mini Dual Lite : 2 x Cortex- A53,1 x Cortex-M4(VPU not supported)
  - i.MX 8M Mini Solo : 1 x Cortex- A53, 1 x Cortex-M4
  - i.MX 8M Mini Solo Lite : 1 x Cortex- A53,1 x Cortex-M4(VPU not supported)
- i.MX 8M Nano Q/QL/D/DL/S/SL Processor[1]:
  - i.MX 8M Nano Quad : 4 x Cortex- A53, 1 x Cortex-M7
  - i.MX 8M Nano Quad Lite : 4 x Cortex- A53, 1 x Cortex-M7 (GPU not supported)
  - i.MX 8M Nano Dual : 2 x Cortex- A53, 1 x Cortex-M7
  - i.MX 8M Nano Dual Lite : 2 x Cortex- A53, 1 x Cortex-M7 (GPU not supported)
  - i.MX 8M Nano Solo : 1 x Cortex- A53, 1 x Cortex-M7
  - i.MX 8M Nano Solo Lite : 1 x Cortex- A53, 1 x Cortex-M7 (GPU not supported)

Power

- BD71847AMWV-E2 PMIC

Memory

- i.MX 8M Mini SOM
  - LPDDR4 - 1GB (Expandable up to 8GB)[2,3]
- i.MX 8M Nano SOM
  - LPDDR4 - 1GB (Expandable up to 4GB)[2,3]
- eMMC Flash - 8GB (Expandable)[3]
- Micro SD slot (Optional)[4]
- QSPI Flash (Optional)

Other On-SOM Features

- WiFi 802.11a/b/g/n/ac + Bluetooth 5.0 Module[4]
- Gigabit Ethernet PHY Transceiver
- RTC Controller
- MIPI CSI x 1 Channel

µQseven PCB Edge Interfaces

- Gigabit Ethernet x 1 Port
- PCIe x 1 Port[5]
- SD (4bit) x 1 Port
- USB 2.0 OTG x 1 Port[6]
- USB 2.0 Host x 3 Port[6]
- LVDS/HDMI x 1 Port[7]
- CAN x 1 Port
- SAI/I2S (Audio Interface) x 1 Port
- Data UART (with CTS & RTS) x 1 Port
- eCSPI x 1 Port
- I2C x 2 Port
- Debug UART
- PWM x 2 Port
- Power & Management Signals

General Specification

- Power Supply : 5V, 2.5A
- Form Factor : 40mm X 70mm

1. *There are six configurations of i.MX 8M Mini or i.MX 8M Nano SoC supported by NXP, hence in this document i.MX 8M Mini or i.MX 8M Nano Q/QL/D/DL/S/SLis used to represent either of one based on SOM Part Number.*
2. *The i.MX 8M Mini CPU can support up to 8GB RAM but considering the available LPDDR4 Chips, SOM can support up to 4GB (32Gb) RAM.*
3. *Memory Size will differ based on iWave's SOM Product Part Number.*
4. *uSDHC1 is shared between Wi-Fi module and microSD connector, by default it will be connected to Wi-Fi Module. So, on SOM microSD will be an optional feature.*
5. *PCIe is not supported in i.MX 8M Nano SoC.*
6. *Since USB2 is NC in i.MX 8M Nano SoC, USB2.0 lines are supported through a switch.*
7. *At a time either LVDS or HDMI can be supported. By default, LVDS is supported.*

2.3 CPU

iW-RainboW-G34M/G37M i.MX 8M Mini or i.MX 8M Nano µQseven SOM can support different i.MX 8M Mini or i.MX 8M Nano SoCs from NXP.

2.3.1 i.MX 8M Mini CPU

The i.MX 8M Mini Family consists of six processors: i.MX 8M Mini Quad, Quad Lite, Dual, Dual Lite, Solo, Solo Lite.

The Major difference between i.MX 8M Mini SoCs are:

- i.MX 8M Mini Quad : 4 x Cortex- A53, 1 x Cortex-M4
- i.MX 8M Mini Quad Lite : 4 x Cortex- A53, 1 x Cortex-M4(VPU not supported)
- i.MX 8M Mini Dual : 2 x Cortex- A53, 1 x Cortex-M4
- i.MX 8M Mini Dual Lite : 2 x Cortex- A53, 1 x Cortex-M4(VPU not supported)
- i.MX 8M Mini Solo : 1 x Cortex- A53, 1 x Cortex-M4
- i.MX 8M Mini Solo Lite : 1 x Cortex- A53, 1 x Cortex-M4(VPU not supported)

The i.MX 8M Mini Family supports ARM Cortex-A53 Core @ 1.6 GHz, ARM Cortex-M4F Core @ 400 MHz, 1080p, VPU, and dual failover-ready display controllers, 1×1080p display, including MIPI-DSI. Memory interfaces supporting LPDDR4, DDR4, DDR3L, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, RAW NAND and SD, and a wide range of peripheral I/Os such as PCIe 2.0 provide wide flexibility.

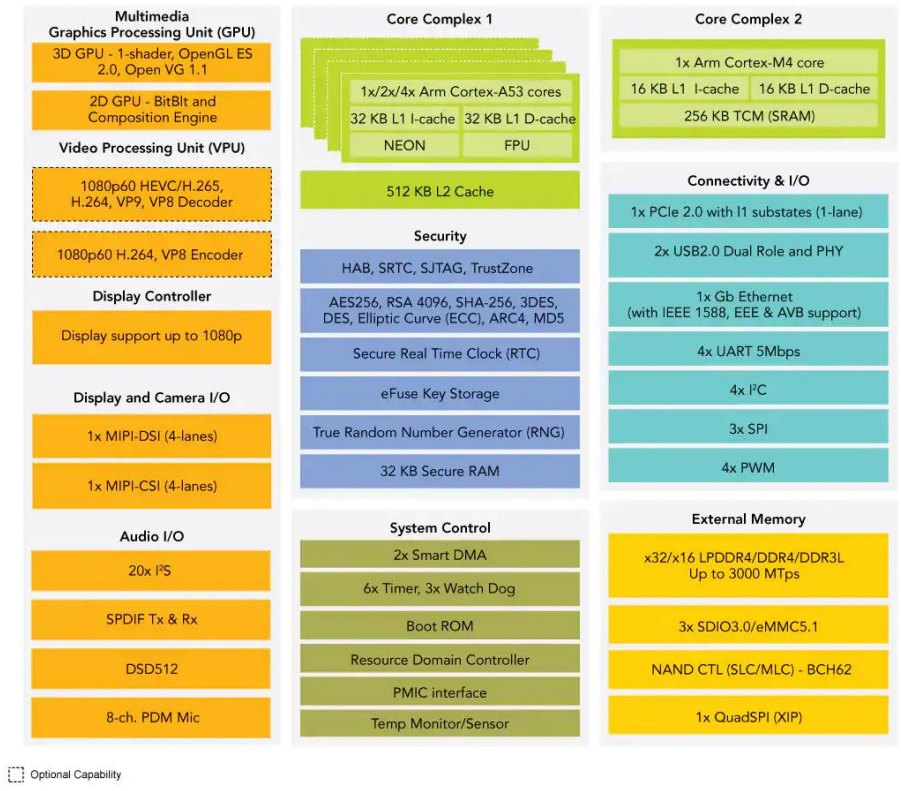

Figure 2: i.MX 8M Mini Block Diagram

2.3.2 i.MX 8M Nano SoC

The i.MX 8M Nano Family consists of six processors: i.MX 8M Nano Quad, Quad Lite, Dual, Dual Lite, Solo, Solo Lite. The Major difference between i.MX 8M Nano SoCs are:

- i.MX 8M Nano Quad : 4 x Cortex- A53, 1 x Cortex-M7
- i.MX 8M Nano Quad Lite : 4 x Cortex- A53, 1 x Cortex-M7 (VPU not supported)
- i.MX 8M Nano Dual : 2 x Cortex- A53, 1 x Cortex-M7
- i.MX 8M Nano Dual Lite : 2 x Cortex- A53, 1 x Cortex-M7 (VPU not supported)
- i.MX 8M Nano Solo : 1 x Cortex- A53, 1 x Cortex-M7
- i.MX 8M Nano Solo Lite : 1 x Cortex- A53, 1 x Cortex-M7 (VPU not supported)

The i.MX 8M Nano Family supports ARM Cortex-A53 Core @ 1.4 GHz, ARM Cortex-M7 Core @ 600 MHz, 1080p, and dual fail over-ready display controllers, 1× 1080p display, including MIPI-DSI. Memory interfaces supporting LPDDR4, DDR4, DDR3L, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, RAW NAND and SD, and a wide range of peripheral I/Os.

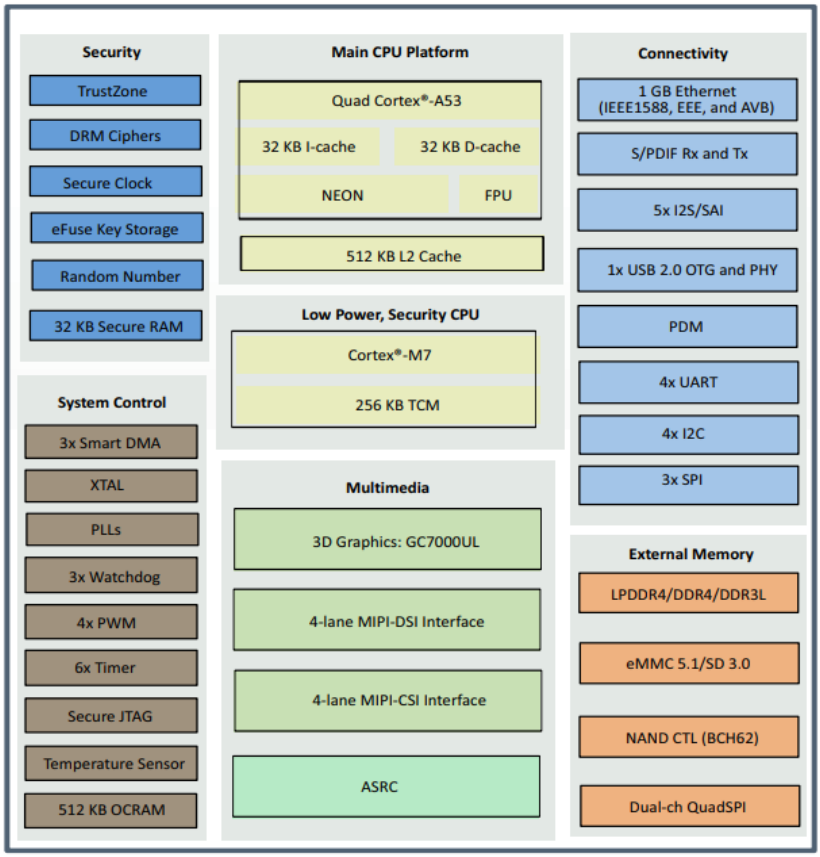

Figure 3: i.MX 8M Nano Block Diagram

Note: The i.MX 8M Mini or i.MX 8M Nano processor offers numerous advanced features, please refer the latest i.MX 8M Mini or i.MX 8M Nano Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PMIC

i.MX 8M Mini or i.MX 8M Nano µQseven SOM uses Rohm's BD71847AMWV on-SOM PMIC for Power management of i.MX 8M Mini or i.MX 8M Nano SOMs. The BD71847AMWV is a Power Management Integrated Circuit (PMIC) designed specifically for powering single-core, dual-core, and quad-core SoC's such as NXP-i.MX 8M Mini.

The BD71847AMWV is a power management integrated circuit (PMIC) features six high efficiency buck converters and six linear regulators (LDOs) for powering the processor, memory and miscellaneous peripherals. Built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through I2C1 after start up offering flexibility for different system states. The BD71847AMWV(U9) comes in 56pin QFN Package and placed on Top side of SOM.

2.5 Memory

2.5.1 LPDDR4 RAM

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports 2GB RAM using 32bit LPDDR4 IC for Mini and 1GB RAM using 16bit LPDDR4 IC for Nano connected to DDR controller of CPU to support LPDDR4 clock up to 1.5 GHz in Mini and up to 1.6GHz in Nano. The LPDDR4 IC (U11) placed on Top side of the SOM. The RAM size can be expandable up to maximum of 8GB in Mini and up to 2GB in Nano. To customize the LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 8M Mini µQseven SOM supports 8GB eMMC as default boot device and storage device. This is connected to eMMC0 version 5.1v controller of the i.MX 8M Mini SoC and operates at 1.8V (I/O supply) and 3.3V(NAND core supply) Voltage levels.

The eMMC flash (U21) memory is physically located on bottom side of the µQseven SOM. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 Micro SD Connector (Optional)

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM optionally supports Micro SD slot which can be used to connect Micro SD card as optional boot device as well as Mass storage device. Micro SD card connector (J2) is directly connected to the USDHC1 controller of the i.MX 8M Mini or i.MX 8M Nano SoC. The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX 8M Mini µQseven SOM supports configurable I/O voltage levels (3.3V/1.8V) for USDHC1 lines through GPIO GPIO1_3. If GPIO1_3 is set to low, then 3.3V IO level is selected for uSDHC1 lines. If GPIO4_3 is set to high, then 1.8V IO level is selected for uSDHC1 lines. The microSD Connector is physically located on Top side of the i.MX 8M Mini or i.MX 8M Nano µQseven SOM as shown below.

Note: In default configuration USDHC1 is used for on board Wi-Fi module. Contact iWave Support team if microSD feature is required.

Figure 4: Micro SD Connector

2.5.4 QSPI Flash (Optional)

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM optionally supports 2MB QSPI Flash and can be used as optional boot device. This is connected to QSPI_A controller of the i.MX 8M Mini SoC and operates at 1.8V Voltage levels. The QSPI flash (U19) is physically located on Bottom side of the µQseven SOM. The QSPI Flash size can be expandable. For customised QSPI Flash support, contact iWave.

2.6 RTC Controller

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports external RTC Controller "PCF85263" On-SOM for Real time clock support. This external RTC Controller IC (U12) is connected to i.MX 8M Mini SoC through I2C1 Interface and operates at 3.3V voltage level. In SOM power off condition, this device will take power from µQseven PCB Edge - Pin No. 193 (VRTC_3V0) coin cell power input and continues to keep the current time.

2.7 Wi-Fi and Bluetooth Interface

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM is integrated with Murata's "LBEE5HY1MW" based Wi-Fi& Bluetooth module. The LBEE5HY1MW module is a very high-performance module based on Cypress CYW43455 combo chipset which supports WiFi IEEE 802.11a/b/g/n/ac + Bluetooth 5.0 BR/EDR/LE standard.

The LBEE5HY1MW module utilizes highly optimized IEEE 802.11 Bluetooth coexistence protocols and supports single stream 1x1 IEEE 802.11a/b/g/n/ac mode providing up to 390Mbps. The LBEE5HY1MWmodule features small form factor when integrating Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive switch, Power Management. The LBEE5HY1MW module need external Antenna but it requires a 32.768 kHz clock for sleep operation.

The LBEE5HY1MW module (U13) provides Secure Digital Input Output (SDIO) for interfacing with the host controller for Wi-Fi and UART interface for Bluetooth. The i.MX 8M Mini or i.MX 8M Nano µQseven SOM uses processor's UART1 interface for Bluetooth and USDHC1 interface for Wi-Fi in default configuration. In i.MX 8M Mini or i.MX 8M Nano µQseven SOM, antenna pin of Wi-Fi & Bluetooth module is connected to J4 Connector.

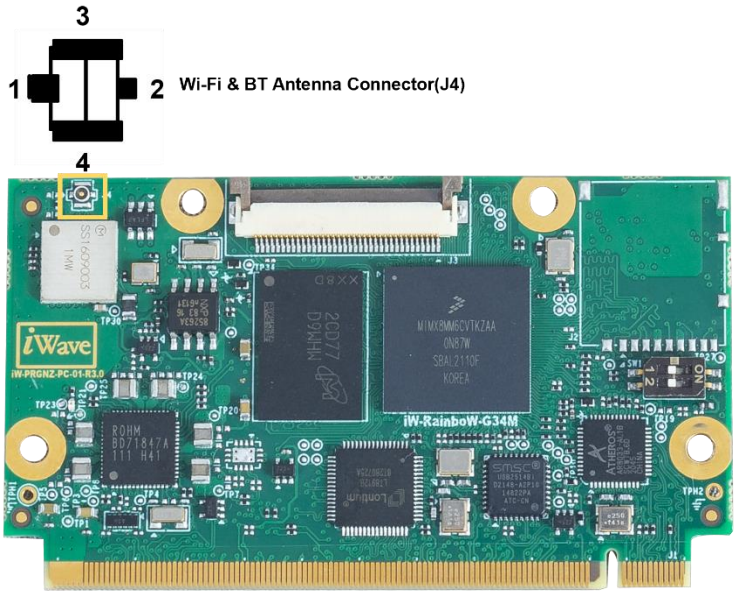

Figure 5: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : MM4829-2702RA4 from Murata Electronics.

Antenna Part Number - : 2042811100 from Molex/FXP830.24.0100B from Taoglas Limited

Note: The LBEE5HY1MW module supports operating temperature -30°C to 85°C with the default module's firmware. To set the module temperature to industrial grade in firmware, please contact iWave.

2.8 MIPI CSI Connector

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports one 4-lane MIPI CSI 2.0 serial camera interface on µQseven PCB Edge connector. The i.MX 8M Mini or i.MX 8M Nano SoC is compliant to D-PHY specification v1.2 and MIPI CSI2 Specification v1.3 except for C-PHY feature. The D-PHY interface Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The D-PHY interface Controller takes care of all packet formatting details and transmission over the MIPI bus.

Note: MIPI CSI Camera in i.MX 8M Mini or i.MX 8M Nano µQseven SOM can be supported through iWave's OV5640 MIPI Camera daughter Board.

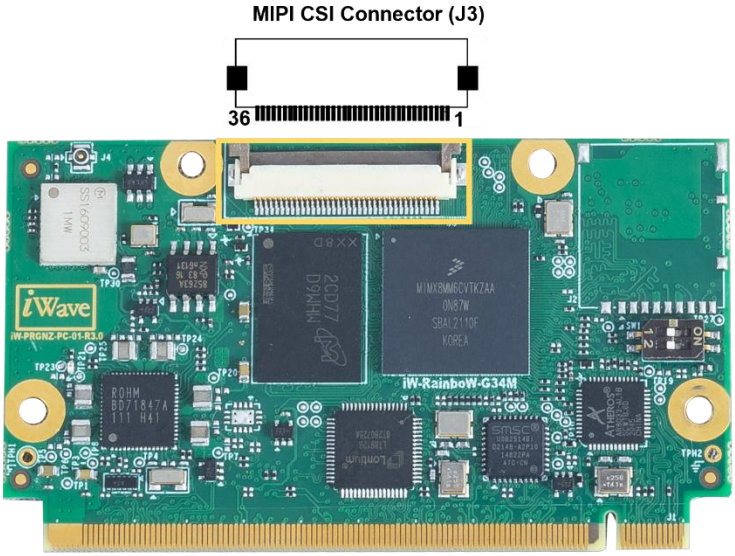

Figure 6: MIPI CSI Connector

Number of Pins - : 36

Connector Part - : FH12A-36S-0.5SH(55)

For more details on MIPI CSI pinouts, refer below table:

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	CAM_PWR	NA	Power	3V3 Camera Power
2	CAM_PWR	NA	Power	3V3 Camera Power
3	MIPI_CSI_DATA0_P	MIPI_CSI_D0_P/ B14	I, MIPI	MIPI CSI differential data lane 0 positive.
4	MIPI_CSI_DATA0_N	MIPI_CSI_D0_N/ A14	I, MIPI	MIPI CSI differential data lane 0 negative.
5	GND	NA	Power	Ground.
6	MIPI_CSI_DATA1_P	MIPI_CSI_D1_P/ B15	I, MIPI	MIPI CSI differential data lane 1 positive.

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
7	MIPI_CSI_DATA1_N	MIPI_CSI_D1_N/ A15	I, MIPI	MIPI CSI differential data lane 1 negative.
8	GND	NA	Power	Ground.
9	MIPI_CSI_DATA2_P	MIPI_CSI_D2_P/ B17	I, MIPI	MIPI CSI differential data lane 2 positive.
10	MIPI_CSI_DATA2_N	MIPI_CSI_D2_N/ A17	I, MIPI	MIPI CSI differential data lane 2 negative.
11	CAM0_RST(GPIO3_06)	NAND_DATA00/ P23	I, 1.8V CMOS/10K PU	MIPI Camera Reset signal
12	MIPI_CSI_DATA3_P	MIPI_CSI_D3_P/ B18	I, MIPI	MIPI CSI differential data lane 3 positive.
13	MIPI_CSI_DATA3_N	MIPI_CSI_D3_N/ A18	I, MIPI	MIPI CSI differential data lane 3 negative.
14	GND	NA	Power	Ground.
15	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P/ B16	I, MIPI	MIPI CSI differential Clock positive.
16	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N/ A16	I, MIPI	MIPI CSI differential Clock negative.
17	GND	NA	Power	Ground.
18	I2C2_SCL_1V8	NA	I, 1.8V OD/ 4.7K PU	I2C Clock for MIPI Camera.
19	I2C2_SDA_1V8	NA	IO, 1.8V OD/ 4.7K PU	I2C Data for MIPI Camera.
20	CAM0_EN(GPIO3_08)	NAND_DATA02/ K23	I, 1.8V CMOS/10K PU	Camera 0 Enable (active low).
21	MCLK (GPIO4_20)	SAI1_MCLK/ AB18	I, 1.8V CMOS	Master Clock. *Note: NC in Nano SoC*
22	NC	NA	-	NC.
23	NC	NA	-	NC.
24	NC	NA	-	NC.
25	GND	NA	Power	Ground.
26	NC	NA	-	NC.
27	NC	NA	-	NC.
28	GND	NA	Power	Ground.
29	NC	NA	-	NC.
30	NC	NA	-	NC.
31	NC	NA	-	NC.
32	NC	NA	-	NC.
33	NC	NA	-	NC.
34	GND	NA	Power	Ground.
35	CAM0_GPIO(GPIO3_07)	NAND_DATA02/ K24	I/O, 1.8V CMOS	GPIO for Camera 0
36	CAM1_GPIO(GPIO4_01)	SAI1_RXC/ AF16	I/O, 1.8V CMOS	Default NC *Note: Connected optionally. NC in Nano SoC*

2.9 Boot Media Setting

i.MX 8M Mini or i.MX 8M Nano SoC boot process begins at Power On Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. i.MX 8M Mini SoC Boot ROM code uses the state of the internal register BOOT_MODE [1:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behaviour of the device.i.MX 8M Mini or i.MX 8M Nano µQseven SOM boot media is fixed as eMMC flash by On-SOM GPIO setting in hardware.

Note: Contact iWave if different boot media support is required other than eMMC flash.

Figure 7: Boot Media Switch

Table 3: Boot Media Switch Settings

Boot Media	SW1(2 Position Switch)	
	POS1	POS2
USB Serial Download	ON	OFF
eMMC	OFF	ON

Table 4: Boot Mode Pin Settings Truth Table

BOOT_MODE [1]	BOOT_MODE [0]	Boot Type	Description
1	0	Internal Boot Mode	In this mode, i.MX 8M Mini or i.MX 8M Nano boots from eMMC.
0	1	Serial Downloader Mode	In this mode, i.MX 8M Mini or i.MX 8M Nano boot media can be Programmed through its USB OTG interface using UUU tool supported by NXP.

Also, i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports BIOS_DISABLE#/BOOT_ALT# functionality as per Qseven specification. By pulling low on this pin puts i.MX 8M Mini or i.MX 8M Nano SoC in serial download mode where the CPU boot media can be programmed through its USB OTG interface.

2.10 µQseven PCB Edge Connector

i.MX 8M Mini or i.MX 8M Nano µQseven SOM Supports 230pin µQseven PCB edge connector for interfaces expansion. The interfaces which are available at µQseven Edge connector are explained in the following sections.

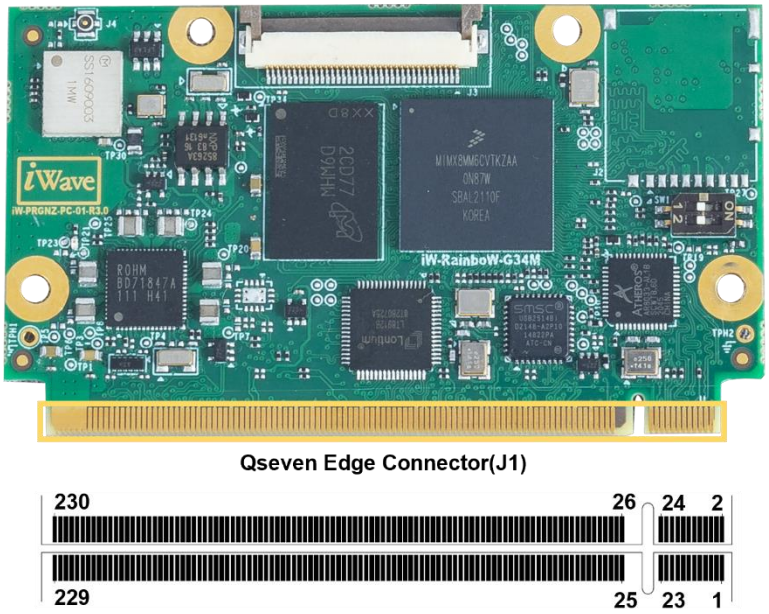

Figure 8: µQseven Edge Connector

Number of Pins - : 230

Connector Part - : Not Applicable (On Board PCB Edge connector)

Mating Connector - : 88882-2Dxx from Aces

BEC5230S9xFREDC from Yamaichi

AS0B32x-S78N-xF from FOXCONN

IMSA-18010S-230A-GN1 from IRISO

Table 5: µQseven Edge Connector Pinouts

Signal	µQseven Pin (Bottom)	µQseven Pin (Top)	Signal
GND	1	2	GND
GPHY_DTXRXM	3	4	GPHY_CTXRXM
GPHY_DTXRXP	5	6	GPHY_CTXRXP
GPHY_LINK10_100_LED	7	8	GPHY_LINK_1000_LED
GPHY_BTXRXM	9	10	GPHY_ATXRXM
GPHY_BTXRXP	11	12	GPHY_ATXRXP
GPHY_LINK_LED	13	14	GPHY_ACT_LED1
VDVDH_GPHY1	15	16	SUS_S5_Q7
NC	17	18	SUS_S3_Q7

Signal	µQseven Pin (Bottom)	µQseven Pin (Top)	Signal
SUS_STAT_Q7	19	20	PWRBTN#
GPII_1	21	22	GPII_0
GND	23	24	GND
Key			
GND	25	26	PWRGIN
GPII_2	27	28	RSTBN
NC	29	30	NC
NC	31	32	NC
NC	33	34	GND
NC	35	36	NC
NC	37	38	NC
GND	39	40	GND
BIOS_DISABLE#/BOOT_ALT#	41	42	SD2_CLK
SD2_CD	43	44	SD1_LED
SD2_CMD	45	46	GPIO_SD2_WP(GPIO5_26)
GPIO_SD1_PWR(GPIO1_01)	47	48	SD2_DATA1
SD2_DATA0	49	50	SD2_DATA3
SD2_DATA2	51	52	NC
NC	53	54	NC
NC	55	56	USB1_OTG_PWR(GPIO1_12)
GND	57	58	GND
SAI5_TX_SYNC(SAI5_RXD1	59	60	I2C3_SCL
SSI_RST	61	62	I2C3_SDA
SAI5_TX_BCLK(SAI5_RXD2)	63	64	SMB_ALERT_B(GPIO1_15)
SAI5_RX_DATA0(SAI5_RXD0)	65	66	I2C2_SCL
SAI5_TX_DATA0(SAI5_RXD3)	67	68	I2C2_SDA
THRM#	69	70	Q7_WDTRIG_B
GPIO_THRMTRIP_Q7(GPIO1_14)	71	72	Q7_WDOG_B
GND	73	74	GND
NC	75	76	NC
NC	77	78	NC
NC	79	80	USB_4_OC
NC	81	82	USB_HUB4OUT_DM
NC	83	84	USB_HUB4OUT_DP
USB_HUB3_OC/USB_HUB2_OC	85	86	USB_0_1_OC
USB_HUB3OUT_DM	87	88	USB_HUB2OUT_DM
USB_HUB3OUT_DP	89	90	USB_HUB2OUT_DP
USB_OTG1_VBUS	91	92	USB_ID
USB1_DN	93	94	USB_HUB1OUT_DM
USB1_DP	95	96	USB_HUB1POT_DP
GND	97	98	GND

Signal	µQseven Pin (Bottom)	µQseven Pin (Top)	Signal
LVDS_CH0_P	99	100	NC
LVDS_CH0_N	101	102	NC
LVDS_CH1_P	103	104	NC
LVDS_CH1_N	105	106	NC
LVDS_CH2_P	107	108	NC
LVDS_CH2_N	109	110	NC
GPIO_LVDS_PPEN(GPIO5_04)	111	112	GPIO_LVDS_BLEN(GPIO5_05)
LVDS_CH3_P	113	114	NC
LVDS_CH3_N	115	116	NC
GND	117	118	GND
LVDS_CLK_P	119	120	NC
LVDS_CLK_N	121	122	NC
GPIO_LVDS_BLT_CTRL(GPIO5_03)	123	124	GP_1_WB
I2C2_SDA	125	126	NC
I2C2_SCL	127	128	NC
CAN0_TX	129	130	CAN0_RX
HDMI_CLKP	131	132	NC
HDMI_CLKM	133	134	NC
GND	135	136	GND
HDMI_D1P	137	138	NC
HDMI_D1M	139	140	NC
GND	141	142	GND
HDMI_D0P	143	144	NC
HDMI_D0M	145	146	NC
GND	147	148	GND
HDMI_D2P	149	150	I2C3_SDA
HDMI_D2M	151	152	I2C3_SCL
HDMI_HPD	153	154	NC
PCIE_REFCLK_DP*	155	156	PCIe_WAKE_B(GPIO1_10)
PCIE_REFCLK_DN*	157	158	PCIe_RST(GPIO1_11)
GND	159	160	GND
NC	161	162	NC
NC	163	164	NC
GND	165	166	GND
NC	167	168	NC
NC	169	170	NC
UART2_TX(SAI3_TXC)	171	172	UART2_CTS_B(SAI3_RXC)
NC	173	174	NC
NC	175	176	NC
UART2_RX(SAI3_TXFS)	177	178	UART2_RTS_B(SAI3_RXD)
PCIE_TXP*	179	180	PCIe_RXP*

Signal	µQseven Pin (Bottom)	µQseven Pin (Top)	Signal
PCIE_TXN*	181	182	PCIe_RXM*
GND	183	184	GND
Q7_GPIO0(GPIO5_22)	185	186	Q7_GPIO1(GPIO1_05)
Q7_GPIO2(GPIO5_23)	187	188	Q7_GPIO3(GPIO1_06)
Q7_GPIO4(GPIO5_24)	189	190	Q7_GPIO5(GPIO1_07)
Q7_GPIO6(GPIO5_25)	191	192	Q7_GPIO7(GPIO1_08)
VRTC_3V0	193	194	PWM1_OUT(I2C4_SDA)
NC	195	196	PWM2_OUT(I2C4_SCL)
GND	197	198	GND
ECSPI1_MOSI	199	200	ECSPI1_SS0
ECSPI1_MISO	201	202	GPIO_ECSPI1_SS1
ECSPI1_SCLK	203	204	JTAG_TRST_B(BOOT_MODE2) *Note: NC*
NC	205	206	NC
JTAG_TCK	207	208	JTDI_URX
JTDO_UTX	209	210	JTAG_TMS
NC	211	212	NC
NC	213	214	NC
NC	215	216	NC
NC	217	218	NC
VCC_5V	219	220	VCC_5V
VCC_5V	221	222	VCC_5V
VCC_5V	223	224	VCC_5V
VCC_5V	225	226	VCC_5V
VCC_5V	227	228	VCC_5V
VCC_5V	229	230	VCC_5V

** Not supported in i.MX 8M Nano SoC.*

2.10.1 Gigabit Ethernet

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports Gigabit Ethernet capable ports GBE on µQseven PCB Edge connector.

Gigabit Ethernet (GBE) port of µQseven PCB Edge connector is supported through i.MX 8M Mini or i.MX 8M Nano SoC's ENET controller. The MAC is integrated in the i.MX 8M Mini SoC ENET and connected to the external Gigabit Ethernet PHY "AR8031" from Atheros/Qualcomm on SOM through RGMII interface. The AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements. Since MAC and PHY are supported on SOM itself, only Magnetics are required on the carrier board. i.MX 8M Mini or i.MX 8M Nano µQseven SOM also supports Link and Activity indication LED control signals for GBE0 port to µQseven PCB Edge connector.

For more details on GBE pinouts on µQseven PCB Edge connector, refer below Table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
10	GPHY_ATXRXM	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 negative.
12	GPHY_ATXRXP	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 positive.
9	GPHY_BTXRXM	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 negative.
11	GPHY_BTXRXP	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 positive.
4	GPHY_CTXRXM	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 negative.
6	GPHY_CTXRXP	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 positive.
3	GPHY_DTXRXM	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 negative.
5	GPHY_DTXRXP	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 positive.
15	VDVDH_GPHY1	NA	Power	Power Inductor pin of Gigabit Ethernet
13	GPHY_LINK_LED	NA	O, 3.3V CMOS	Gigabit Ethernet link status LED.
8	GPHY_LINK_1000_LED	NA	O, 3.3V CMOS	Gigabit Ethernet link status LED.
14	GPHY_ACT_LED	NA	O, 3.3V CMOS	Gigabit Ethernet activity status.

2.10.2 PCIe Interface

The i.MX 8M Mini SoC supports single Lane PCI Express-2.0 channels. In i.MX 8M Mini µQseven SOM PCIe Lane is directly connected to µQseven Edge connector by default. CPU internal PCIe REFLCK is connected to µQseven PCB Edge for PCIe reference clock. Also, PCIe wake is supported on µQseven PCB Edge connector from i.MX 8M Mini SoC IO GPIO1_10.

Note: PCIe differential transmitter lines are ac coupled on SOM itself.

For more details on PCIe pinouts on µQseven PCB Edge connector, refer below table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
155	PCIE_REFCLK_DP	NA	O, PCIe	PCIe Clock Positive. *Note: This signal is coming from CPU.*
157	PCIE_REFCLK_DM	NA	O, PCIe	PCIe Clock Negative. *Note: This signal is coming from CPU*
180	PCIE_RXP	PCIE_RXN_P/B19	I, PCIe	PCIe Receive Positive.
182	PCIE_RXN	PCIE_RXN_N/A19	I, PCIe	PCIe Receive Negative.
179	PCIE_TXP	PCIE_TXN_P/B20	O, PCIe / 0.1uF AC Couple	PCIe Transmit Positive.
181	PCIE_TXN	PCIE_TXN_N/A20	O, PCIe / 0.1uF AC Couple	PCIe Transmit Negative.
156	PCIE_WAKE_B(GPIO1_10)	GPIO1_IO10/AD10	I, 3.3V CMOS	PCIe Wake.
158	PCIe_RST(GPIO1_11)	GPIO1_IO11/AC10	O, 3.3V CMOS	PCIe Reset.

Note: PCIe is not supported in i.MX 8M Nano SoC.

2.10.3 SD Interface

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports 4bit SD interface over µQseven PCB Edge connector which can be used to connect SD card as Mass storage or optional boot device. uSDHC2 controller of the i.MX 8M Mini or i.MX 8M Nano SoC is used to support µQseven SD interface. It supports 1-bit or 4-bit transfer mode for SD/SDIO and works up to UHS-I mode @ up to 208 MHz. The I/O voltage level of USDHC2 lines is set to 3.3V.

For more details on SD pinouts on µQseven PCB Edge connector, refer below Table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
45	SD2_CMD	SD2_CMD/W24	IO, 3.3V CMOS/10K PU	SD command.
43	SD2_CD_B	SD2_CD_B/AA26	I, 3.3V/CMOS	SD Card Detect.
42	SD2_CLK	SD2_CLK/W23	O, 3.3V/CMOS	SD Clock.
49	SD2_DATA0	SD2_DATA0/AB23	IO, 3.3V CMOS/10K PU	SD data 0.
48	SD2_DATA1	SD2_DATA1/AB24	IO, 3.3V CMOS/10K PU	SD data 1.
51	SD2_DATA2	SD2_DATA2/V24	IO, 3.3V CMOS/10K PU	SD data 2.
50	SD2_DATA3	SD2_DATA3/V23	IO, 3.3V CMOS/10K PU	SD data 3.
46	GPIO_SD2_WP(GPIO5_26)	UART3_RXD/E18	IO, 3.3V CMOS	SD Write Protect
47	GPIO_SD1_PWR(GPIO1_01)	GPIO1_IO01/AF14	I, 3.3V CMOS	Power Enable.

2.10.4 USB Interface

The i.MX 8M Mini SoC supports two USB2.0, whereas i.MX 8M Nano supports single USB2.0. In i.MX 8M Nano SOM, USB OTG will be supported only in Flash mode. In Boot mode only USB Host is supported.

Note: Since USB2 is NC in i.MX 8M Nano SoC, USB2.0 lines are optionally supported through a switch.

For more details on USB1 2.0 OTG pinouts near µQseven edge connector, refer below table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
95	USB1_DP	USB1_DP/ B22	IO, USB	USB Port1 Data Positive.
93	USB1_DN	USB1_DN/ A22	IO, USB	USB Port1 Data Negative.
56	USB1_OTG_PWR(GPIO1_12)	GPIO1_IO12/ AB10	IO, 3.3V CMOS	USB Port1 Power Enable
91	USB_OTG1_VBUS	USB1_VBUS/ F22	I, 5V Power	USB1 host power detection, when this port is used as a device.
92	USB_ID	USB1_ID/ D22	I, 3.3V CMOS/PU 10K	USB1 OTG ID.

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
86	USB1_OTG_OC(GPIO1_13)	GPIO1_IO13/ AD9	I, 3.3V CMOS	USB Port1 Over Current Indicator.

For more details on USB2 2.0 pinouts near µQseven edge connector, refer below table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
82	USB_HUB4OUT_DM	NA	IO, DIFF	USB Host port 4 data negative.
84	USB_HUB4OUT_DP	NA	IO, DIFF	USB Host port 4 data positive.
80	USB_4_OC	NA	I, 3.3V CMOS/PU 10K	Over current sense for USB port 4
85	USB_HUB3_OC/USB_HUB2_OC	NA	I, 3.3V CMOS/PU 10K	Over current sense for USB port 2 & 3.
86	USB_0_1_OC	NA	I, 3.3V CMOS/ 10K PU	Over current sense for USB port 0 & 1.
87	USB_HUB3OUT_DM	NA	IO, DIFF	USB Host port 3 data negative.
88	USB_HUB2OUT_DM	NA	IO, DIFF	USB Host port 2 data negative.
89	USB_HUB3OUT_DP	NA	IO, DIFF	USB Host port 3 data positive.
90	USB_HUB2OUT_DP	NA	IO, DIFF	USB Host port 2 data positive.
94	USB_HUB1OUT_DM	NA	IO, DIFF	USB Host Port 1 data negative.
96	USB_HUB1OUT_DP	NA	IO, DIFF	USB Host Port 1 data positive.

2.10.5 LVDS/HDMI Display Interface

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports either LVDS or HDMI display on µQseven PCB Edge connector. The LVDS/HDMI signals are connected to µQseven PCB Edge connector through an On-SOM MIPI DSI to LVDS/HDMI Bridge. The MIPI_DSI to LVDS and HDMI Bridge (LT8912B) features a single-channel MIPI® D-PHY receiver with 4 data lanes per channel operating at 1.5Gbps per data lane and a maximum input bandwidth of 6Gbps.

For more details on DSI pinouts on µQseven PCB Edge connector, refer below table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
99	LVDS_CH0_P	NA	IO, DIFF	LVDS channel differential pair 0 positive.
101	LVDS_CH0_N	NA	IO, DIFF	LVDS channel differential pair 0 negative.
103	LVDS_CH1_P	NA	IO, DIFF	LVDS channel differential pair 1 positive.
105	LVDS_CH1_N	NA	IO, DIFF	LVDS channel differential pair 1 negative.
107	LVDS_CH2_P	NA	IO, DIFF	LVDS channel differential pair2 positive.
109	LVDS_CH2_N	NA	IO, DIFF	LVDS channel differential pair 2 negative.
113	LVDS_CH3_P	NA	IO, DIFF	LVDS channel differential pair 3 positive.
115	LVDS_CH3_N	NA	IO, DIFF	LVDS channel differential pair 3 negative.
119	LVDS_CLK_P	NA	IO, DIFF	LVDS channel differential clock positive.

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
121	LVDS_CLK_N	NA	IO, DIFF	LVDS channel differential clock negative.
131	HDMI_CLKP	NA	O, TMDS	HDMI differential clock positive.
133	HDMI_CLKM	NA	O, TMDS	HDMI differential clock negative.
137	HDMI_D1P	NA	O, TMDS	HDMI differential data lane 1 positive.
139	HDMI_D1M	NA	O, TMDS	HDMI differential data lane 1 negative.
143	HDMI_D0P	NA	O, TMDS	HDMI differential data lane 0 positive.
145	HDMI_D0M	NA	O, TMDS	HDMI differential data lane 0 negative.
149	HDMI_D2P	NA	O, TMDS	HDMI differential data lane 2 positive.
151	HDMI_D2M	NA	O, TMDS	HDMI differential data lane 2 negative.
153	HDMI_HPD	NA	I, 1.8V CMOS	HDMI Hot plug detect.

2.10.6 Audio Interface

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports one I2S interface on µQseven Edge connector from CPU's SAI5 channel. In i.MX 8M Mini or i.MX 8M Nano µQseven SOM SAI5 channel is directly connected to µQseven Edge connector by default. The SAI peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, AC97 and other audio CODEC/DSP interfaces. The SAI general features are including Transmitter section with independent bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits and supports graceful restart after FIFO error.

In i.MX 8M Mini or i.MX 8M Nano µQseven SOM the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For more details on Audio Interface pinouts on µQseven PCB Edge connector, refer below table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
59	SAI5_TX_SYNC(SAI5_RXD1)	SAI5_RXD1/AC14	O, 3.3V CMOS	SAI5 Transmitter Frame Sync.
67	SAI5_TX_DATA0(SAI5_RXD3)	SAI5_RXD3/AC13	O, 3.3V CMOS	SAI5 Transmit Data Lane 0.
65	SAI5_RX_DATA0(SAI5_RXD0)	SAI5_RXD0/AD18	I, 3.3V CMOS	SAI5 Receive Data Lane 0.
63	SAI5_TX_BCLK(SAI5_RXD2)	SAI5_RXD2/AD13	O, 3.3V CMOS/ 33E Series	SAI5 Transmitter Bit Clock.

2.10.7 UART Interface

In i.MX 8M Mini or i.MX 8M Nano SoC, UART1 & UART2 are with CTS and RTS support and UART4 is without CTS and RTS support. The i.MX 8M Mini or i.MX 8M Nano SOM's UART2, UART4 are connected to µQseven Edge Connector, whereas UART1 is connected to on SOM Bluetooth module by default. UART2 can be used for any data communication. UART4 of the CPU is connected to µQseven Edge connector and used as Debug UART.

For more details on UART pinouts on µQseven PCB Edge connector, refer below table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
171	UART2_TX(SAI3_TXC)	SAI3_TXC/AG6	O, 3.3V CMOS	UART2 Transmitter.
177	UART2_RX(SAI3_TXFS)	SAI3_TXFS/AC6	I, 3.3V CMOS	UART2 Receiver.
178	UART2_RTS_B(SAI3_RXD)	SAI3_RXD/AF7	I, 3.3V CMOS	UART2 Request to Send.
172	UART2_CTS_B(SAI3_RXC)	SAI3_RXC/AG7	O, 3.3V CMOS	UART2 Clear to Send.
209	UART4_TXD	UART4_TXD/F18	O, 3.3V CMOS	Debug UART Transmitter.
208	UART4_RXD	UART4_RXD/F19	I, 3.3V CMOS	Debug UART Receiver.

2.10.8 SPI Interface

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports 1 Enhanced Configurable SPI interface ECSPI1 on µQseven PCB Edge connector. The i.MX 8M Mini SoC's Enhanced Configurable Serial Peripheral Interface (ECSPI) module is full-duplex, synchronous switch data rate up to 52 Mbit/s, four-wire serial communication block and Master/Slave configurable with maximum clock speed of 20MHz.

For more details on ECSPI1 pinouts on µQseven PCB Edge connector, refer below table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
200	ECSPI1_SS0	ECSPI1_SS0/B6	O, 3.3V CMOS	SPI1 Chip Select 0
203	ECSPI1_SCLK	ECSPI1_SCLK/D6	O, 3.3V CMOS/ 33E Series	SPI1 Clock
201	ECSPI1_MISO	ECSPI1_MISO/A7	I, 3.3V CMOS	SPI1 Master In Slave Out
199	ECSPI1_MOSI	ECSPI1_MOSI/B7	O, 3.3V CMOS	SPI1 Master Out Slave In

2.10.9 CAN Interface

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports one CAN interface on µQseven Edge connector via SPI to CAN Controller.

For more details on CAN0 pinouts on µQseven PCB Edge connector, refer below table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
129	CAN0_TX	NA	O, 3.3V CMOS	Transmit output for CAN bus.
130	CAN0_RX	NA	I, 3.3V CMOS	Receive output for CAN bus.

2.10.10 I2C Interface

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports two I2C interface on µQseven PCB Edge connector. i.MX 8M Mini SoC's I2C2 & I2C3 interfaces are connected to µQseven PCB Edge connector for I2C whereas i.MX 8M Mini SoC's I2C1 interface is connected to On-SOM PMIC and RTC Controller.

For more details on I2C Interface pinouts on µQseven PCB edge connector, refer the below table.

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
60	I2C3_SCL	I2C3_SCL /E10	O, 3.3V OD/ 4.7K PU	I2C3 Serial Clock for General Purpose. *Note: Same signal is also connected to Qseven edge connector 152th pin.*
62	I2C3_SDA	I2C3_SDA / F10	IO, 3.3V OD/ 4.7K PU	I2C3 Serial Data for General Purpose. *Note: Same signal is also connected to Qseven edge connector 150th pin.*
66	I2C2_SCL	I2C2_SCL/D10	O, 3.3V OD/ 4.7K PU	I2C2 Serial Clock for General Purpose *Note: Same signal is also connected to Qseven edge connector 127th pin through a resistor.*
68	I2C2_SDA	I2C2_SDA/D9	IO, 3.3V OD/ 4.7K PU	I2C2 Serial Data for General Purpose. *Note: Same signal is also connected to Qseven edge connector 125th pin through a resistor.*

2.10.11 JTAG Interface

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports JTAG interface for CPU debug purpose optionally. The System JTAG Controller (SJC) provides debug and test control with the maximum security. The test access port (TAP) is designed to support features compatible with the IEEE Standard 1149.1 v2001 (JTAG).

For more details on JTAG pinouts on µQseven PCB Edge connector, refer below table:

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
204	NC	JTAG_TRST_B/C27	I, 3.3V CMOS/ 10K PU	JTAG test reset signal. *Note: By default, do not connect to JTAG_TRST_B*
208	JTAG_TDI	JTAG_TDI/E27	I, 3.3V CMOS/ 10K PU	JTAG test data input. *Note: Connected optionally. By default, UART4 is used.*
210	JTAG_TMS	JTAG_TMS/F27	I, 3.3V CMOS/ 10K PU	JTAG test mode select.
207	JTAG_TCK	JTAG_TCK/F26	I, 3.3V CMOS/ 10K PD	JTAG test Clock.
209	JTAG_TDO	JTAG_TDO/E26	O, 3.3V CMOS/ 10K PU	JTAG test data output. *Note: Connected optionally. By default, UART4 is used.*

2.10.12 GPIO Interface

The i.MX 8M Mini or i.MX 8M Nano SOM supports GPIOs on µQseven PCB Edge connector in i.MX 8M Mini µQseven Development platform's default configuration. Most of the i.MX 8M Mini SoC Pins which are connected to µQseven Edge connector can be configured as GPIO with interrupt capable (if not used as other interface) The i.MX 8M Mini or i.MX 8M Nano SoC's GPIO (general-purpose input/output) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts.

For more details on GPIO Interface pinouts on µQseven PCB edge connector, refer the below table.

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
185	Q7_GPIO0(GPIO5_22)	UART1_RXD/E14	IO, 3.3V CMOS	General purpose input/output 0.
186	Q7_GPIO1(GPIO1_05)	GPIO1_IO05/AF12	IO, 3.3V CMOS	General purpose input/output 1.
187	Q7_GPIO2(GPIO5_23)	UART1_TXD/F13	IO, 3.3V CMOS	General purpose input/output 2.
188	Q7_GPIO3(GPIO1_06)	GPIO1_IO06/AG11	IO, 3.3V CMOS	General purpose input/output 3.
189	Q7_GPIO4(GPIO5_24)	ART2_RXD/F15	IO, 3.3V CMOS	General purpose input/output 4.
190	Q7_GPIO5(GPIO1_07)	GPIO1_IO07/AF11	IO, 3.3V CMOS	General purpose input/output 5.
191	Q7_GPIO6(GPIO5_25)	UART2_TXD/E15	IO, 3.3V CMOS	General purpose input/output 6.
192	Q7_GPIO7(GPIO1_08)	GPIO1_IO08/AG10	IO, 3.3V CMOS	General purpose input/output 7.

Note: These signals are default configured as input GPIOs (General Purpose Input/Output).

2.10.13 Management Pins

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports Management pins for Reset button input and Power button input.

i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports reset button input (RSTBN) on µQseven Edge connector. Reset button input from µQseven Edge connector is the active low signal which is connected to PMIC's PWRON_B pin in i.MX 8M Mini or i.MX 8M Nano µQseven SOM. Once PWRON_B becomes low PMIC will reset the i.MX 8M Mini SoC by making POR_B input signal to CPU low.

i.MX 8M Mini or i.MX 8M Nano µQseven SOM also supports Power button input (PWRBTN#) on µQseven PCB Edge connector which is the active low signal and connected to i.MX 8M Mini SoC's ONOFF pin. This pin can be used to ON/OFF the i.MX 8M Mini or i.MX 8M Nano SoC by connecting push button in the carrier board. When the board power is On, a button press between 750ms to 5s will send an interrupt to core to request software to bring down the i.MX 8M Mini or i.MX 8M Nano safely (if software supports). Otherwise, button press greater than 5s results in a direct

hardware power down which is applicable when software is unable to power OFF the device. When the i.MX 8M Mini SoC power supply is Off, a button presses greater in duration than 750ms asserts an output signal to request power from a power IC to power up the i.MX 8M Mini or i.MX 8M Nano SoC.

For more details on supported Management Signals pinouts on µQseven PCB Edge connector and corresponding pin description, refer the below table.

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
28	RSTBN	NA	I,3.3V CMOS 100K PU	RESET Input to SOM. *Note: This will restart the power cycle of SOM.* Active low reset button input. *Important Note: This reset input is connected to PMIC's PWRON_B Pin with On-SOM pullup and so don't add any external pullup in carrier board on this pin.*
20	PWRBTN#	ONOFF/ D12	I, 3V CMOS/ 10K PU	Power button input.

2.10.14 Miscellaneous Signals

The i.MX 8MMini µQseven SOM PCB Edge Connector includes the remaining signals from i.MX 8M Mini SoC which includes Board Configuration GPIOs, PWM Signals. For more details on these signal pinouts on µQseven Edge Connector, refer the below table.

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
194	PWM1_OUT(I2C4_SDA)	I2C4_SDA/ E13	O, 3.3V CMOS	PWM1 Output.
196	PWM2_OUT(I2C4_SCL)	I2C4_SCL/ D13	O, 3.3V CMOS	PWM2 Output. *Note: I2C4_SCL is optionally connected for PCIe1_CLKREQ_B to enable CPU internal PCIe Reference clock through a resistor, but default not populated.*
123	GPIO_LVDS_BLT_CTRL(GPIO5_03)	SPDIF_TX/ AF9	O, 3.3V CMOS	LCD Panel backlight brightness control
111	GPIO_LVDS_PPEN(GPIO 5_04)	SPDIF_RX/ AG9	O, 3.3V CMOS	Controls LVDS LCD panel power enable.
112	GPIO2_5_LVDS_BLEN(GPIO5_05)	SPDIF_EXT_ CLK/ AF8	O, 3.3V CMOS	Controls LVDS LCD panel backlight enable.
69	THRM#	NA	O, 3.3V CMOS	Thermal Alarm active low signal
71	GPIO_THRMTRIP_Q7(G PIO1_14)	GPIO1_IO14 /AC9	I, 3.3V CMOS	Overheating indicator
70	Q7_WDTRIG_B	NA	I, 3.3V CMOS	Watchdog trigger.
72	Q7_WDOG_B	NA	O, 3.3V CMOS	Watchdog event indicator.
16	SUS_S5_Q7	NA	O, 3.3V CMOS/ 10K PU	Suspend status. *Note: Not supported*
18	SUS_S3_Q7	NA	O, 3.3V CMOS/ 10K PU	Suspend status. *Note: Not supported*
19	SUS_STAT_Q7	UART3_TXD /D18	O, 3.3V CMOS/10K PU	Suspend status. *Note: Can be used as GPIO*

2.10.15 Power and GND

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM works with single 5V power input (VCC) from µQseven Edge connector and generates all other required powers internally On-SOM itself. i.MX 8M Mini or i.MX 8M Nano µQseven coin cell power input (VDD_RTC) from µQseven PCB Edge Connector to On-SOM RTC controller for real time clock.

µQseven Pin No.	µQseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229 & 230	VCC_5V	NA	I, 5V Power	Supply Voltage.
1, 2, 23, 24, 25, 34, 39, 40, 57, 58, 73, 74, 97, 98, 117, 118, 135, 136, 141, 142, 147, 148, 159, 160, 165, 166, 183, 184, 197 & 198	GND	NA	Power	Ground.
193	VRTC_3V0	NA	I, 3V Power	3V coin cell input for RTC.

2.11 i.MX 8M Mini Pin Multiplexing on µQseven Edge

The i.MX 8M Mini SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8M Mini SOC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8M Mini SoC pin connections to the µQseven edge connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8M Mini Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the µQseven SOM Edge connector for iWave's BSP reusability.

Table 5: i.MX 8M Mini CPU IOMUX for µQseven Edge Connector interfaces

Interface/ Function	µQseven Edge Pin Number	i.MX 8M Mini CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
Carrier SD Interface	43	AA26	USDHC2_CD_B					GPIO2_IO[12]		GPIO2_IO[12]
	42	W23	USDHC2_CLK					GPIO2_IO[13]		GPIO2_IO[13]
	45	W24	USDHC2_CMD					GPIO2_IO[14]		GPIO2_IO[14]
	49	AB23	USDHC2_DATA0					GPIO2_IO[15]		GPIO2_IO[15]
	48	AB24	USDHC2_DATA1					GPIO2_IO[16]		GPIO2_IO[16]
	51	V24	USDHC2_DATA2					GPIO2_IO[17]		GPIO2_IO[17]
	50	V23	USDHC2_DATA3					GPIO2_IO[18]	SRC_EARLY_RESET	GPIO2_IO[18]
PCIe	182	A19	PCIE_RXN_N							PCIE_RXN_N
	180	B19	PCIE_RXN_P							PCIE_RXN_P
	181	A20	PCIE_TXN_N							PCIE_TXN_N
	179	B20	PCIE_TXN_P							PCIE_TXN_P
	156	AD10	GPIO1_IO[10]	USB1_OTG_ID						GPIO1_IO[10]
	158	AC10	GPIO1_IO[11]	USB2_OTG_ID			USDHC3_VSELECT	CCM_PMIC_READY		GPIO1_IO[11]
ECSPI1	203	D6	ECSPI1_SCLK	UART3_RX				GPIO5_IO[6]		GPIO5_IO[6]
	199	B7	ECSPI1_MOSI	UART3_TX				GPIO5_IO[7]		GPIO5_IO[7]
	201	A7	ECSPI1_MISO	UART3_CTS_B				GPIO5_IO[8]		GPIO5_IO[8]
	200	B6	ECSPI1_SS0	UART3_RTS_B				GPIO5_IO[9]		GPIO5_IO[9]
PWM	194	D13	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B			GPIO5_IO[20]		GPIO5_IO[20]
	196	E13	I2C4_SDA	PWM1_OUT				GPIO5_IO[21]		GPIO5_IO[21]

Interface/ Function	µQseven Edge Pin Number	i.MX 8M Mini CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
I2C2	66	D10	I2C2_SCL	ENET1_1588_EVENT1_IN	USDHC3_CD_B			GPIO5_IO[16]		GPIO5_IO[16]
	68	D9	I2C2_SDA	ENET1_1588_EVENT1_OUT	USDHC3_WP			GPIO5_IO[17]		GPIO5_IO[17]
I2C3	150	E10	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO[18]		GPIO5_IO[18]
	152	F10	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO[19]		GPIO5_IO[19]
UART2	172	AG7	SAI3_RX_BCLK	GPT1_CLK	SAI5_RX_BCLK		UART2_CTS_B	GPIO4_IO[29]		GPIO4_IO[29]
	178	AF7	SAI3_RX_DATA[0]	GPT1_COMPARE1	SAI5_RX_DATA[0]		UART2_RTS_B	GPIO4_IO[30]		GPIO4_IO[30]
	177	AC6	SAI3_TX_SYNC	GPT1_CAPTURE2	SAI5_RX_DATA[1]	SAI3_TX_DATA[1]	UART2_RX	GPIO4_IO[31]		GPIO4_IO[31]
	171	AG6	SAI3_TX_BCLK	GPT1_COMPARE2	SAI5_RX_DATA[2]		UART2_TX	GPIO5_IO[0]		GPIO5_IO[0]
UART4	209	F19	UART4_RX	UART2_CTS_B	PCIE1_CLKREQ_B			GPIO5_IO[28]		GPIO5_IO[28]
	208	F18	UART4_TX	UART2_RTS_B				GPIO5_IO[29]		GPIO5_IO[29]
USB1 2.0 OTG	93	A22	USB1_DN							USB1_DN
	95	B22	USB1_DP							USB1_DP
	92	D22	USB1_ID							USB1_ID
	56	AB10	GPIO1_IO[12]	USB1_OTG_PWR				SDMA2_EXT_EVENT[1]		GPIO1_IO[12]
	86	AD9	GPIO1_IO[13]	USB1_OTG_OC				PWM2_OUT		GPIO1_IO[13]
SAI5 Audio	65	AD18	SAI5_RX_DATA[0]	SAI1_TX_DATA[2]				GPIO3_IO[21]		GPIO3_IO[21]
	59	AC14	SAI5_RX_DATA[1]	SAI1_TX_DATA[3]	SAI1_TX_SYNC	SAI5_TX_SYNC		GPIO3_IO[22]		GPIO3_IO[22]
	63	AD13	SAI5_RX_DATA[2]	SAI1_TX_DATA[4]	SAI1_TX_SYNC	SAI5_TX_BCLK		GPIO3_IO[23]		GPIO3_IO[23]
	67	AC13	SAI5_RX_DATA[3]	SAI1_TX_DATA[5]	SAI1_TX_SYNC	SAI5_TX_DATA[0]		GPIO3_IO[24]		GPIO3_IO[24]
JTAG	204	C27	JTAG_TRST_B							CJTAG_TRST_B
	210	F27	JTAG_TMS							CJTAG_TMS
	207	F26	JTAG_TCK							CJTAG_TCK
GPIOs	188	AG11	GPIO1_IO[6]	ENET1_MDC				USDHC1_CD_B	CCM_EXT_CLK3	GPIO1_IO[6]
	190	AF11	GPIO1_IO[7]	ENET1_MDIO				USDHC1_WP	CCM_EXT_CLK4	GPIO1_IO[7]
	186	AF12	GPIO1_IO[5]	M4_NMI				CCM_PMIC_READY		

Interface/ Function	µQseven Edge Pin Number	i.MX 8M Mini CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	192	AG10	GPIO1_IO[8]	ENET1_1588_EVENT0_IN				USDHC2_RESET_B		
	185	E14	UART1_RX	ECSPI3_SCLK				GPIO5_IO[22]		
	187	F13	UART1_TX	ECSPI3_MOSI				GPIO5_IO[23]		
	189	F15	UART2_RX	ECSPI3_MISO				GPIO5_IO[24]		
	191	E15	UART2_TX	ECSPI3_SS0				GPIO5_IO[25]		
	91	AC15	SAI5_RX_BCLK	SAI1_TX_DATA[1]				GPIO3_IO[20]		GPIO3_IO[20]
	178	AF9	SPDIF1_OUT	PWM3_OUT				GPIO5_IO[3]		GPIO5_IO[3]
	177	AG9	SPDIF1_IN	PWM2_OUT				GPIO5_IO[4]		GPIO5_IO[4]
	176	AF8	SPDIF1_EXT_CLK	PWM1_OUT				GPIO5_IO[5]		GPIO5_IO[5]

Important Note: The SAI1 signals which is having Boot configuration functionality in Funtion6 -BOOT_CFG[0:15] are also used for i.MX 8M Mini SoC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot media configurations.

2.12 i.MX 8M Nano Pin Multiplexing on µQseven Edge

The i.MX 8M Nano SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8M Nano SOC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8M Nano SoC pin connections to the µQseven edge connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8M Nano Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the µQseven SOM Edge connector for iWave's BSP reusability

Interface/ Function	µQseven Edge Pin Number	i.MX 8M Nano CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
Carrier SD Interface	43	AA26	USDHC2_CD_B					GPIO2_IO[12]		GPIO2_IO[12]
	42	W23	USDHC2_CLK					GPIO2_IO[13]		GPIO2_IO[13]
	45	W24	USDHC2_CMD					GPIO2_IO[14]		GPIO2_IO[14]
	49	AB23	USDHC2_DATA0					GPIO2_IO[15]		GPIO2_IO[15]
	48	AB24	USDHC2_DATA1					GPIO2_IO[16]		GPIO2_IO[16]
	51	V24	USDHC2_DATA2					GPIO2_IO[17]		GPIO2_IO[17]
	50	V23	USDHC2_DATA3					GPIO2_IO[18]		GPIO2_IO[18]
ECSPI1	203	D6	ECSPI1_SCLK	UART3_RX				GPIO5_IO[6]		GPIO5_IO[6]
	199	B7	ECSPI1_MOSI	UART3_TX				GPIO5_IO[7]		GPIO5_IO[7]
	201	A7	ECSPI1_MISO	UART3_CTS_B				GPIO5_IO[8]		GPIO5_IO[8]
	200	B6	ECSPI1_SS0	UART3_RTS_B				GPIO5_IO[9]		GPIO5_IO[9]
PWM	194	D13	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B			GPIO5_IO[20]		GPIO5_IO[20]
	196	E13	I2C4_SDA	PWM1_OUT				GPIO5_IO[21]		GPIO5_IO[21]
I2C2	66	D10	I2C2_SCL	ENET1_1588_EVENT1_IN	USDHC3_CD_B			GPIO5_IO[16]		GPIO5_IO[16]
	68	D9	I2C2_SDA	ENET1_1588_EVENT1_OUT	USDHC3_WP			GPIO5_IO[17]		GPIO5_IO[17]
I2C3	150	E10	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO[18]		GPIO5_IO[18]
	152	F10	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO[19]		GPIO5_IO[19]
UART2	172	AG7	SAI3_RX_BCLK	GPT1_CLK	SAI5_RX_BCLK		UART2_CTS_B	GPIO4_IO[29]		GPIO4_IO[29]
	178	AF7	SAI3_RX_DATA[0]	GPT1_COMPARE1	SAI5_RX_DATA[0]		UART2_RTS_B	GPIO4_IO[30]		GPIO4_IO[30]
	177	AC6	SAI3_TX_SYNC	GPT1_CAPTURE2	SAI5_RX_DATA[1]	SAI3_TX_DATA[1]	UART2_RX	GPIO4_IO[31]		GPIO4_IO[31]

Interface/ Function	µQseven Edge Pin Number	i.MX 8M Nano CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	171	AG6	SAI3_TX_BCLK	GPT1_COMPARE2	SAI5_RX_DATA[2]		UART2_TX	GPIO5_IO[0]		GPIO5_IO[0]
UART4	209	F19	UART4_RX	UART2_CTS_B				GPIO5_IO[28]		GPIO5_IO[28]
	208	F18	UART4_TX	UART2_RTS_B				GPIO5_IO[29]		GPIO5_IO[29]
USB1 2.0 OTG	93	A22	USB1_DN							USB1_DN
	95	B22	USB1_DP							USB1_DP
	92	D22	USB1_ID							USB1_ID
	56	AB10	GPIO1_IO[12]	USB1_OTG_PWR				SDMA2_EXT_EVENT[1]		GPIO1_IO[12]
	86	AD9	GPIO1_IO[13]	USB1_OTG_OC				PWM2_OUT		GPIO1_IO[13]
SAI5 Audio	65	AD18	SAI5_RX_DATA[0]				PDM_BIT_STREAM0	GPIO3_IO[21]		GPIO3_IO[21]
	59	AC14	SAI5_RX_DATA[1]			SAI5_TX_SYNC	PDM_BIT_STREAM1	GPIO3_IO[22]		GPIO3_IO[22]
	63	AD13	SAI5_RX_DATA[2]			SAI5_TX_BCLK	PDM_BIT_STREAM2	GPIO3_IO[23]		GPIO3_IO[23]
	67	AC13	SAI5_RX_DATA[3]			SAI5_TX_DATA[0]	PDM_BIT_STREAM3	GPIO3_IO[24]		GPIO3_IO[24]
JTAG	204	C27	CJTAG_TRST_B							CJTAG_TRST_B
	210	F27	CJTAG_TMS							CJTAG_TMS
	207	F26	CJTAG_TCK							CJTAG_TCK
GPIOs	188	AG11	GPIO1_IO[6]	ENET1_MDC				USDHC1_CD_B	CCM_EXT_CLK3	GPIO1_IO[6]
	190	AF11	GPIO1_IO[7]	ENET1_MDIO				USDHC1_WP	CCM_EXT_CLK4	GPIO1_IO[7]
	186	AF12	GPIO1_IO[5]	M4_NMI				CCM_PMIC_READY		
	192	AG10	GPIO1_IO[8]	ENET1_1588_EVENT0_IN				USDHC2_RESET_B		
	185	E14	UART1_RX	ECSPI3_SCLK				GPIO5_IO[22]		
	187	F13	UART1_TX	ECSPI3_MOSI				GPIO5_IO[23]		
	189	F15	UART2_RX	ECSPI3_MISO				GPIO5_IO[24]		
	191	E15	UART2_TX	ECSPI3_SS0				GPIO5_IO[25]		

Interface/ Function	µQseven Edge Pin Number	i.MX 8M Nano CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	91	AC15	SAI5_RX_BCLK	SAI1_TX_DATA[1]				GPIO3_IO[20]		GPIO3_IO[20]
	178	AF9	SPDIF1_OUT	PWM3_OUT				GPIO5_IO[3]		GPIO5_IO[3]
	177	AG9	SPDIF1_IN	PWM2_OUT				GPIO5_IO[4]		GPIO5_IO[4]
	176	AF8	SPDIF1_EXT_CLK	PWM1_OUT				GPIO5_IO[5]		GPIO5_IO[5]

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8M Mini or i.MX 8M Nano µQseven SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the VCC_5V pins and returned through the numerous GND pins on the connector. A Module will withstand an indefinite exposure to an applied VCC_5V that 4.75V to 5.25V range. 12 pins are allocated to VCC_5V. The connector pin current rating is 0.5A per pin. This works out to 6A total for the 12 pins.

Table 6: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75	5V	5.25V	±50mV
2	VCC_RTC[2]	2.4V	3V	3.3V	±20 mV

[1] i.MX 8M Mini or i.MX 8M Nano µQseven SOM is designed to work with VCC_5V input power rail from µQseven Edge connector.

[2]i.MX 8M Mini or i.MX 8M Nano µQseven SOM uses this voltage as backup power source to RTC controller when VCC is off. This power is an optional power and can be left open if RTC functionality is not required.

3.1.1 Power Input Sequencing

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM's Power Input sequence requirement is explained below.

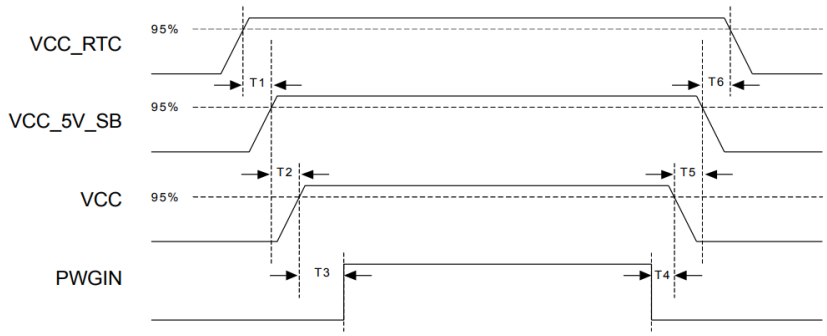

Figure 9: Power Input Sequencing

Table 7: Power Sequence Timing

Item	Description	Value
T1	VCC_RTC rise to VCC_5V_SB rise	≥ 0 ms
T2	VCC_5V_SB rise to VCC rise	≥ 0 ms
T3	VCC rise to PWGIN rise	≥ 0 ms

T4	PWGIN fall to VCC fall	≥ 0 ms
T5	VCC fall to VCC_5V_SB fall	≥ 0 ms
T6	VCC_5V_SB fall to VCC_RTC fall	≥ 0 ms

Important Note: All carrier board power supplies should be powered ON only after the SOM is powered ON completely. Also make sure that all Carrier board interface peripherals' power supply must be OFF if SOM is powered OFF, otherwise it can cause internal latch-up and malfunctions/boot up issues due to reverse current flows. NXP recommends customers to remove power (Voltage source) to all components on the board in the event of a processor reset.

3.2 Power Consumption

Table 8: i.MX 8M Mini µQseven Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Audio	VCC_5V	TBD
Play Video run in HDMI Display[2]	VCC_5V	TBD
Play Video run in LVDS Display[2]	VCC_5V	TBD
Ping Bluetooth	VCC_5V	TBD
Ping Wi-Fi	VCC_5V	TBD
Ping Ethernet at 1000Mbps	VCC_5V	TBD
Ping Ethernet at 100Mbps	VCC_5V	TBD
Ping Ethernet at 10Mbps	VCC_5V	TBD
Ethernet Streaming (Video Play)	VCC_5V	TBD
eMMC to Carrier Standard SD file transfer	VCC_5V	TBD
eMMC to USB2.0 file transfer	VCC_5V	TBD
eMMC to PCIe file transfer	VCC_5V	TBD
Bluetooth file transfer	VCC_5V	TBD
GPU Processor -Graphics 3D Test	VCC_5V	TBD
Transfer the 1MB file between USB2.0, PCIe and Carrier SD with 1000 count	VCC_5V	TBD
Dhrystone	VCC_5V	TBD
Typical Maximum Power: Run the below during Maximum Power Test, • Run the video on HDMI using Gplay • Ethernet - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1GB files in storage devices • Run the Graphics (GPU) application on LVDS/HDMI • Bluetooth ping • Wi-Fi ping	VCC_5V	TBD
Low Power Mode Power Consumption		
System Idle Mode	VCC_5V	TBD
Deep Sleep Mode	VCC_5V	TBD
RTC power when no VCC_5V supply is provided	VRTC_3V0	TBD

[1] Power consumption measurements have been done in iWave's i.MX 8M based µQseven Development platform with iWave's iW-PRGNZ-SC-01-R3.0-REL0.1-Linux_5.4.70_2.3.0 BSP.

[2] At a time either LVDS or HDMI can be supported. By default, HDMI is supported.

Table 9: i.MX 8M Nano µQseven Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Audio	VCC_5V	TBD
Play Video run in HDMI Display[2]	VCC_5V	TBD
Play Video run in LVDS Display[2]	VCC_5V	TBD
Ping Bluetooth	VCC_5V	TBD
Ping Wi-Fi	VCC_5V	TBD
Ping Ethernet at 1000Mbps	VCC_5V	TBD
Ping Ethernet at 100Mbps	VCC_5V	TBD
Ping Ethernet at 10Mbps	VCC_5V	TBD
Ethernet Streaming (Video Play)	VCC_5V	TBD
eMMC to Carrier microSD file transfer	VCC_5V	TBD
eMMC to USB2.0 file transfer	VCC_5V	TBD
Bluetooth file transfer	VCC_5V	TBD
GPU Processor -Graphics 3D Test	VCC_5V	TBD
Transfer the 1MB file between USB2.0 and Carrier SD with 1000 count	VCC_5V	TBD
Dhrystone	VCC_5V	TBD
Typical Maximum Power: • Run the below during Maximum Power Test, • Run the video on HDMI using Gplay • Ethernet - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1GB files in storage devices • Run the Graphics (GPU) application on HDMI • Bluetooth ping • Wi-Fi ping	VCC_5V	TBD
Low Power Mode Power Consumption		
System Idle Mode	VCC_5V	TBD
Deep Sleep Mode	VCC_5V	TBD
RTC power when no VCC_5V supply is provided	VRTC_3V0	TBD

[1] Power consumption measurements have been done in iWave's i.MX 8M Nano SoC based µQseven Development platform with iWave's iW-PRGNZ-SC-01-R3.0-REL0.1-Linux_5.4.70_2.3.0 BSP.

[2] At a time either LVDS or HDMI can be supported. By default, HDMI is supported.

3.3 EnvironmentalCharacteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX 8M Mini or i.MX 8M Nano µQseven SOM.

Table 10: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2]The LBEE5HY1MW Wi-Fi & BT module supports operating temperature -30°C to 85°C with the default module's firmware. To set the module temperature to industrial grade in firmware, please contact iWave.

[3] If Micro SD connector has to be supported in i.MX 8M µQseven SOM, operating temperature range is -25°C to 85°C.

[4] For more information on Thermal solution & Heat sink/ Heat Spreader refer the following section.

3.3.2 Heat Sink/ Heat Spreader

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique like Heat spreader, Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the CPU.

Note: iWave supports Heat Sink/ Heat Spreader Solution for i.MX 8M Mini or i.MX 8M Nano µQseven SOM. For more information on Heat Sink/ Heat Spreader contact iWave support team. Do not Power On the SOM without a proper thermal solution.

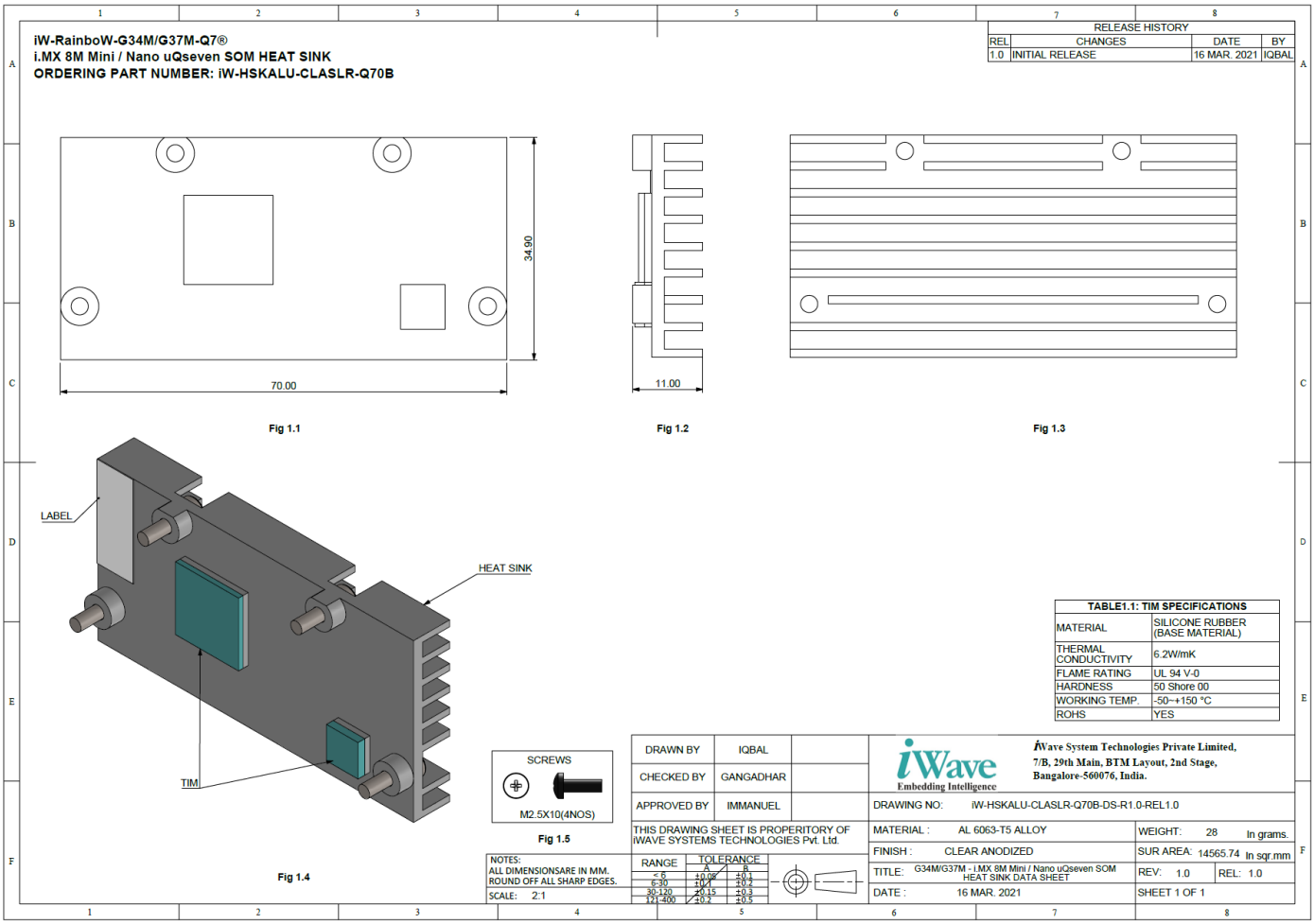

Figure 10: Mechanical dimension Heat Sink

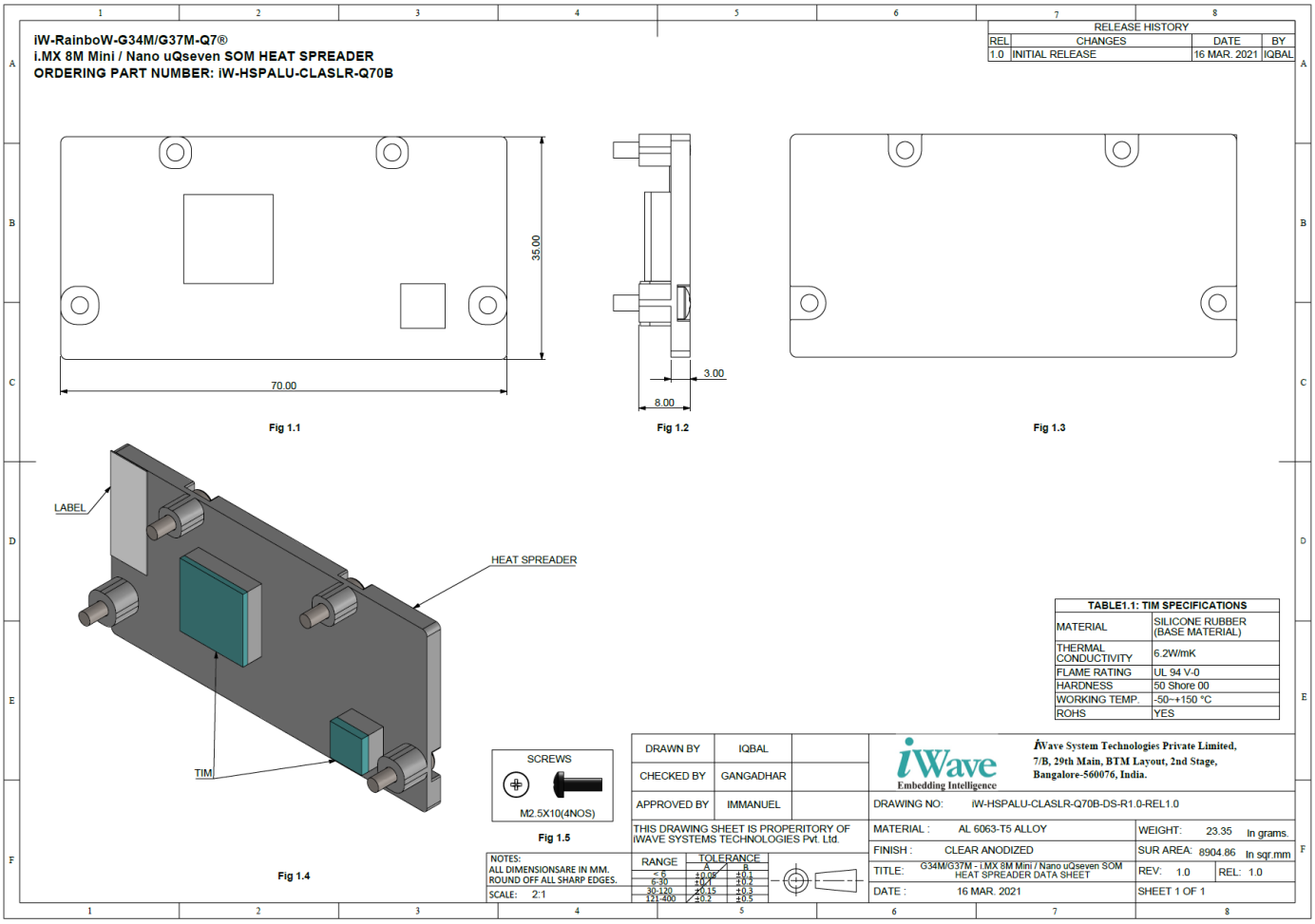

Figure 11: Mechanical dimension Heat Spreader

3.3.3 RoHS Compliance

iWave's i.MX 8M Mini or i.MX 8M Nano µQseven SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.4 Electrostatic Discharge

iWave's i.MX 8M Mini or i.MX 8M Nano µQseven SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage SOM e of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX 8M Mini or i.MX 8M Nano µQseven SOM Mechanical Dimensions

i.MX 8M Mini or i.MX 8M Nano µQseven SOM PCB size is 40mm x 70mm x 1.2mm. µQseven SOM mechanical dimension is shown below. (All dimensions are shown in mm)

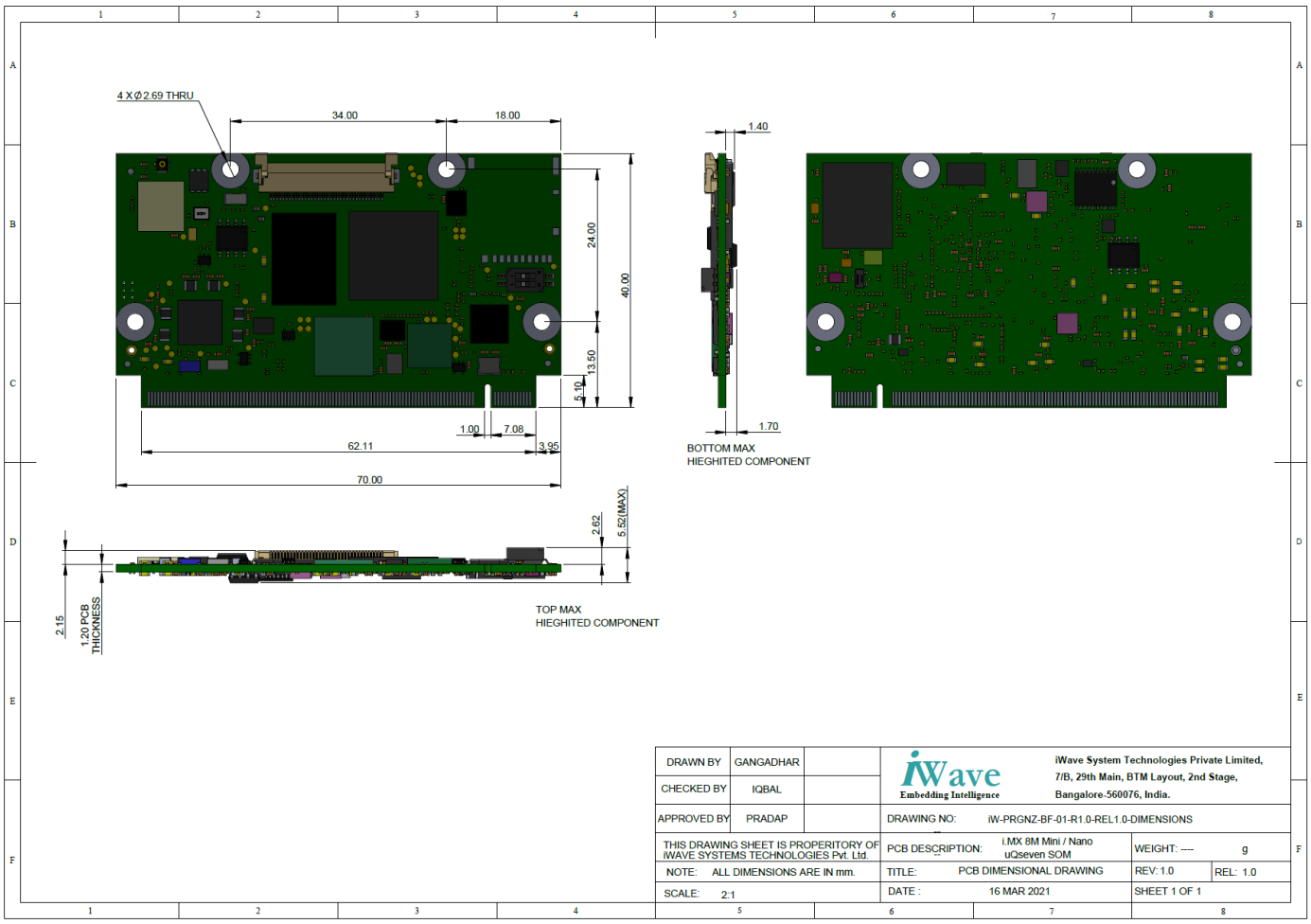

Figure 12: Mechanical dimension of i.MX 8M Mini or i.MX 8M Nano µQseven SOM

The i.MX 8M Mini or i.MX 8M Nano µQseven SOM PCB thickness is 1.2mm±0.1mm, top side maximum height component is 2.62mm (Boot media switch will be the maximum height on Top side followed by MIPI CSI Connector 2.15mm) and bottom side maximum height component is QSPI (1.70mm) which is optional in default configuration hence U22 IC (1.40mm) will be the maximum height on bottom side in default configuration. Please refer the above figure which gives height details of the i.MX 8M Mini µQseven SOM.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8M Mini or i.MX 8M Nano µQseven SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 11: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G34M - i.MX 8M Mini µQseven SOM (Industrial grade) with 1GB LPDDR4, Wi-Fi & Ethernet		
iW-G34M-Q704-4L001G-E008G-BIE	i.MX 8M Mini Quad, 1GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q74L-4L001G-E008G-BIE	i.MX 8M Mini Quad Lite, 1GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q702-4L001G-E008G-BIE	i.MX 8M Mini Dual, 1GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q72L-4L001G-E008G-BIE	i.MX 8M Mini Dual Lite, 1GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q701-4L001G-E008G-BIE	i.MX 8M Mini Solo, 1GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q71L-4L001G-E008G-BIE	i.MX 8M Mini Solo Lite, 1GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-Rainbow G34M - i.MX 8M Mini µQseven SOM (Industrial grade) with 2GB LPDDR4, Wi-Fi & Ethernet		
iW-G34M-Q704-4L002G-E008G-BIE	i.MX 8M Mini Quad, 2GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q74L-4L002G-E008G-BIE	i.MX 8M Mini Quad Lite, 2GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q702-4L002G-E008G-BIE	i.MX 8M Mini Dual, 2GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q72L-4L002G-E008G-BIE	i.MX 8M Mini Dual Lite, 2GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q701-4L002G-E008G-BIE	i.MX 8M Mini Solo, 2GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G34M-Q71L-4L002G-E008G-BIE	i.MX 8M Mini Solo Lite, 2GB LPDDR4, 8GB eMMC, ETH with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-Rainbow G34M - i.MX 8M Mini µQseven (Industrial grade) SOM with 1GB LPDDR4 & without Wi-Fi		
iW-G34M-Q704-4L001G-E008G-BIF	i.MX 8M Mini Quad, 1GB LPDDR4, 8GB eMMC, ETH with boot code	-40°C to 85°C
iW-G34M-Q74L-4L001G-E008G-BIF	i.MX 8M Mini Quad Lite, 1GB LPDDR4, 8GB eMMC, ETH with boot code	-40°C to 85°C
iW-G34M-Q702-4L001G-E008G-BIF	i.MX 8M Mini Dual, 1GB LPDDR4, 8GB eMMC, ETH with boot code	-40°C to 85°C

Product Part Number	Description	Temperature
iW-G34M-Q72L-4L001G-E008G-BIF	i.MX 8M Mini Dual Lite, 1GB LPDDR4, 8GB eMMC, ETH with boot code	-40°C to 85°C
iW-Rainbow G34M - i.MX 8M Mini µQseven (Industrial grade) SOM with 2GB LPDDR4 & without Wi-Fi		
iW-G34M-Q704-4L002G-E008G-BIF	i.MX 8M Mini Quad, 2GB LPDDR4, 8GB eMMC, ETH with boot code	-40°C to 85°C
iW-G34M-Q74L-4L002G-E008G-BIF	i.MX 8M Mini Quad Lite, 2GB LPDDR4, 8GB eMMC, ETH with boot code	-40°C to 85°C
iW-G34M-Q702-4L002G-E008G-BIF	i.MX 8M Mini Dual, 2GB LPDDR4, 8GB eMMC, ETH with boot code	-40°C to 85°C
iW-G34M-Q72L-4L002G-E008G-BIF	i.MX 8M Mini Dual Lite, 2GB LPDDR4, 8GB eMMC, ETH with boot code	-40°C to 85°C
iW-Rainbow G37M - i.MX 8M Nano µQseven SOM (Industrial grade) with 1GB LPDDR4 and Wi-Fi		
iW-G37M-Q704-4L001G-E008G-BIC	i.MX8M Nano Quad, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-Q74L-4L001G-E008G-BIC	i.MX8M Nano Quad Lite, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-Q702-4L001G-E008G-BIC	i.MX8M Nano Dual, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-Q72L-4L001G-E008G-BIC	i.MX8M Nano Dual Lite, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-Q701-4L001G-E008G-BIC	i.MX8M Nano Solo, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-G37M-Q71L-4L001G-E008G-BIC	i.MX8M Nano Solo Lite, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT with boot code	-40°C to 85°C
iW-Rainbow G37M - i.MX 8M Nano µQseven SOM (Industrial grade) with 1GB LPDDR4 without Wi-Fi		
iW-G37M-Q704-4L001G-E008G-BID	i.MX8M Nano Quad, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-Q74L-4L001G-E008G-BID	i.MX8M Nano Quad Lite, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-Q702-4L001G-E008G-BID	i.MX8M Nano Dual, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-Q72L-4L001G-E008G-BID	i.MX8M Nano Dual Lite, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-Q701-4L001G-E008G-BID	i.MX8M Nano Solo, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C
iW-G37M-Q71L-4L001G-E008G-BID	i.MX8M Nano Solo Lite, 1GB LPDDR4, 8GB eMMC with boot code	-40°C to 85°C

Important Note: Some of the above-mentioned Part Numbers are subject to MOQ purchase. Please contact iWave for further details.

For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with Barcode readable format on SOM.

APPENDIX I

4.1 i.MX 8M Mini or i.MX 8M Nano µQseven SOM Development Platform

iWave Systems supports iW-RainboW-G34D/G37D-i.MX 8M Mini or i.MX 8M Nano µQseven SOM Development Platform which is targeted for quick validation of i.MX 8M Mini or i.MX 8M Nano SoC based µQseven SOM and its features. Being a Nano-ITX form factor with 120mm x 120mm size, the carrier board is highly packed with all necessary interfaces & on-board connectors to validate complete supported features.

https://www.iwavesystems.com/product/i-mx-8m-mini-nano-uqseven-som/

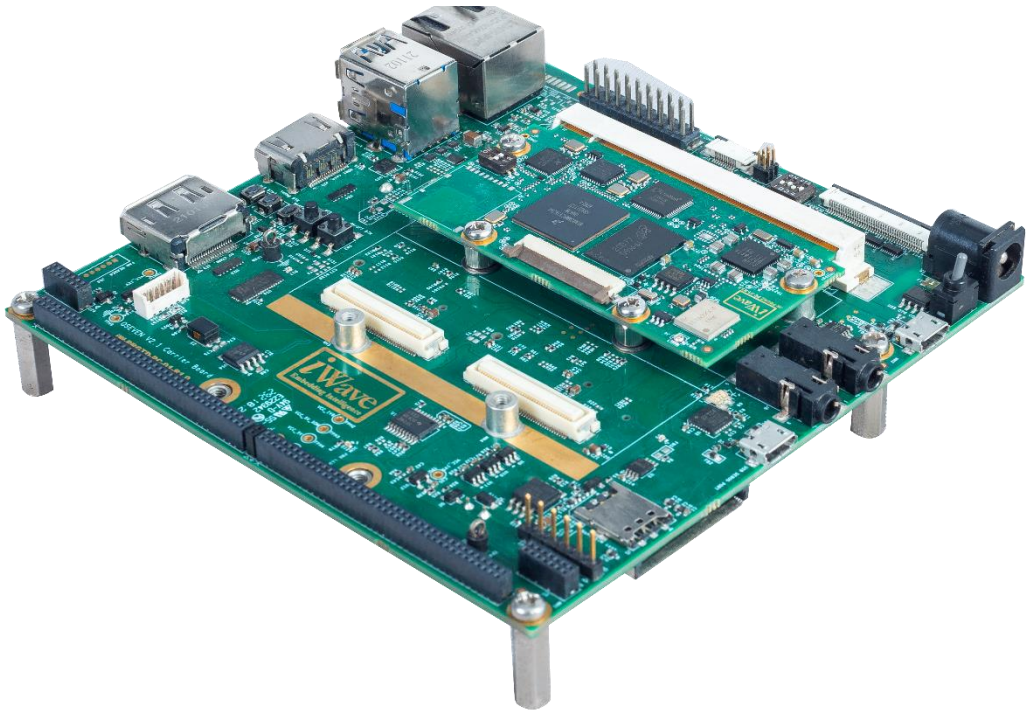

Figure 13: i.MX 8M Mini or i.MX 8M Nano µQseven SOM Development Platform


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