



TPS92560 Simple Led Driver for MR16 and AR111 Applications

1 Features

- Controlled peak input current to prevent over-stressing of the electronic transformer
- Allows Either Step-Up or Step-Up/Down Operation
- Compatible to Generic Electronic Transformers
- Compatible to Magnetic Transformers and DC Power Supplies
- Integrated Active Low-Side Input Rectifiers
- Compact and Simple Circuit
- >85% Efficiency (12-VDC Input)
- Power Factor > 0.9 (Full Load With AC input)
- Hysteretic Control Scheme
- Output Overvoltage Protection
- Overtemperature Shutdown
- 10-pin Thermally Enhanced Very-Thin Fine Pitch Small-Outline Package

2 Applications

- MR16/AR111 LED Lamps
- Lighting System Using Electronic Transformer
- General Lighting Systems That Require a Boost / SEPIC LED Driver

3 Description

The TPS92560 is a simple LED driver designed to drive high-power LEDs by drawing constant current from the power source. The device is ideal for MR16 and AR111 applications, which require good compatibility to DC and AC voltages and electronic transformers. The hysteretic control scheme does not need control loop compensation while providing the benefits of fast transient response and high power factor. The patent pending feedback control method allows the output power to be determined by the number of LED used without component change. The TPS92560 supports both boost and SEPIC configurations for the use of different LED modules.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92560	HVSSOP (10)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

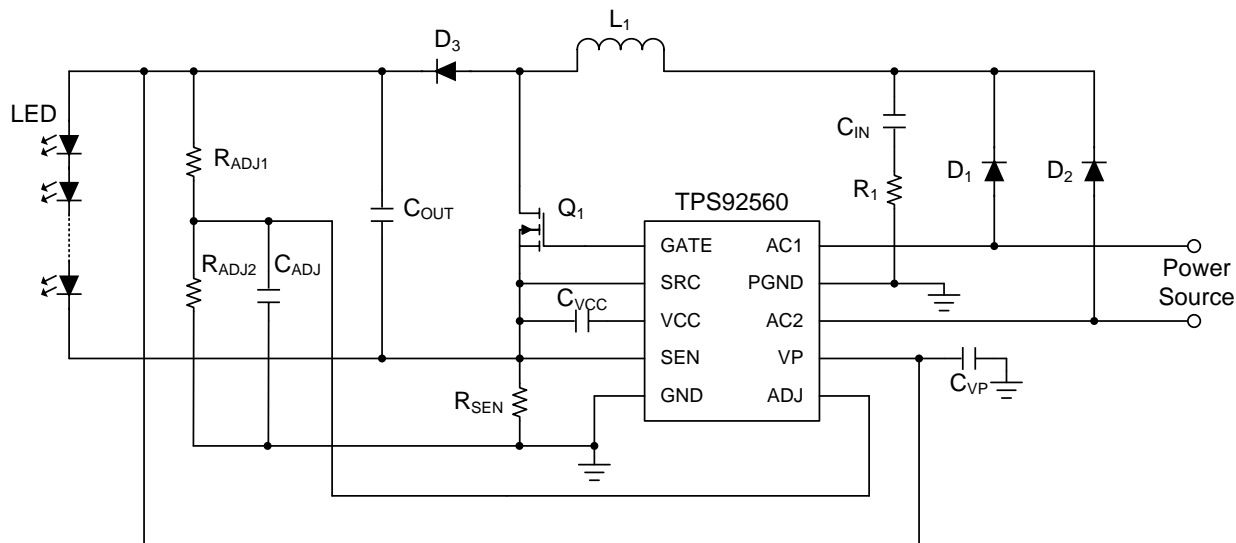


Table of Contents

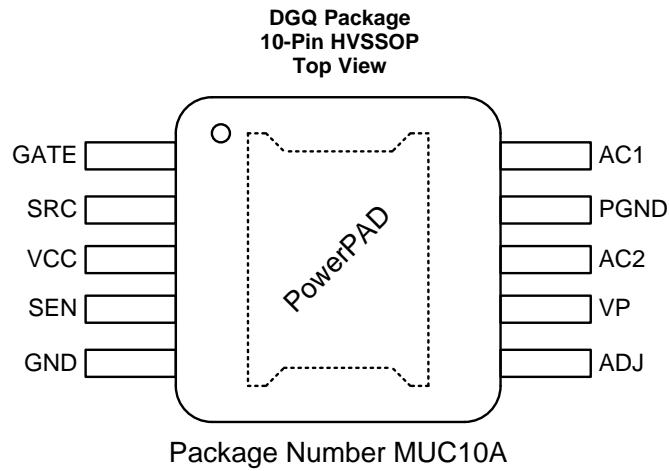
1 Features	1	7.3 Feature Description.....	10
2 Applications	1	7.4 Device Functional Modes.....	14
3 Description	1	8 Application and Implementation	15
4 Revision History	2	8.1 Application Information.....	15
5 Pin Configuration and Functions	3	8.2 Typical Applications	16
6 Specifications	4	9 Power Supply Recommendations	21
6.1 Absolute Maximum Ratings	4	10 Layout	21
6.2 ESD Ratings.....	4	10.1 Layout Guidelines	21
6.3 Recommended Operating Conditions.....	4	10.2 Layout Example	21
6.4 Thermal Information	4	11 Device and Documentation Support	22
6.5 Electrical Characteristics.....	5	11.1 Community Resources.....	22
6.6 Typical Characteristics.....	7	11.2 Trademarks	22
7 Detailed Description	9	11.3 Electrostatic Discharge Caution.....	22
7.1 Overview	9	11.4 Glossary	22
7.2 Functional Block Diagram	9	12 Mechanical, Packaging, and Orderable Information	22

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2013) to Revision B	Page
<ul style="list-style-type: none"> Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	GATE	O	Gate driver output pin	Connect to the Gate terminal of the low-side N-channel Power FET
2	SRC	I	Gate driver return	Connect to the Source terminal of the low-side N-channel Power FET
3	VCC	O	VCC regulator output	Connect 0.47-μF decoupling capacitor from this pin to SRC pin
4	SEN	I	Current sense pin	Kelvin-sense current sensing input. Should connect to the current sensing resistor, R_{SEN} .
5	GND	—	Analog ground	Reference point for current sensing.
6	ADJ	I	LED current adjust pin	Connect to resistor divider from LED top voltage rail to set LED current
7	VP	I	Power supply of the IC	Connect it to the LED top voltage rail (for boost) or Connect it through a diode from LED top voltage rail (for SEPIC)
8	AC2	I	Power return terminal	Connect to AC or DC input terminal
9	PGND	—	Power ground	Connect to system ground plane
10	AC1	I	Power return terminal	Connect to AC or DC input terminal
PowerPAD™		—	Thermal DAP	Connect to system ground plane for heat dissipation

6 Specifications

6.1 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.⁽¹⁾

	MIN	MAX	UNIT
SRC, SEN, ADJ	−0.3	5	V
AC1, AC2	−1	45	V
VP	−0.3	45	V
VCC	−0.3	12	V
T _J Junction temperature	−40	125	°C
T _{stg} Storage temperature	−65	150	°C

(1) Absolute Maximum Ratings are limits which damage to the device may occur. Operating ratings are conditions under which operation of the device is intended to be functional. For specified specifications and test conditions, see the electrical characteristics.

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VP Supply voltage	6.5		42	V
T _J Junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS92560	UNIT
		DGQ (HVSSOP)	
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	55.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	43.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	32.1	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	31.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	5.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Over recommended operating conditions with $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$. Unless otherwise stated the following conditions apply: $V_{VP} = 12\text{V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{IN}	V_{IN} Operating current	$6.5\text{ V} < V_{VP} < 42\text{ V}$	0.7	1.4	1.95	mA
VCC REGULATOR						
V_{CC}	V_{CC} Regulated voltage ⁽¹⁾	$I_{CC} \leq 10\text{ mA}$, $C_{VCC} = 0.47\text{ }\mu\text{F}$ $12\text{ V} < V_{VP} < 42\text{ V}$	7.82	8.45	9.08	V
		$I_{CC} = 10\text{ mA}$, $C_{VCC} = 0.47\text{ }\mu\text{F}$ $V_{VP} = 6.5\text{ V}$	5.22	5.8	6.18	
		$I_{CC} = 0\text{ mA}$, $C_{VCC} = 0.47\text{ }\mu\text{F}$ $V_{VP} = 2\text{ V}$	1.96	2		
I_{CC-LIM}	V_{CC} Current limit	$V_{CC} = 0\text{ V}$ $6.5\text{ V} < V_{VP} < 42\text{ V}$	21	30	39	mA
$V_{CC-UVLO-UPTH}$	V_{CC} UVLO upper threshold		5	5.38	5.76	V
$V_{CC-UVLO-LOTH}$	V_{CC} UVLO lower threshold		4.63	4.98	5.33	V
$V_{CC-UVLO-HYS}$	V_{CC} UVLO hysteresis		190	400	640	mV
MOSFET GATE DRIVER						
$V_{GATE-HIGH}$	Gate driver output high	w.r.t. SRC Sinking 100mA from GATE Force $V_{CC} = 8.5\text{ V}$	7.61	8.1	8.5	V
$V_{GATE-LOW}$	Gate driver output low	w.r.t. SRC Sourcing 100 mA to GATE	100	180	290	mV
t_{RISE}	V_{GATE} Rise time	$C_{GATE} = 1\text{ nF}$ across GATE and SRC		22		ns
t_{FALL}	V_{GATE} Fall time	$C_{GATE} = 1\text{ nF}$ across GATE and SRC		14		ns
$t_{RISE-PG-DELAY}$	V_{GATE} Low-to-high propagation delay	$C_{GATE} = 1\text{ nF}$ across GATE and SRC		68		ns
$t_{FALL-PG-DELAY}$	V_{GATE} High-to-low propagation delay	$C_{GATE} = 1\text{ nF}$ across GATE and SRC		84		ns
CURRENT SOURCE AT ADJ PIN						
$I_{ADJ-STARTUP}$	Output current of ADJ pin at start-up	$V_{ADJ} = 0\text{ V}$	16	20	24	μA
$I_{ADJ-ELEC-XFR}$	Output current of ADJ pin for electronic transformers	An Electronic transformer is detected	8	11.5	15	μA
$I_{ADJ-MAG-XFR}$	Output current of ADJ pin for inductive transformers	A magnetic transformer is detected	7	9.5	12	μA
CURRENT SENSE COMPARATOR						
$V_{SEN-UPPER-TH}$	V_{SEN} Upper threshold over V_{ADJ}	$V_{SEN}-V_{ADJ}$, $V_{ADJ}=0.2\text{ V}$, V_{GATE} at falling edge	8.9	14.9	20.9	mV
$V_{SEN-LOWER-TH}$	V_{SEN} Lower threshold over V_{ADJ}	$V_{SEN}-V_{ADJ}$, $V_{ADJ}=0.2\text{ V}$ V_{GATE} at rising edge	-20.6	-14.9	-8.8	mV
$V_{SEN-HYS}$	V_{SEN} Hysteresis	$(V_{SEN-UPPER-TH} - V_{SEN-LOWER-TH})$	22.5	29.8	37.5	mV
$V_{SEN-OFFSET}$	V_{SEN} Offset w.r.t. V_{ADJ}	$(V_{SEN-UPPER-TH} + V_{SEN-LOWER-TH})/2$	-3.5	0.02	3.5	mV
ACTIVE LOW-SIDE INPUT RECTIFIERS						
R_{ACn-ON}	In resistance of AC1 and AC2 to GND	$I_{ACn} = 200\text{ mA}$		300	570	m Ω
$V_{ACn-ON-TH}$	Turn ON voltage threshold of AC1 and AC2	V_{ACn} Decreasing, $T_J = 25^{\circ}\text{C}$	36	52	67	mV
$V_{ACn-OFF-TH}$	Turn OFF voltage threshold of AC1 and AC2	V_{ACn} Increasing, $T_J = 25^{\circ}\text{C}$	77	90	104	mV
$V_{ACn-TH-HYS}$	Hysteresis voltage of AC1 and AC2	$V_{ACn-OFF-TH} - V_{ACn-ON-TH}$		39		mV

(1) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Electrical Characteristics (continued)

Over recommended operating conditions with $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$. Unless otherwise stated the following conditions apply: $V_{VP} = 12\text{V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{ACn-OFF}$	Off current of AC1 and AC2	$V_{ACn} = 45\text{ V}$		21	32	μA
OUTPUT OVERVOLTAGE-PROTECTION (OVP)						
$V_{ADJ-OVP-UPTH}$	Output overvoltage-detection upper threshold	V_{ADJ} Increasing, V_{GATE} at falling edge	0.353	0.384	0.415	V
$V_{ADJ-OVP-LOTH}$	Output overvoltage-detection lower threshold	V_{ADJ} Decreasing, V_{GATE} at rising edge	0.312	0.339	0.366	V
$V_{ADJ-OVP-HYS}$	Output overvoltage-detection hysteresis	$V_{ADJ-OVP-UPTH} - V_{ADJ-OVP-LOTH}$	25	46	67	mV
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	T_J Rising		165		$^{\circ}\text{C}$
T_{SD-HYS}	Thermal shutdown temperature hysteresis	T_J Falling		30		$^{\circ}\text{C}$

6.6 Typical Characteristics

All curves taken for the boost circuit are with 500-mA nominal input current and 6 serial LEDs. All curves taken for the SEPIC circuit are with 500-mA nominal input current and 3 serial LEDs. $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise specified.

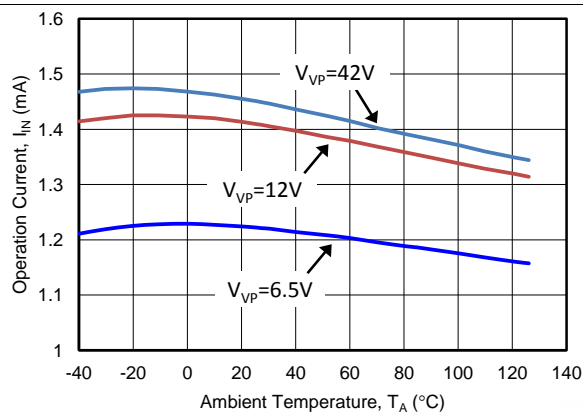


Figure 1. Operation Current vs Temperature

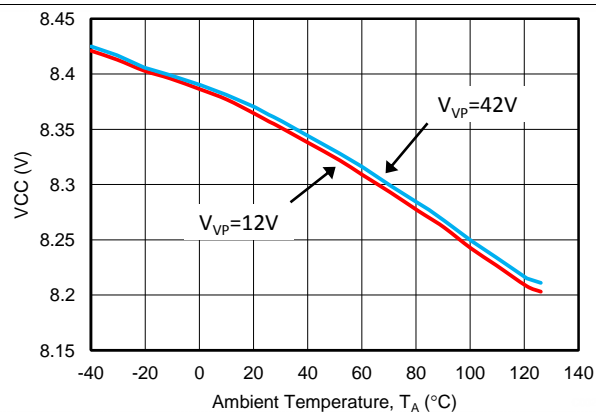


Figure 2. VCC vs Temperature ($I_{VCC} = 0$ mA)

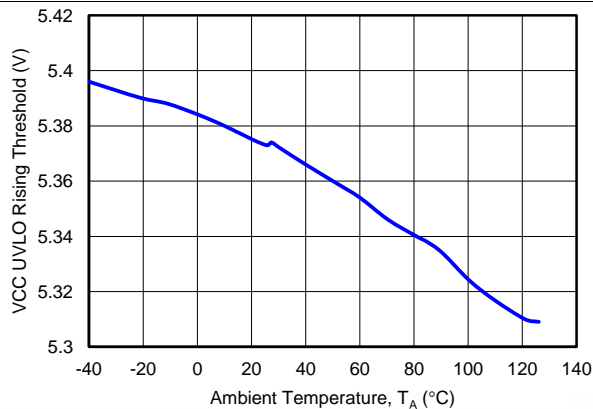


Figure 3. VCC UVLO Rising Threshold vs Temperature
 $V_{TP} = 12$ V, GATE = Hi

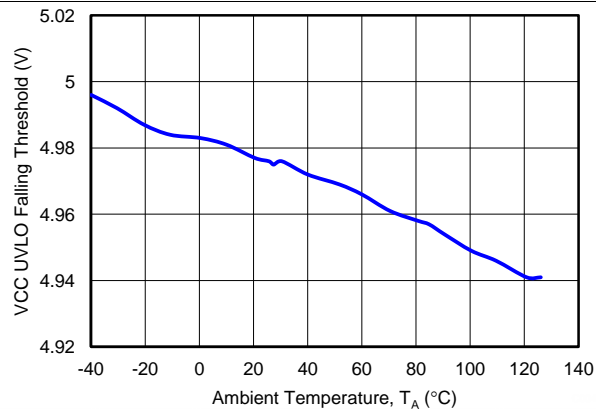


Figure 4. VCC UVLO Falling Threshold vs Temperature
 $V_{TP} = 12$ V, GATE = Low

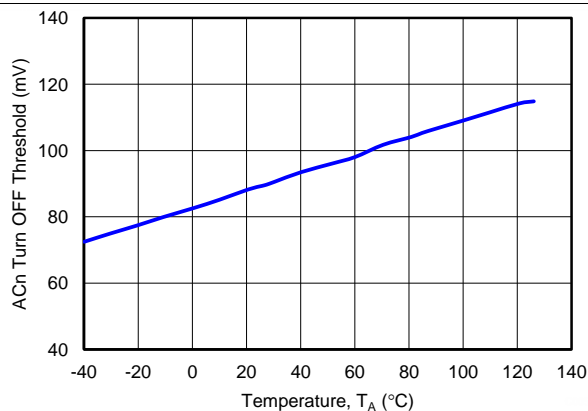


Figure 5. ACn Turn Off Threshold vs Temperature

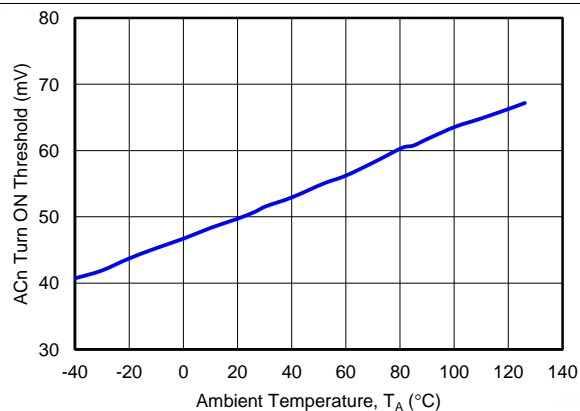


Figure 6. ACn Turn On Threshold vs Temperature

Typical Characteristics (continued)

All curves taken for the boost circuit are with 500-mA nominal input current and 6 serial LEDs. All curves taken for the SEPIC circuit are with 500-mA nominal input current and 3 serial LEDs. $T_A = -40^{\circ}\text{C}$ to 125°C , unless otherwise specified.

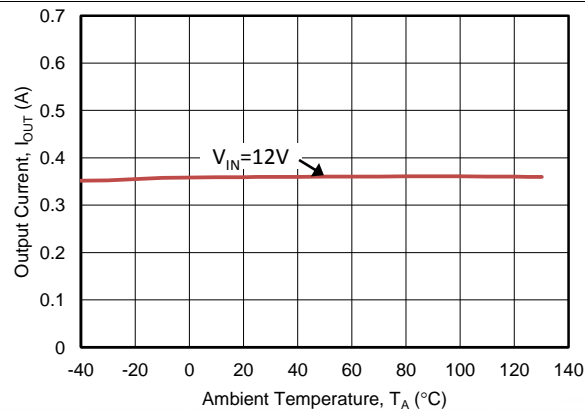


Figure 7. Output Current (BOOST) vs Temperature

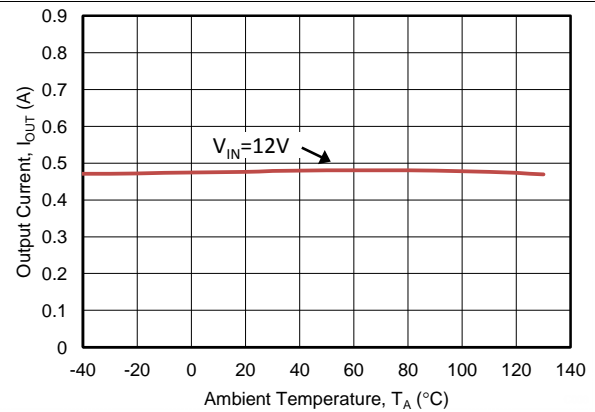


Figure 8. Output Current (SEPIC) vs Temperature

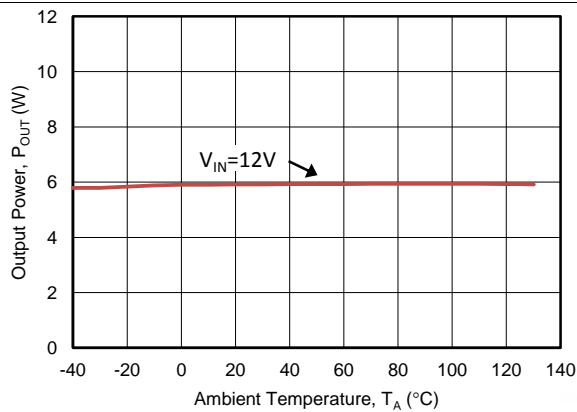


Figure 9. Output Power (BOOST) vs Temperature

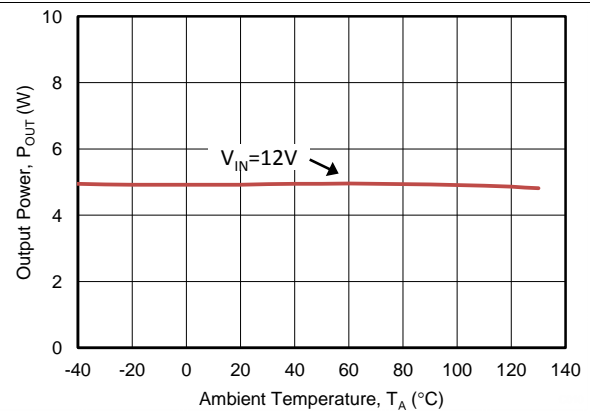


Figure 10. Output Power (SEPIC) vs Temperature

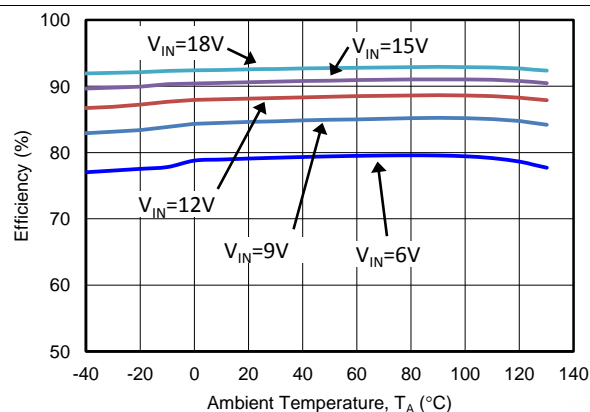


Figure 11. Efficiency (BOOST) vs Temperature

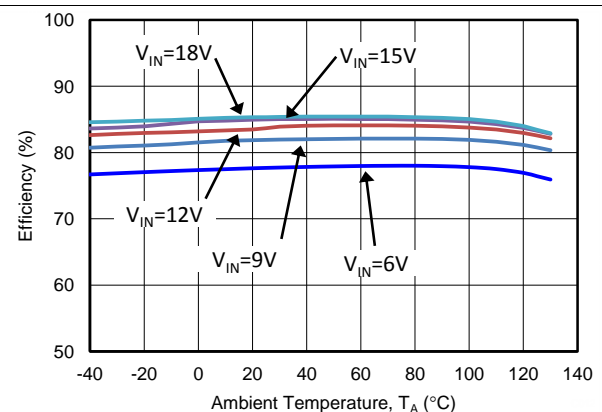


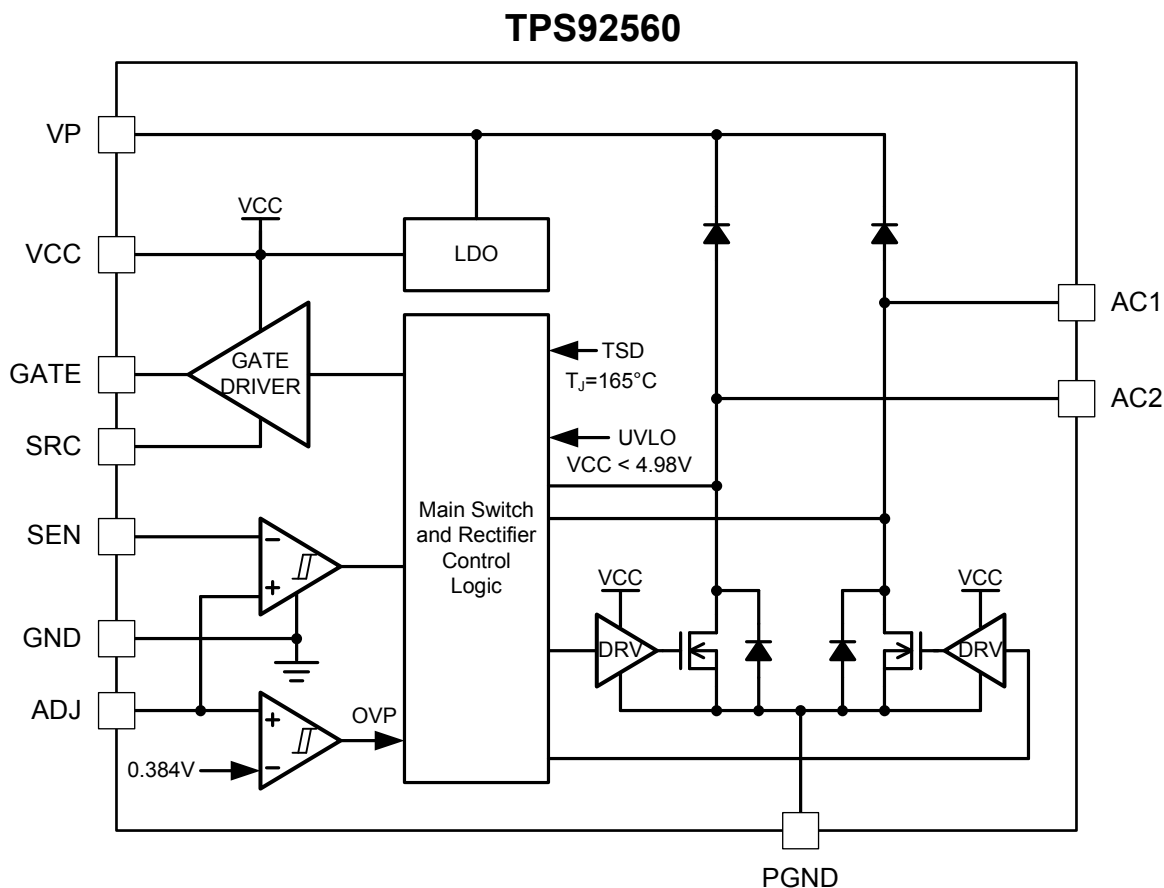
Figure 12. Efficiency (SEPIC) vs Temperature

7 Detailed Description

7.1 Overview

The TPS92560 is a simple hysteretic control switching LED driver for MR16 or AR111 lighting applications. The device accepts DC voltage, AC voltage and electronic transformer as an input power source. The compact application circuit can fit into a generic case of MR16 lamps easily. The hysteretic inductor current control scheme requires no small signal control loop compensation and maintains constant average input current to secure high compatibility to different kinds of input power source. The TPS92560 can be configured to either a step-up or step-up/down LED driver for the use of different number of LEDs. The patent pending current control mechanism allows the use of a single set of component and PCB layout for serving different output power requirements by changing the number of LEDs. The integrating of the active low-side input rectifiers reduces the power loss for voltage rectification and saves two external diodes of a generic bridge rectifier to aim for a simple end application circuit. When the driver is used with an AC voltage source or electronic transformer, the current regulation level increases accordingly to maintain an output current close to the level that when it is used with a DC voltage source. With the output overvoltage protection and over-temperature shutdown functions, the TPS92560 is specifically suitable for the applications that are space limited and need wide acceptance to different power sources.

7.2 Functional Block Diagram



SVA-30207403

7.3 Feature Description

7.3.1 VCC Regulator

The VCC pin is the output of the internal linear regulator for providing an 8.45V typical supply voltage to the MOSFET driver and internal circuits. The output current of the VCC pin is limited to 30mA typical. A low ESR ceramic capacitor of 0.47-μF or higher capacitance should be connected across the VCC and SRC pins to supply transient current to the MOSFET driver.

7.3.2 MOSFET Driver

The GATE pin is the output of the gate driver which referenced to the SRC pin. The gate driver is powered directly by the VCC regulator which the maximum gate driving current is limited to 30 mA (typical). To prevent hitting the VCC current limit, TI suggests using a low gate charge MOSFET when high switching frequency is needed.

7.3.3 ADJ Pin

The voltage on the ADJ pin determines the reference voltage for the input current regulation. Typically, the ADJ pin voltage is divided from the output voltage of the circuit by a voltage divider, thus the average input current is adjusted with respect to the number of LEDs used. The voltage of the ADJ pin determines the input current following the expression:

$$I_{IN(nom)} = \frac{V_{VP}}{R_{SEN}} \times \frac{R_{ADJ2}}{R_{ADJ1} + R_{ADJ2}} \quad (1)$$

7.3.3.1 Output OVP

In the TPS92560, a function of output overvoltage protection (OVP) is provided to prevent damaging the circuit due to an open circuit of the LED. The OVP function is implemented to the ADJ pin. When the voltage of the ADJ pin exceeds 0.384V typical, the OVP circuit disables the MOSFET driver and turns off the main switch to allow the output capacitor to discharge. As the voltage of the ADJ pin decreases to below 0.353 V (typical), the MOSFET driver is enabled and the TPS92560 returns to normal operation. The triggering threshold of the output voltage is determined by the value of the resistors R_{ADJ1} and R_{ADJ2} , which can be calculated using the following equation:

$$V_{VP} \times \frac{R_{ADJ2}}{R_{ADJ1} + R_{ADJ2}} \leq 0.384V \quad (2)$$

When defining the OVP threshold voltage, it is necessary to certain that the OVP threshold voltage does not exceed the rated voltage of the output rectifier and capacitor to avoid damaging of the circuit.

7.3.4 AC1 and AC2 Pins

The TPS92560 provides two internal active rectifiers for input voltage rectification. Each internal rectifier connects across the ACn pin to GND. These internal active rectifiers function as the low-side diode rectifiers of a generic bridge rectifier. The integrating of the active rectifiers helps in saving two external diodes of a bridge rectifier along with an improvement of power efficiency. For high power applications, for instance, 12-W output power, external diode rectifiers can be added across the ACn pin to GND to reduce heat dissipation on the TPS92560.

Feature Description (continued)

7.3.5 Detection of Power Source

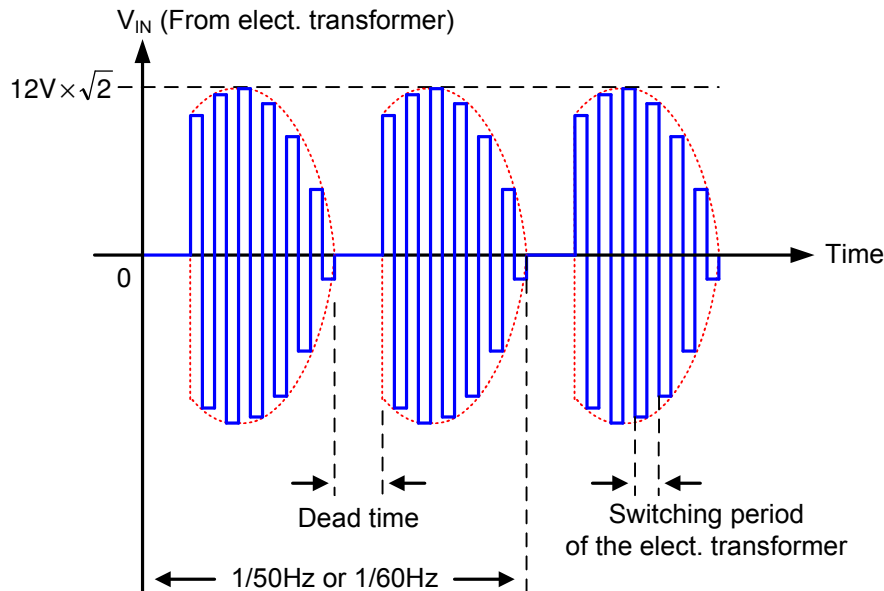


Figure 13. Inherent Dead Time of the Output Voltage of an Electronic Transformer

Both the voltages of a generic AC source (50/60Hz) and an electronic transformer carry certain amount of dead time inherently, as shown in [Figure 13](#). The existing of the dead time leads to a drop of the RMS input power to the driver circuit. In order to compensate the drop of the RMS input power, the ADJ pin sources current to the resistor, R_{ADJ2} to increase the reference voltage for the current regulation loop and in turn increase the RMS input power accordingly when an AC voltage source or electronic transformer is detected. The output current of the ADJ pin for an AC input voltage and electronic transformer are 9.5μA and 11.5μA typical respectively. Practically the amount of the power for compensating the dead time of the input power source differs case to case depending on the characteristics of the power source, the value of the R_{ADJ1} and R_{ADJ2} might need a fine adjustment in accordance to the characteristics of the power source. The additional output power for compensating the dead time of the power sources (ΔP_{LED}) are calculated using the following [Equation 3](#) and [Equation 4](#).

For 50/60Hz AC power source:

$$\Delta P_{LED-50/60\text{ Hz}} = V_{IN} \times \frac{R_{ADJ2} \times 9.5\text{ }\mu\text{A}}{R_{SEN}} \times \eta \quad (3)$$

For electronic transformer:

$$\Delta P_{LED-ELECT-XFR} = V_{IN} \times \frac{R_{ADJ2} \times 11.5\text{ }\mu\text{A}}{R_{SEN}} \times \eta \quad (4)$$

7.3.6 Current Regulation

In the TPS92560, the input current regulation is attained by limiting the peak and valley of the inductor current. Practically the inductor current sensing is facilitated by detecting the voltage on the resistor, R_{SEN} . Because the current flows through the R_{SEN} is a sum total of the currents of the main switch and LEDs, the voltage drop on the R_{SEN} reflects the current of the inductor that is identical to the input current to the LED driver circuit. [Figure 14](#) shows the waveform of the inductor current ripple with the peak and valley values controlled.

Feature Description (continued)

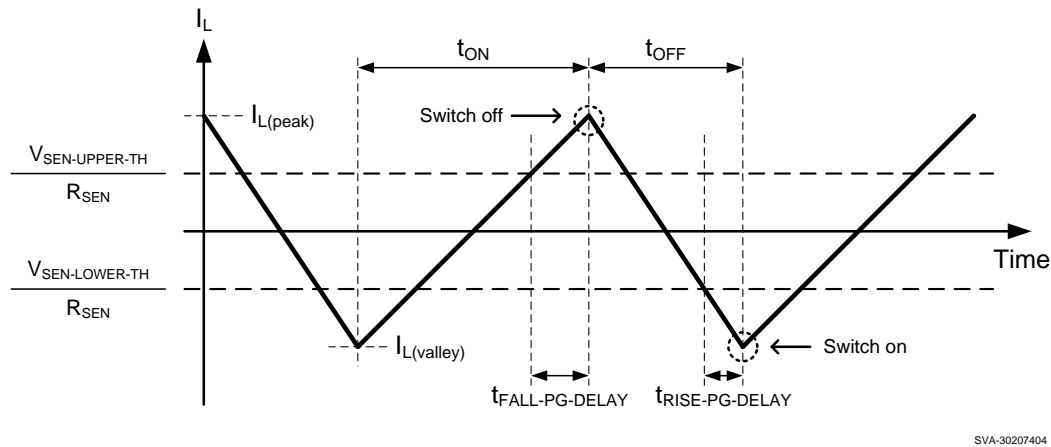


Figure 14. Inductor Current Ripple in Steady State

The voltage of the ADJ pin is determined by the forward voltage of the LED and divided from the V_{VP} by a resistor divider. The equation for calculating the V_{ADJ} as shown in [Equation 5](#).

$$V_{ADJ} = V_{VP} \times \frac{R_{ADJ2}}{R_{ADJ1} + R_{ADJ2}} \quad (5)$$

In steady state, the voltage drop on the R_{ADJ1} is identical to the forward voltage of the LED (V_{LED}) and the voltage across the R_{ADJ2} is identical to the voltage across the R_{SEN} . The LED current, I_{LED} is then calculated following the equations:

In steady state:

$$V_{LED} = V_{RADJ1} \quad (6)$$

$$V_{\text{SEN}} = V_{\text{RADJ2}} \quad (7)$$

$$I_{IN(nom)} = \frac{V_{SEN}}{R_{SEN}} \quad (8)$$

Since

$$P_{LED} = P_{IN} \times \eta \quad \text{where } \eta \text{ is the conversion efficiency} \quad (9)$$

Thus,

$$V_{LED} \times I_{LED} = V_{IN} \times I_{IN(nom)} \times \eta \quad (10)$$

Put the expressions (2) to (4) into (5):

$$I_{LED} = V_{IN} \times \frac{I_{ADJ2} \times R_{ADJ2}}{I_{ADJ1} \times R_{ADJ1} \times R_{SEN}} \times \eta \quad (11)$$

Due to the high input impedance of the ADJ pin, the current flows into the ADJ pin can be neglected and thus I_{RADJ1} equals I_{RADJ2} . The LED current is then calculated following the expressions below:

$$I_{LED} = V_{IN} \times \frac{R_{ADJ2}}{R_{ADJ1} \times R_{SEN}} \times \eta \quad (12)$$

Practically, the conversion efficiency of a boost circuit is almost a constant around 85%. Being assumed that the efficiency term in the I_{LED} expression is a constant, the LED current depends solely on the magnitude of the input voltage, V_{IN} . Without changing a component, the output power of the typical application circuits of the TPS92560 is adjustable by using different number of LEDs.

The output power is calculated by following the expression:

Feature Description (continued)

$$P_{LED} = V_{LED} \times V_{IN} \times \frac{R_{ADJ2}}{R_{ADJ1} \times R_{SEN}} \times \eta \quad (13)$$

7.3.7 Switching Frequency (Boost Configuration)

In the following sections, the equations and calculations are limited to the boost configuration only (that is, the LED forward voltage higher than the input voltage), unless otherwise specified. The application information for the SEPIC and other circuit topologies are available in separate application notes and reference designs. In the boost configuration, including the propagation delay of the control circuit, the ON and OFF times of the main switch are calculated using [Equation 14](#) and [Equation 15](#).

$$t_{ON} = \left\{ \frac{|V_{SEN-UPPER-TH}| \times L}{R_{SEN} \times [V_{IN} - V_D - I_{IN(nom)} \times (R_L + R_{DS(ON)} + R_{SEN} + R_{AC-FET})]} + t_{FALL-PG-DELAY} \right\} \times 2 \quad (14)$$

$$t_{OFF} = \left\{ \frac{|V_{SEN-LOWER-TH}| \times L}{R_{SEN} \times [V_{LED} - V_{IN} - 2V_D - I_{IN(nom)} \times (R_L + R_{SEN} + R_{AC-FET})]} + t_{RISE-PG-DELAY} \right\} \times 2 \quad (15)$$

In the previous equations, the V_D is the forward voltage of D_3 , R_L is the DC resistance of L_1 , $R_{DS(ON)}$ is the ON resistance of Q_1 and R_{AC-FET} is the turn ON resistance of the internal active rectifier with respect to the typical application circuit diagram.

Practically the resistance of the R_L , $R_{DS(on)}$ and R_{AC-FET} is in the order of several tenth of $m\Omega$, by assuming a 0.5-V diode forward voltage and the sum total of the R_L , $R_{DS(ON)}$ and R_{AC-FET} is close to 1 Ω , the on and off times of Q_1 can be approximated using the [Equation 16](#) and [Equation 17](#).

$$t_{ON} \approx \left\{ \frac{14.9mV \times L}{R_{SEN} \times [V_{IN} - 0.5V - I_{IN(nom)} \times (1 + R_{SEN})]} + 84ns \right\} \times 2 \quad (16)$$

$$t_{OFF} \approx \left\{ \frac{14.9mV \times L}{R_{SEN} \times [V_{LED} - V_{IN} - 1V - I_{IN(nom)} \times (1 + R_{SEN})]} + 68ns \right\} \times 2 \quad (17)$$

With the switching on and OF times determined, the switching frequency can be calculated using [Equation 18](#).

$$f_{sw} = \frac{1}{t_{ON} + t_{OFF}} \quad (18)$$

Because of the using of hysteretic control scheme, the switching frequency of the TPS92560 in steady state is dependent on the input voltage, output voltage and inductance of the inductor. Generally a 1-MHz to 1.5-MHz switching frequency is suggested for applications using an electronic transformer as the power source.

7.3.8 Inductor Selection (Boost Configuration)

Because of the using of the hysteretic control scheme, the switching frequency of the TPS92560 in a boost configuration can be adjusted in accordance to the value of the inductor being used. Derived from the equations (12) and (13), the value of the inductor can be determined base on the desired switching frequency by using [Equation 19](#).

$$L = \frac{\left(\frac{1}{f_{sw}} - 304ns \right) \times R_{SEN}}{\left(\frac{1}{V_{IN} - 0.5V - I_{IN(nom)} \times (1 + R_{SEN})} + \frac{1}{V_{LED} - V_{IN} - 1V - I_{IN(nom)} \times (1 + R_{SEN})} \right) \times 29.8mV} \quad (19)$$

When selecting the inductor, it is essential to ensure the peak inductor current does not exceed the the factory suggested saturation current of the inductor. The values of the peak and valley inductor current are calculated using the following equations:

Peak inductor current:

Feature Description (continued)

$$I_{L(\text{peak})} = \frac{[V_{\text{IN}} - V_D - I_{\text{IN}(\text{nom})} \times (R_L + R_{\text{DS(on)}} + R_{\text{SEN}} + R_{\text{AC-FET}})] \times t_{\text{ON}}}{2L} + I_{\text{IN}(\text{nom})} \quad (20)$$

Valley inductor current:

$$I_{L(\text{valley})} = I_{\text{IN}(\text{nom})} - \frac{[V_{\text{LED}} - V_{\text{IN}} - 2V_D - I_{\text{IN}(\text{nom})} \times (R_L + R_{\text{SEN}} + R_{\text{AC-FET}})] \times t_{\text{OFF}}}{2L} \quad (21)$$

Assume the total resistance of the R_L , $R_{\text{DS(on)}}$ and $R_{\text{AC-FET}}$ is $1\ \Omega$ and the diode drop, V_D equal to $1\ \text{V}$, the peak and valley currents of the inductor can be approximated using [Equation 22](#) and [Equation 23](#).

$$I_{L(\text{peak})} \approx \frac{[V_{\text{IN}} - 0.5\text{V} - I_{\text{IN}(\text{nom})} \times (1 + R_{\text{SEN}})] \times t_{\text{ON}}}{2L} + I_{\text{IN}(\text{nom})} \quad (22)$$

$$I_{L(\text{valley})} \approx I_{\text{IN}(\text{nom})} - \frac{[V_{\text{LED}} - V_{\text{IN}} - 1\text{V} - I_{\text{IN}(\text{nom})} \times (1 + R_{\text{SEN}})] \times t_{\text{OFF}}}{2L} \quad (23)$$

In order not to saturate the inductor, an inductor with a factory guaranteed saturation current (I_{SAT}) 20% higher than the $I_{L(\text{peak})}$ is suggested. Thus the I_{SAT} of the inductor should fulfill the following requirement:

$$I_{\text{SAT}} \geq I_{L(\text{peak})} \times 1.2 \quad (24)$$

7.3.9 Input Surge Voltage Protection

When use with an electronic transformer, the surge voltage across the input terminals can be sufficiently high to damage the TPS92560 depending on the characteristics of the electronic transformer. To against potential damaging due to the input surge voltage, a 36-V Zener diode can be connected across the input bridge rectifier as shown in [Figure 15](#).

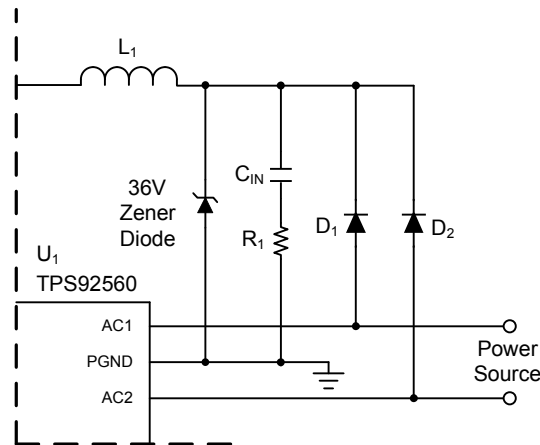


Figure 15. Input Surge Voltage Protection Using an External Zener Diode

7.4 Device Functional Modes

7.4.1 Thermal Shutdown

The TPS92560 includes a thermal shutdown circuitry that ceases the operation of the device to avoid permanent damage. The threshold for thermal shutdown is 165°C with a 30°C hysteresis typical. During thermal shutdown the VCC regulator is disabled and the MOSFET is turned off.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In the applications that need true regulation of the LED current, the intrinsic input current control loop can be changed to monitor the LED current by adding an external LED current sensing circuit. Figure 18 and Figure 23 show the example circuits for true LED current regulation in boost and SEPIC configurations respectively. In the circuits, the U_3 (TL431) maintains a constant 2.5-V voltage drop on the resistors, R_3 and R_7 . Because the U_2 (TL431) maintains a constant voltage drop on the R_3 , the power dissipation on the output current sensing resistor, R_7 can be minimized by setting a low voltage drop on the R_7 . Because the change of the current flowing through the R_7 reflects in the change of the cathode current of U_3 and eventually adjusts the ADJ pin voltage of the TPS92560, the LED current is regulated independent of the change of the input voltage.

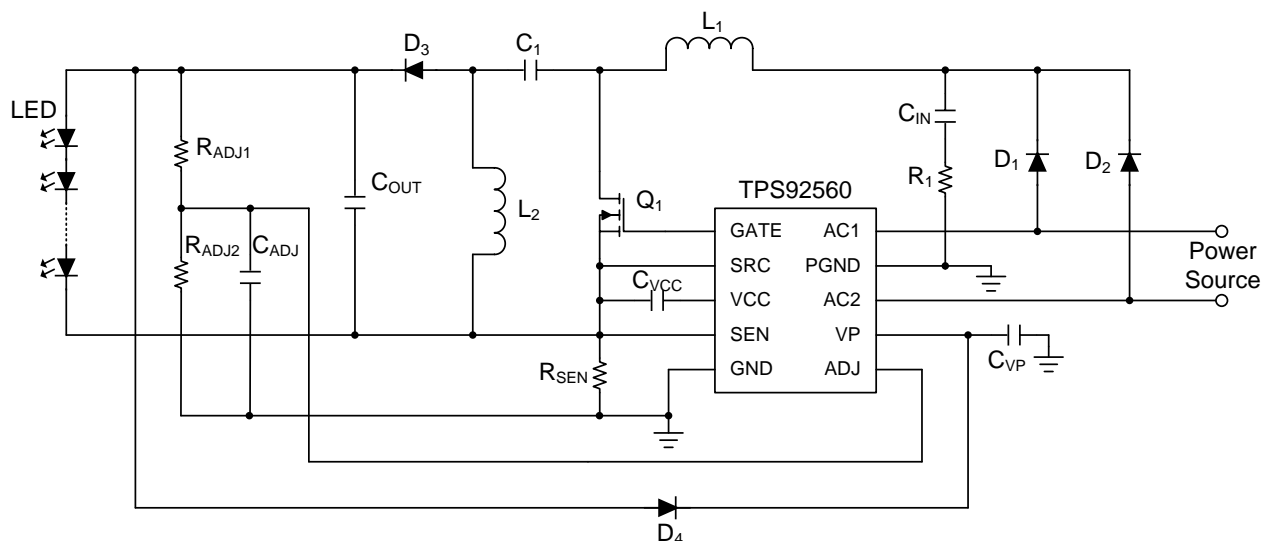


Figure 16. Typical Application Circuit of the TPS92560 Using SEPIC Configuration

Application Information (continued)

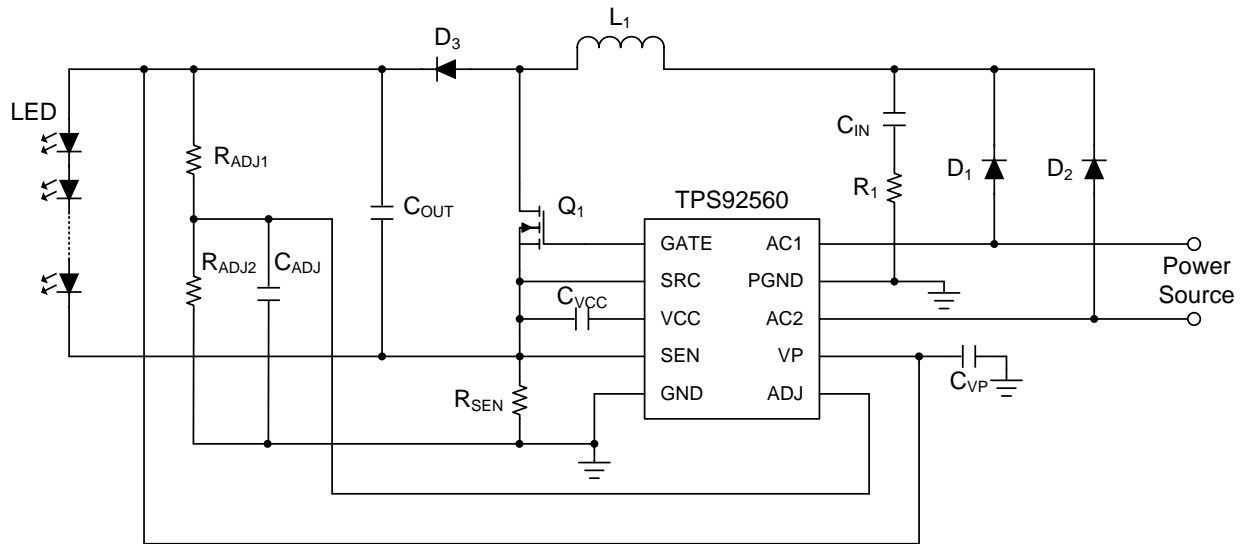


Figure 17. Typical Application Circuit of the TPS92560 Using Boost Configuration

8.2 Typical Applications

8.2.1 Boost Application Design Example

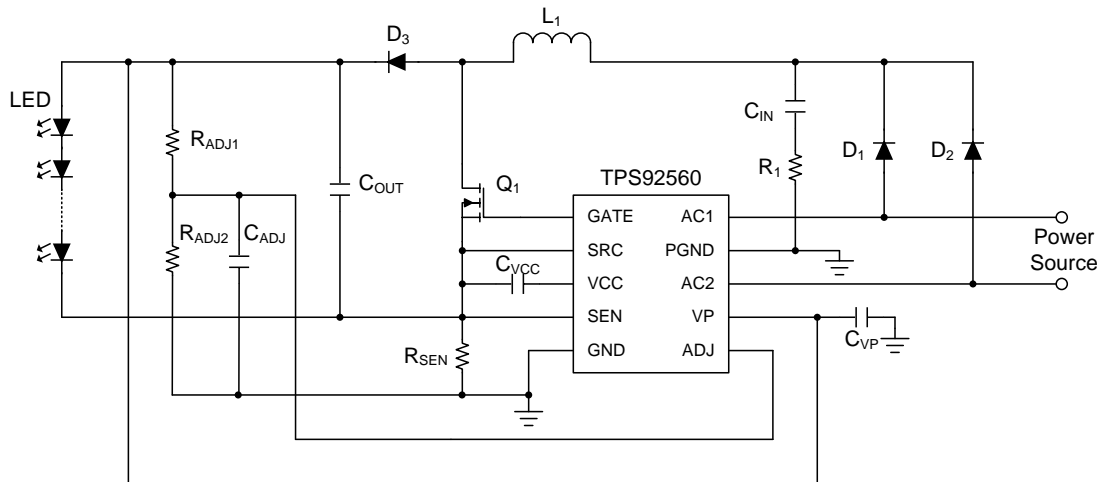


Figure 18. TPS92560 in Boost Configuration With Input Current Regulation

Typical Applications (continued)

8.2.1.1 Design Requirements

The specifications of the boost application circuit in [Figure 18](#) are as listed as follows:

- Input Voltage: $V_{IN} = 12\text{ V}$
- LED Stack Voltage: $V_{LED} = 21\text{ V}$
- Input Current: $I_{IN(nom)} = 500\text{ mA}$
- Input Power = 6 W
- overvoltage Level: $V_{VP(OVP)} = 40\text{ V}$
- Switching Frequency: $f_{SW} = 1.4\text{ MHz}$

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Calculate Values for the ADJ Resistors

First choose a value for R_{ADJ2} in the range of 1 k Ω and 10 k Ω . For this example $R_{ADJ2} = 1\text{ k}\Omega$ is chosen. Then calculate R_{ADJ1} for the desired OVP level using [Equation 25](#).

$$R_{ADJ1} = \frac{V_{VP(OVP)} - 0.384\text{V}}{\left(\frac{0.384}{R_{ADJ2}}\right)} = \frac{40\text{V} - 0.384\text{V}}{\left(\frac{0.384}{1\text{k}\Omega}\right)} = 103\text{k}\Omega \quad (25)$$

Choose the nearest standard resistor value of $R_{ADJ1} = 102\text{ k}\Omega$.

8.2.1.2.2 Calculate the Sense Voltage and Sense Resistor Value

Given the calculated ADJ resistor values the sense voltage (V_{SEN}) can be calculated using [Equation 26](#).

$$V_{SEN} = V_{ADJ} = R_{ADJ2} \times \frac{V_{LED}}{R_{ADJ1}} = 1\text{k}\Omega \times \frac{21\text{V}}{102\text{k}\Omega} = 206\text{mV} \quad (26)$$

Given a current sense voltage of 206 mV the current sense resistor value (R_{SEN}) can be calculated using [Equation 27](#).

$$R_{SEN} = \frac{V_{SEN}}{I_{IN(nom)}} = \frac{206\text{mV}}{500\text{mA}} = 0.412\Omega \quad (27)$$

The nearest standard value if 0.412 Ω so choose $R_{SEN} = 0.412\Omega$.

8.2.1.2.3 Calculate the Inductor Value

Given a desired switching frequency of 1.4 MHz the inductor value can be calculated using [Equation 28](#).

$$L = \frac{\left(\frac{1}{f_{SW}} - 304\text{ns}\right) \times R_{SEN}}{29.8\text{mV} \times \left(\frac{1}{V_{IN} - 0.5\text{V} - I_{IN(nom)} \times (1 + R_{SEN})} + \frac{1}{V_{LED} - V_{IN} - 1\text{V} - I_{IN(nom)} \times (1 + R_{SEN})}\right)} \quad (28)$$

$$L = \frac{\left(\frac{1}{1.4\text{MHz}} - 304\text{ns}\right) \times 0.412\Omega}{29.8\text{mV} \times \left(\frac{1}{12\text{V} - 0.5\text{V} - 500\text{mA} \times (1 + 0.412)} + \frac{1}{21\text{V} - 12\text{V} - 1\text{V} - 500\text{mA} \times (1 + 0.412)}\right)} = 24.7\mu\text{H} \quad (29)$$

Choose the closest standard inductor value of $L = 22\text{ }\mu\text{H}$.

Typical Applications (continued)

8.2.1.3 Application Curve

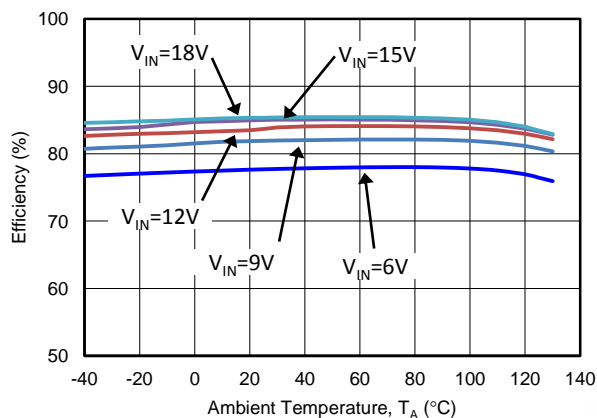
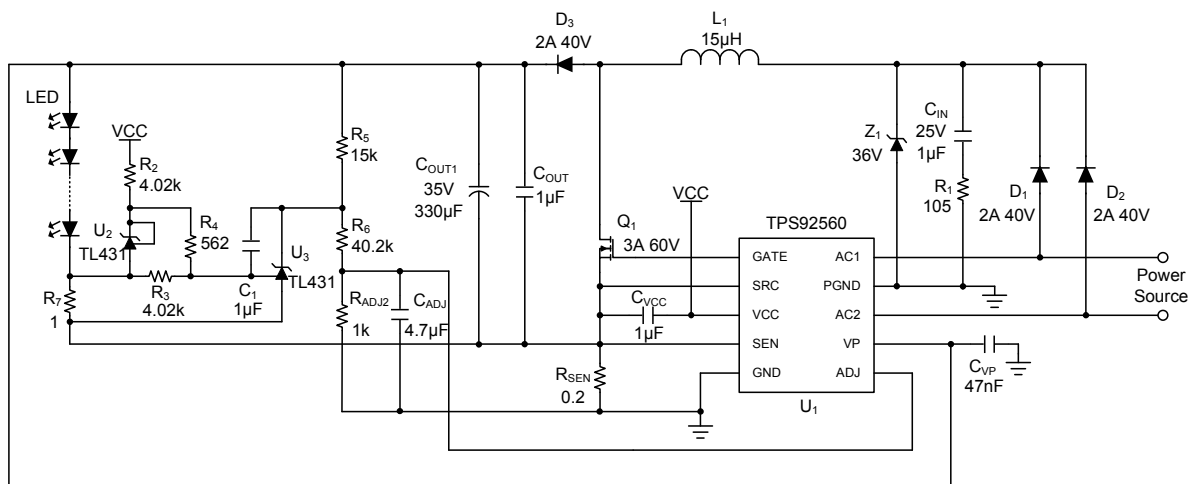


Figure 19. Efficiency

8.2.2 Boost Application Circuit With LED Current Regulation



Typical Applications (continued)

8.2.2.2 Application Curves

All curves taken at $V_{IN} = 3\text{ V to }18\text{ VDC}$ in boost configuration, with 300mA nominal output current, 6 serial LEDs. $T_A = 25^\circ\text{C}$.

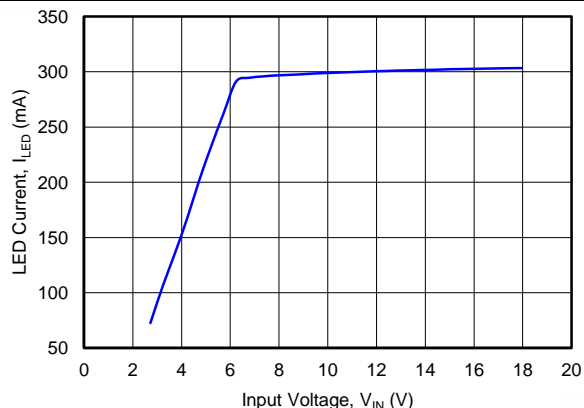


Figure 21. LED Current vs Input Voltage

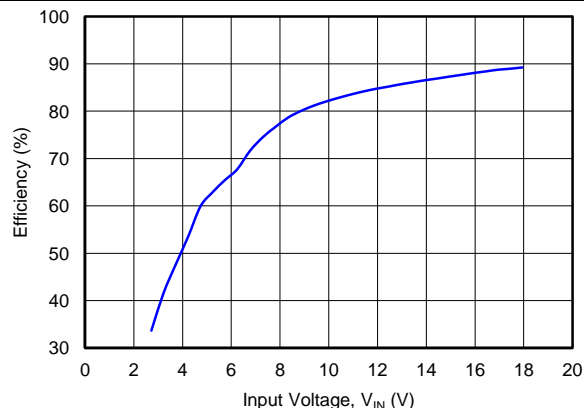


Figure 22. Efficiency vs Input Voltage

8.2.3 SEPIC Application Circuit With LED Current Regulation

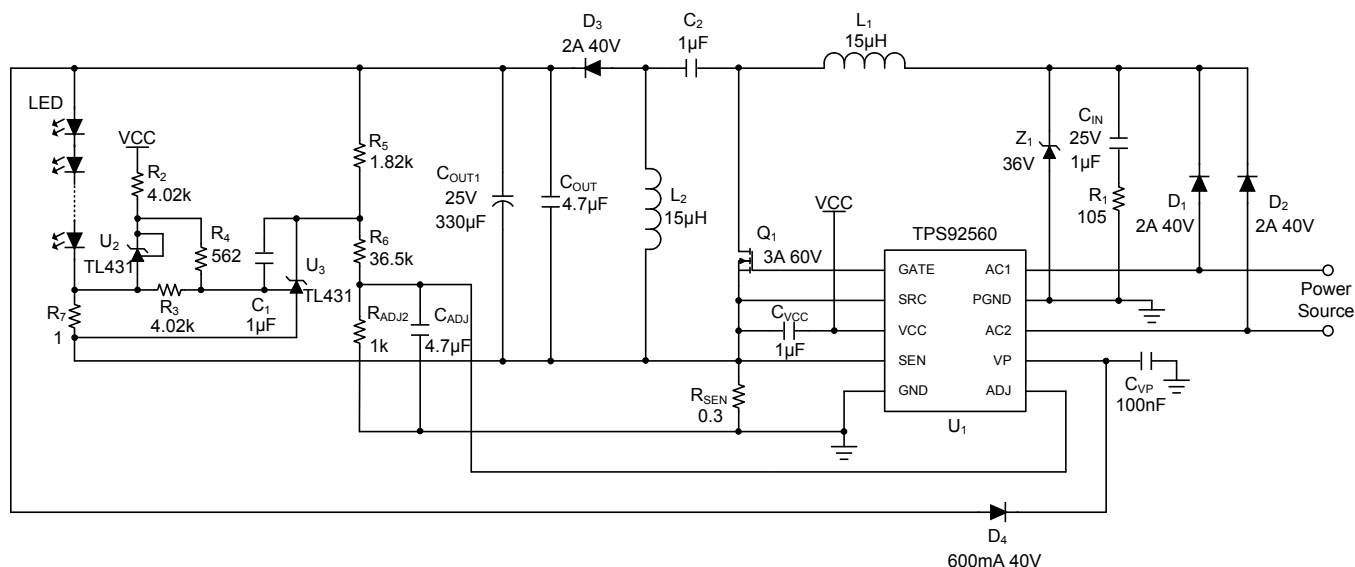


Figure 23. Using the TPS92560 in SEPIC Configuration With LED Current Regulation

8.2.3.1 Design Requirements

The specifications of the SEPIC application circuit in Figure 18 are as listed as follows:

- Objective input voltage: 3 VDC to 18 VDC / 12 VAC (50 Hz or 60 Hz) / Generic MR16 electronic transformer
- LED forward voltage: 13 VDC typical
- Output current: 300 mA typical (at 12-VDC input)
- Output power: 4 W typical (at 12-VDC input)

Typical Applications (continued)

8.2.3.2 Application Curves

All curves taken at $V_{IN} = 3\text{ V to }18\text{ VDC}$ in SEPIC configuration, with 300-mA nominal output current, 4 serial LEDs. $T_A = 25^\circ\text{C}$.

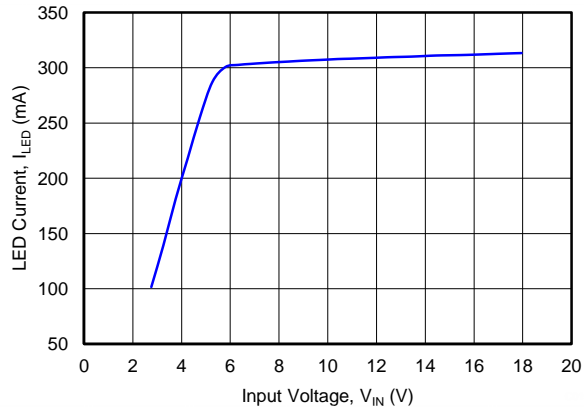


Figure 24. LED Current vs Input Voltage

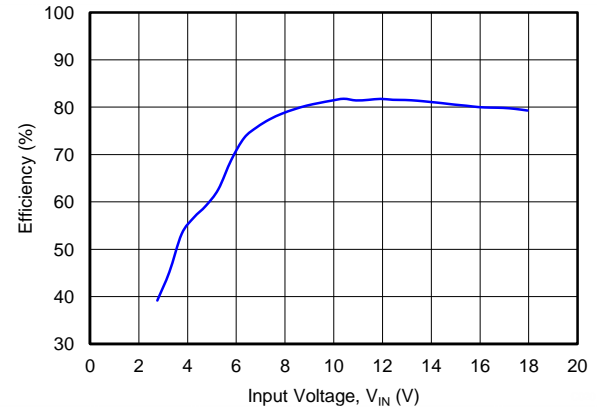


Figure 25. Efficiency vs Input Voltage

9 Power Supply Recommendations

Use any AC or DC power supply capable of the supply voltage required for the application and a power output capability greater than the total circuit input power.

10 Layout

10.1 Layout Guidelines

The VP input capacitor and ADJ resistors/capacitor should be placed as close to the IC as possible. The VCC capacitor should also be placed close to the device. Minimize the switching node area (connection between Q_1 , L_1 , and D_3) and keep the discontinuous current switching path as short as possible. This includes the loop formed by Q_1 , C_{OUT} , and the diode D_3 (designated by the red arrows). The ground connections for the TPS92560 and R_{SEN} should be tied closely together with a solid ground plane. The node connecting the SEN pin, SRC pin, the source of Q_1 , C_{VCC} , and C_{OUT} should be small with all components connected closely together.

10.2 Layout Example

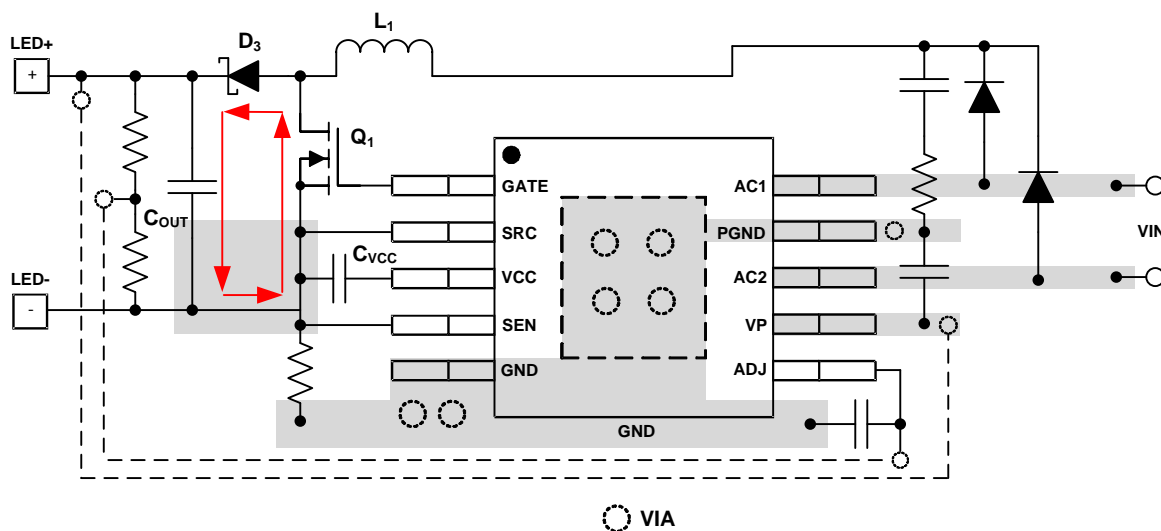


Figure 26. TPS92560 Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92560DGQ/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SN3B	Samples
TPS92560DGQR/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SN3B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92560DGQ/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS92560DGQR/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

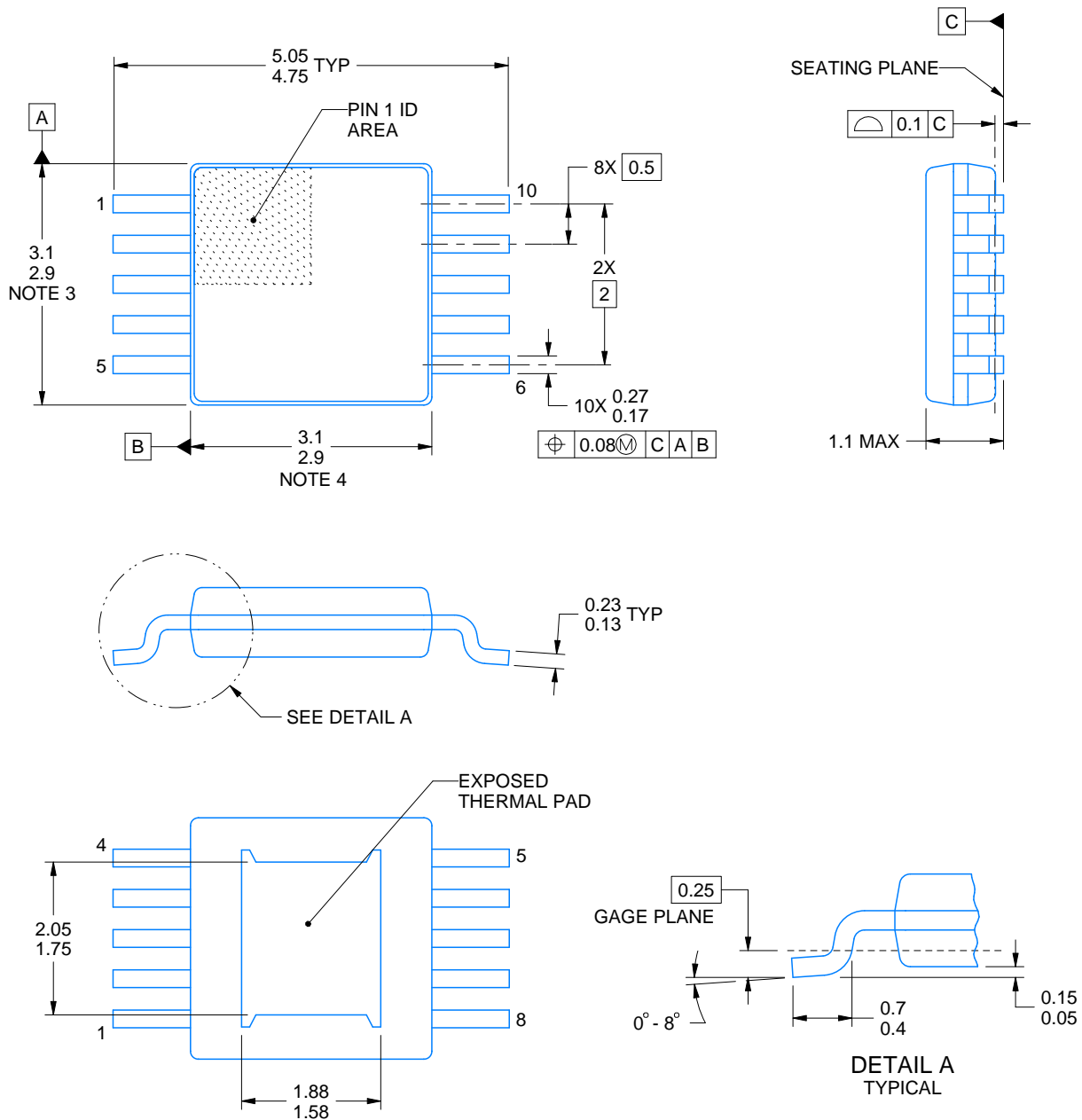
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92560DGQ/NOPB	HVSSOP	DGQ	10	1000	210.0	185.0	35.0
TPS92560DGQR/NOPB	HVSSOP	DGQ	10	3500	367.0	367.0	35.0

DGQ0010A

PACKAGE OUTLINE

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



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PowerPAD is a trademark of Texas Instruments.

NOTES:

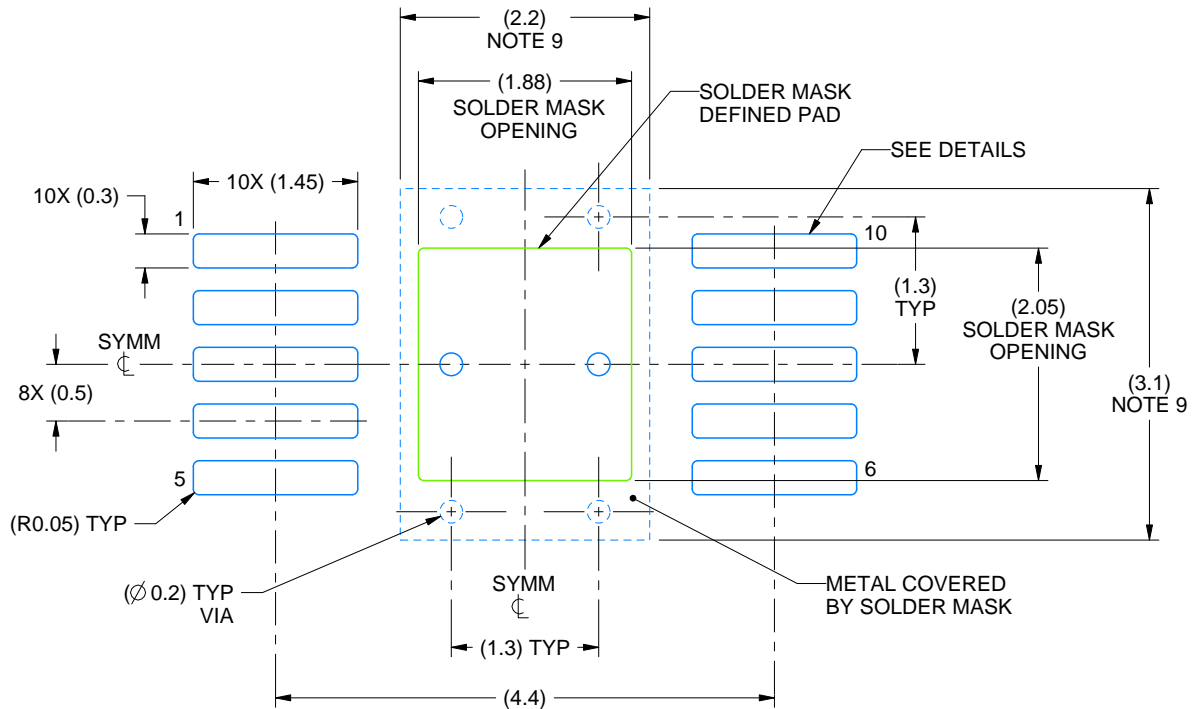
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.

EXAMPLE BOARD LAYOUT

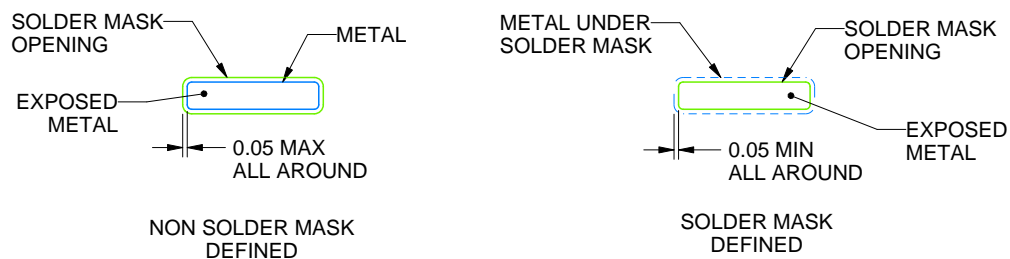
DGQ0010A

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

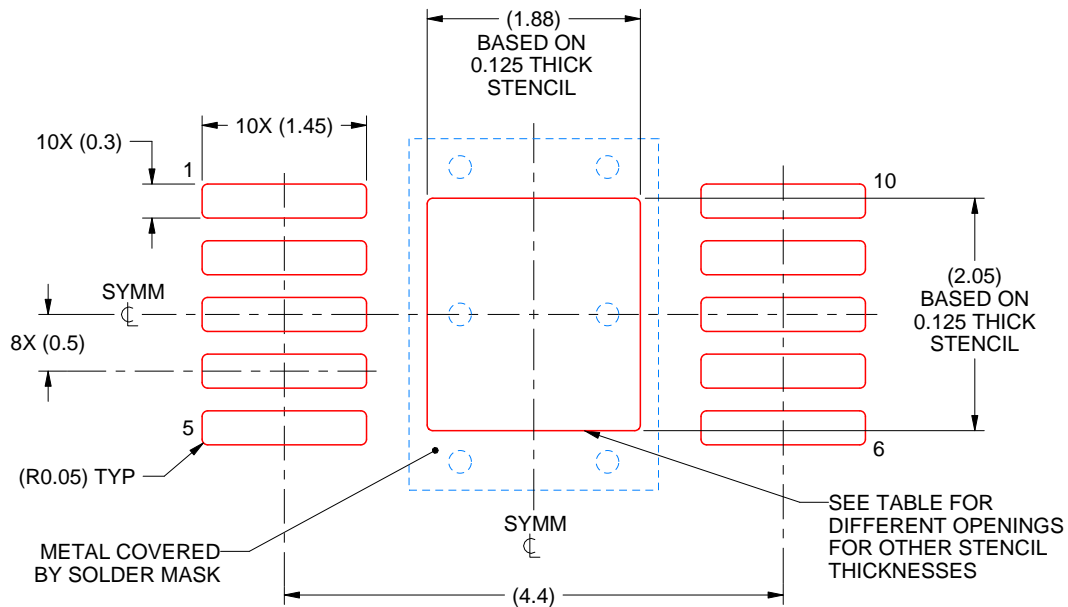
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGQ0010A

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.29
0.125	1.88 X 2.05 (SHOWN)
0.150	1.72 X 1.87
0.175	1.59 X 1.73

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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