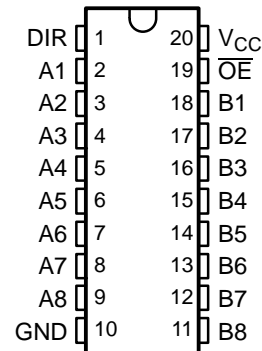


## FEATURES

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree <sup>(1)</sup>**
- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max  $t_{pd}$  of 6.3 ns at 3.3 V**
- **Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

PW PACKAGE  
(TOP VIEW)



- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## DESCRIPTION/ORDERING INFORMATION

This octal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – PW Reel of 2000	SN74LVC245AIPWREP	C245AEP

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	–0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	–0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	–50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>		83	°C/W
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT	
		MIN	MAX	MIN	MAX		
$V_{CC}$	Supply voltage	Operating	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$	V	
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.7		1.7		
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	2		2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$		$0.35 \times V_{CC}$	$0.35 \times V_{CC}$	V	
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$		0.7	0.7		
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$		0.8	0.8		
$V_I$	Input voltage	0	5.5	0	5.5	V	
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V	
$I_{OH}$	High-level output current	$V_{CC} = 1.65\text{ V}$		–4	–4	mA	
		$V_{CC} = 2.3\text{ V}$		–8	–8		
		$V_{CC} = 2.7\text{ V}$		–12	–12		
		$V_{CC} = 3\text{ V}$		–24	–24		
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$		4	4	mA	
		$V_{CC} = 2.3\text{ V}$		8	8		
		$V_{CC} = 2.7\text{ V}$		12	12		
		$V_{CC} = 3\text{ V}$		24	24		
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V	

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LVC245A-EP

## OCTAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

SCAS741B–DECEMBER 2003–REVISED AUGUST 2005

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			–40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 3.6 V	V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2		V
	I <sub>OH</sub> = –4 mA	1.65 V	1.29			1.2		
	I <sub>OH</sub> = –8 mA	2.3 V	1.9			1.7		
	I <sub>OH</sub> = –12 mA	2.7 V	2.2			2.2		
		3 V	2.4			2.4		
I <sub>OH</sub> = –24 mA	3 V	2.3			2.2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V				0.1	0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V				0.24	0.45	
	I <sub>OL</sub> = 8 mA	2.3 V				0.3	0.7	
	I <sub>OL</sub> = 12 mA	2.7 V				0.4	0.4	
	I <sub>OL</sub> = 24 mA	3 V				0.55	0.55	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±1	±5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±1	±10	μA
I <sub>OZ</sub> <sup>(1)</sup>		V <sub>O</sub> = 0 to 5.5 V	3.6 V			±1	±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	3.6 V			1	10	μA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>					1	10	
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	500	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			4		pF
C <sub>io</sub>	A or B port	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			5.5		pF

(1) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

(2) This applies in the disabled state only.

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

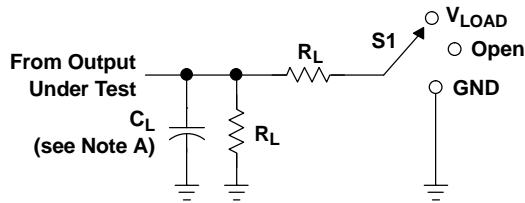
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			–40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	1.8 V ± 0.15 V	1	6	12.2	1	12.7	ns
			2.5 V ± 0.2 V	1	3.9	7.8	1	8.3	
			2.7 V	1	4.2	7.1	1	7.3	
			3.3 V ± 0.3 V	1.5	3.8	6.1	1.5	6.3	
t <sub>en</sub>	OE	A or B	1.8 V ± 0.15 V	1	7	14.8	1	15.3	ns
			2.5 V ± 0.2 V	1	4.5	10	1	10.5	
			2.7 V	1	5.4	9.3	1	9.5	
			3.3 V ± 0.3 V	1.5	4.4	8.3	1.5	8.5	
t <sub>dis</sub>	OE	A or B	1.8 V ± 0.15 V	1	7.8	16.5	1	17	ns
			2.5 V ± 0.2 V	1	4	9	1	9.5	
			2.7 V	1	4.4	8.3	1	8.5	
			3.3 V ± 0.3 V	1.7	4.1	7.3	1.7	7.5	
t <sub>sk(o)</sub>			3.3 V ± 0.3 V				1	ns	

**Operating Characteristics**

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	f = 10 MHz	Outputs enabled		pF
			1.8 V	42	
			2.5 V	43	
			3.3 V	45	
			Outputs disabled		
			1.8 V	1	
2.5 V	1				
			3.3 V	2	

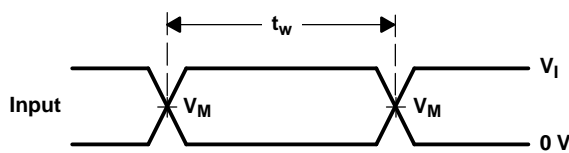
**PARAMETER MEASUREMENT INFORMATION**



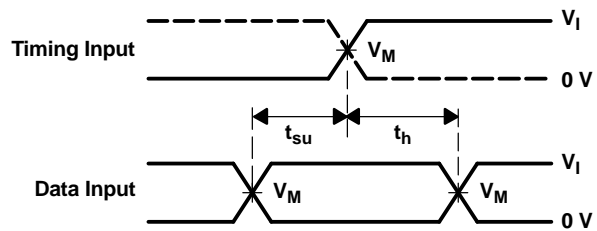
**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

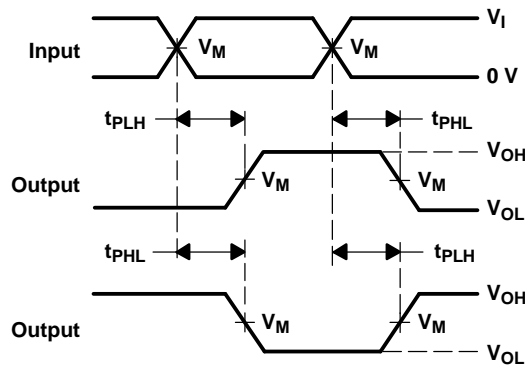
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



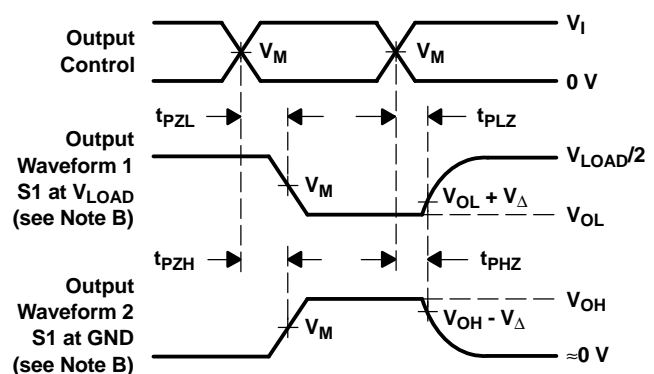
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVLC245AIPWREP	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C245AEP	<a href="#">Samples</a>
V62/04737-01XE	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C245AEP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC245A-EP :**

- Catalog: [SN74LVC245A](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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