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<ul> <li>Members of the Texas Instruments Widebus<sup>™</sup> Family</li> </ul>	SN54ABT16952 WD PACKAGE SN74ABT16952 DGG OR DL PACKAGE (TOP VIEW)	
<ul> <li>State-of-the-Art <i>EPIC</i>-II<i>B</i><sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation</li> </ul>		
<ul> <li>Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17</li> </ul>	1CLKAB 2 55 1CLKBA 1CLKENAB 3 54 1CLKENBA	
<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce) &lt; 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C</li> </ul>	GND	
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise</li> </ul>	1A2 0 6 51 0 1B2 V <sub>CC</sub> 0 7 50 V <sub>CC</sub>	
<ul> <li>Flow-Through Architecture Optimizes PCB Layout</li> </ul>	1A3 [] 8 49 [] 1B3 1A4 [] 9 48 [] 1B4	
<ul> <li>High-Drive Outputs (–32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)</li> </ul>	1A5 [] 10 47 [] 1B5 GND [] 11 46 [] GND	
<ul> <li>Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink</li> </ul>	1A6 [] 12 45 [] 1B6 1A7 [] 13 44 [] 1B7	
Small-Outline (DGG) Packages and 380-mil	1A8 🛛 14 43 🗍 1B8	
Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings	2A1 0 15 42 0 2B1 2A2 0 16 41 0 2B2	
	2A3 🛛 17 40 🗍 2B3	
description		
The 'ABT16952 are 16-bit registered transceivers that contain two sets of D-type flip-flops for temporary storage of data flowing in either	2A4 [] 19 38 [] 2B4 2A5 [] 20 37 [] 2B5 2A6 [] 21 36 [] 2B6	

that contain two sets of D-type flip-flops for temporary storage of data flowing in either direction. The 'ABT16952 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

lock (CLKAB or	GND 🛿 25	32 GND							
he clock-enable	2CLKENAB	31 2CLKENBA							
is low. Taking the	2CLKAB	30 2CLKBA							
BA) input low	2 <mark>0EAB</mark> 28	29 20EBA							
t.									
ate during power up or power down, $\overline{OE}$ should be tied to $V_CC$ through a pullup									

V<sub>CC</sub> 22 2A7 23

2A8 🛛 24

35 V<sub>CC</sub>

34 2B7

33 🛛 2B8

To ensure the high-impedance state during power up or power down, OE should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16952 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16952 is characterized for operation from –40°C to 85°C.



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# SN54ABT16952, SN74ABT16952 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS082C - FEBRUARY 1991 - REVISED JANUARY 1997

#### FUNCTION TABLE<sup>†</sup>

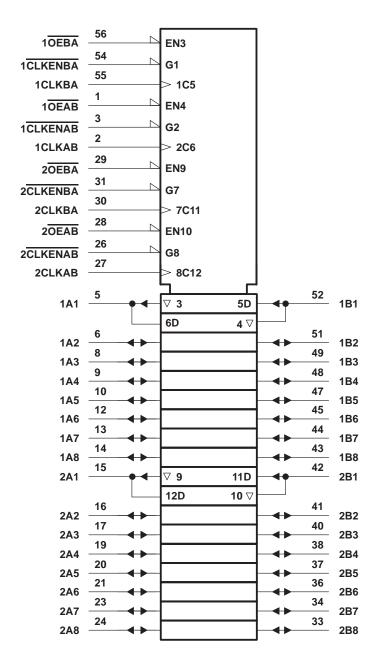
	OUTPUT									
CLKENAB	CLKAB	OEAB	Α	В						
н	Х	L	Х	в <sub>0</sub> ‡ в <sub>0</sub> ‡						
Х	L	L	Х	в <sub>0</sub> ‡						
L	$\uparrow$	L	L	L						
L	$\uparrow$	L	Н	н						
Х	Х	Н	Х	Z						

<sup>†</sup> A-to-B data flow is shown; B-to-A data flow is similar, but uses CLKENBA, CLKBA, and OEBA.

‡Level of B before the indicated steady-state input conditions were established



logic symbol<sup>†</sup>

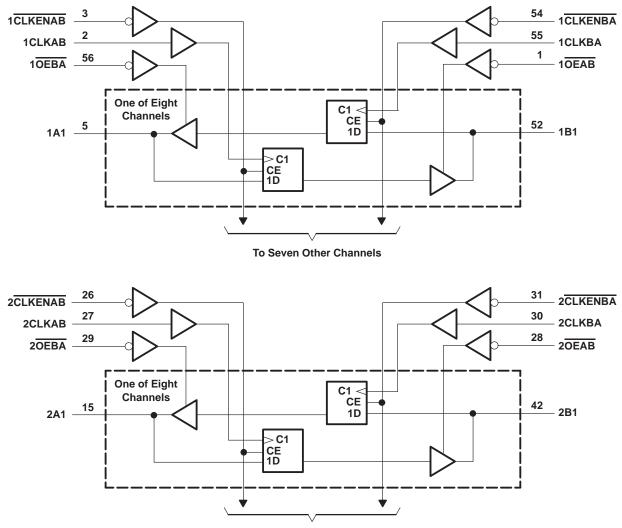


<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



## SN54ABT16952, SN74ABT16952 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS082C - FEBRUARY 1991 - REVISED JANUARY 1997

logic diagram (positive logic)



To Seven Other Channels



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub> Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1) Voltage range applied to any output in the high or power-off state, V <sub>O</sub> Current into any output in the low state, I <sub>O</sub> : SN54ABT16952	
SN74ABT16952	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	81°C/W
DL package	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

#### recommended operating conditions (see Note 3)

			SN54ABT	16952	SN74AB1	16952	UNIT
			MIN	MAX	MIN	MAX	
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2	EW	2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0 0	Vcc	0	VCC	V
ЮН	High-level output current		C,	-24		-32	mA
I <sub>OL</sub>	Low-level output current		202	48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	4	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.



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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			Т	A = 25°C	;	SN54AB	T16952	SN74AB1			
PA	RAMETER	TEST COI	NDITIONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
VIK		V <sub>CC</sub> = 4.5 V,	lj = -18 mA			-1.2		-1.2		-1.2	V
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA	2.5			2.5		2.5		
Vari		$V_{CC} = 5 V,$	I <sub>OH</sub> = -3 mA	3			3		3		V
∨он		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA	2			2				v
		VCC = 4.5 V	I <sub>OH</sub> = -32 mA	2*					2		
VOL		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA			0.55		0.55			V
VOL		VCC = 4.5 V	I <sub>OL</sub> = 64 mA			0.55*				0.55	v
V <sub>hys</sub>					100			2			mV
ŧ	Control inputs	V <sub>CC</sub> = 5.5 V,	$V_{I} = V_{CC} \text{ or } GND$			±1		L/±1		±1	μA
Ч	A or B ports	VCC = 5.5 V,				±100		<u>/</u> ±100		±100	μΑ
IOZH‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50	4	50		50	μΑ
Iozl‡		V <sub>CC</sub> = 5.5 V,	$V_{O} = 0.5 V$			-50	5	-50		-50	μΑ
loff		$V_{CC} = 0,$	$V_I$ or $V_O \leq 4.5~V$			±100	00			±100	μΑ
ICEX		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50	PP	50		50	μΑ
١٥	_	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V	-50	-100	-200	-50	-200	-50	-200	mA
		V <sub>CC</sub> = 5.5 V,	Outputs high			2		2		2	
ICC	A or B ports	$I_{O} = 0,$	Outputs low			35		35		35	mA
		$V_I = V_{CC}$ or GND	Outputs disabled			2		2		2	
∆ICC¶		$V_{CC} = 5.5 V$ , One is Other inputs at $V_{CC}$				0.5		0.5		0.5	mA
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			3						pF
Cio	A or B ports	$V_{O} = 2.5 \text{ V or } 0.5 \text{ V}$	/		8.5						pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V.

<sup>‡</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $\P$  This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



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#### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				= 5 V, 25°C	SN54AB	T16952	SN74AB1	16952	UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency	0	150	0	150	0	150	MHz		
tw†	Pulse duration, CLKAB or CLKBA high or low				3.3	25	3.3		ns	
	Setup time,	A or B	3.5		3.5		3.5			
t <sub>su</sub>	before CLKAB↑ or CLKBA↑	CLKENAB or CLKENBA	3		3		3		ns	
+.	Hold time,	A or B	1		01		1		20	
th	after CLKAB↑ or CLKBA↑	CLKENAB or CLKENBA	1		<b>2</b> 1		1		ns	

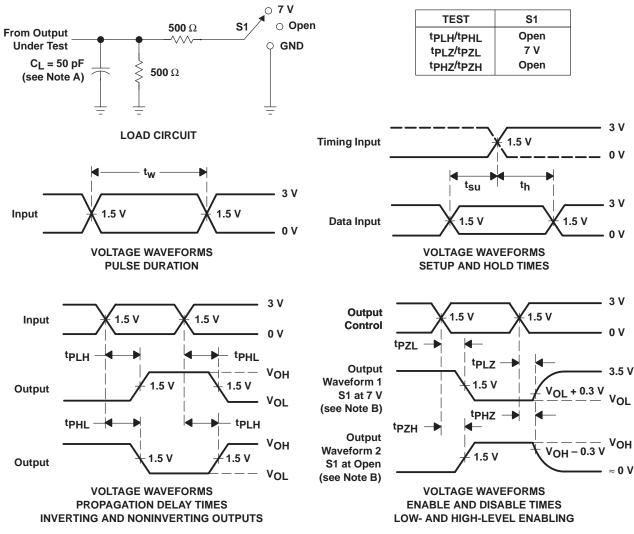
<sup>†</sup> This parameter is warranted, but not production tested.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16952		SN74ABT16952		UNIT
		(001-01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150			150	M	150		MHz
<sup>t</sup> PLH	CLK	A or B	1	2.6	3.9	1	\$4.4	1	4.3	ns
<sup>t</sup> PHL	OLK		1	2.6	4.2	1	4.6	1	4.5	115
<sup>t</sup> PZH	OE	A or P	1	2.5	3.8	1	4.7	1	4.6	
<sup>t</sup> PZL	ÛE	A or B	1	2.8	5.1	$\gamma_{c}$	6.1	1	6	ns
<sup>t</sup> PHZ	OE	A or P	1.7	3.4	4.7	01.7	6.1	1.7	5.5	
<sup>t</sup> PLZ	UE	A or B	1.3	3	3.9	<b>Q</b> 1.3	4.8	1.3	4.2	ns



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### PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>Q</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns. t<sub>f</sub>  $\leq$  2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



TEXAS NSTRUMENTS

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ABT16952DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABT16952DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16952DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16952DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16952DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16952DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16952DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16952DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT16952DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1



# PACKAGE MATERIALS INFORMATION

11-Mar-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16952DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ABT16952DLR	SSOP	DL	56	1000	346.0	346.0	49.0

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