- **Members of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- **_EPIC_™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

SN54ACT16244 . . . WD PACKAGE
74ACT16244 . . . DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	48	2$\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4$\overline{OE}$	24	25	3$\overline{OE}$
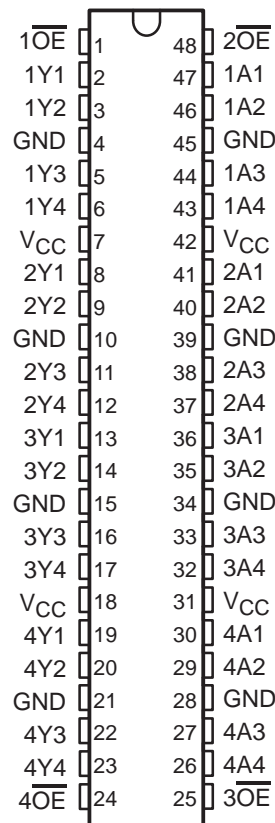
description

The SN54ACT16244 and 74ACT16244 are 16-bit buffers/line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. They can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide true outputs and symmetrical $\overline{OE}$ (active-low) output-enable inputs.

The 74ACT16244 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ACT16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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TEXAS INSTRUMENTS

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logic symbol†

Pin	Input			Output	Pin
1	1OE̅ → EN1				
48	2OE̅ → EN2				
25	3OE̅ → EN3				
24	4OE̅ → EN4				

47	1A1	1 1▽	1Y1	2
46	1A2		1Y2	3
44	1A3		1Y3	5
43	1A4		1Y4	6
41	2A1	1 2▽	2Y1	8
40	2A2		2Y2	9
38	2A3		2Y3	11
37	2A4		2Y4	12
36	3A1	1 3▽	3Y1	13
35	3A2		3Y2	14
33	3A3		3Y3	16
32	3A4		3Y4	17
30	4A1	1 4▽	4Y1	19
29	4A2		4Y2	20
27	4A3		4Y3	22
26	4A4		4Y4	23

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
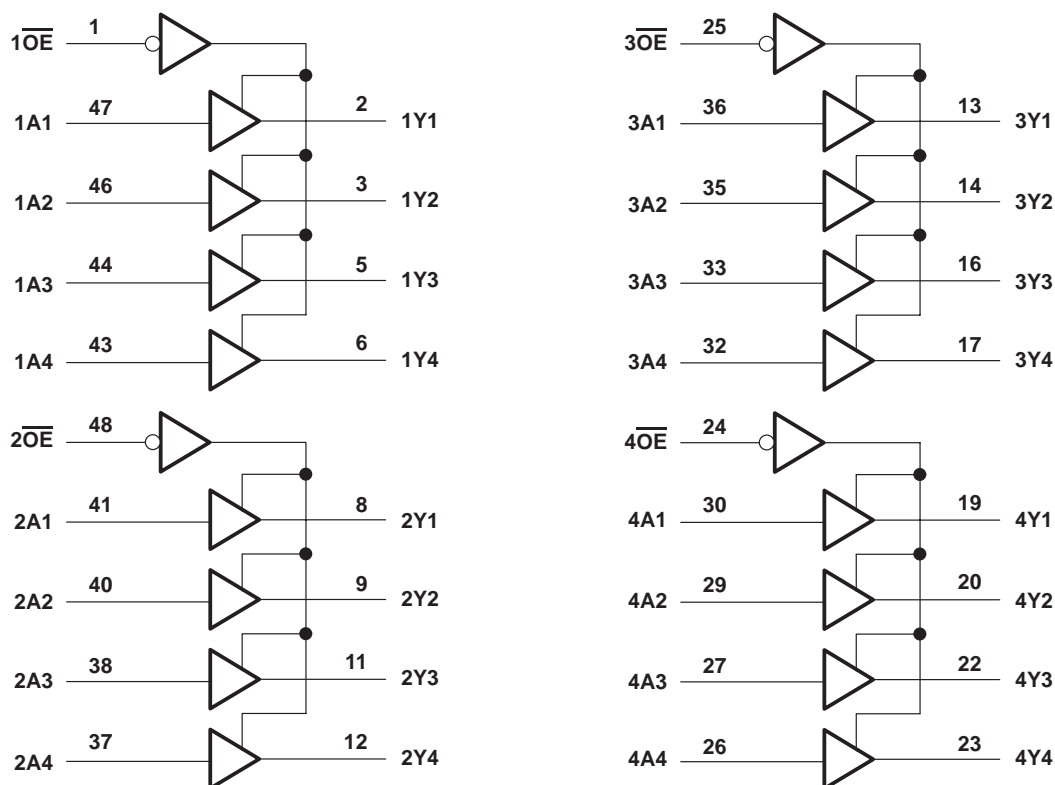
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V

Input voltage range, V_I (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V

Output voltage range, V_O (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . ±20 mA

Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . ±50 mA

Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±50 mA

Continuous current through V_{CC} or GND . . . . ±400 mA

Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package . . . . 0.85 W

DL package . . . . 1.2 W

Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		SN54ACT16244		74ACT16244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 4)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 3. Unused inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater to prevent them from floating.
4. All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54ACT16244		74ACT16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = −50\ \mu A$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = −24$ mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = −50$ mA†	5.5 V				3.85				
	$I_{OH} = −75$ mA†	5.5 V						3.85		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24$ mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50$ mA†	5.5 V					1.65			
	$I_{OL} = 75$ mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		13.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT16244					UNIT
			T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	4	6.5	8.5	3	10.3	ns
t_{PHL}			3.4	6.3	8.7	3.4	10.1	
t_{PZH}	$\overline{OE}$	Y	3	5.8	8.1	3	10.5	ns
t_{PZL}			3.7	6.7	9.3	3.7	11	
t_{PHZ}	$\overline{OE}$	Y	5.4	8.1	11.5	5.4	13	ns
t_{PLZ}			5	7.5	9.5	5	10.9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	74ACT16244					UNIT
			T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	4	6.5	8.5	4	9.4	ns
t_{PHL}			3.4	6.3	8.7	3.4	9.5	
t_{PZH}	$\overline{OE}$	Y	3	5.8	8.1	3	8.9	ns
t_{PZL}			3.7	6.7	9.3	3.7	10.3	
t_{PHZ}	$\overline{OE}$	Y	5.4	8.1	10.3	5.4	11.3	ns
t_{PLZ}			5	7.5	9.5	5	10.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 1 MHz	39	pF
	Outputs disabled			11	

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS
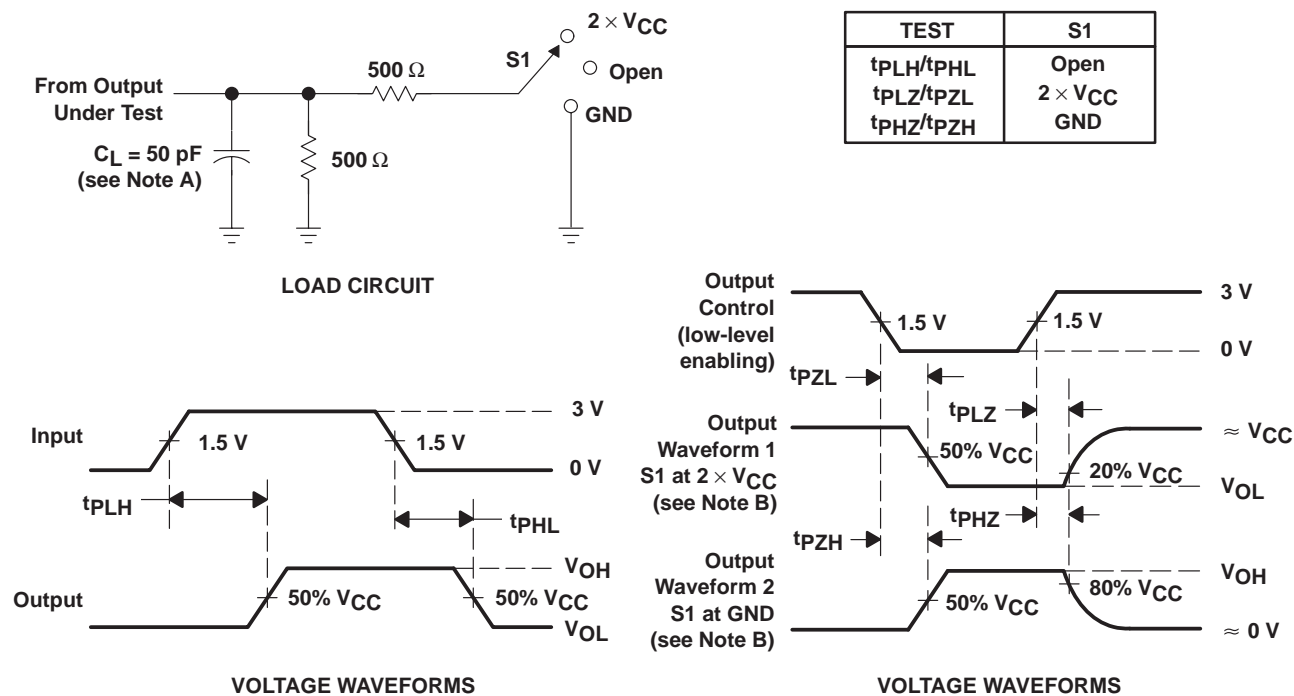
NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
          Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
      D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9202201MXA	ACTIVE	CFP	WD	48	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-9202201MX A SNJ54ACT16244W D	Samples
74ACT16244DGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		ACT16244	Samples
74ACT16244DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244	Samples
74ACT16244DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244	Samples
74ACT16244DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244	Samples
74ACT16244DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244	Samples
74ACT16244DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244	Samples
74ACT16244DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244	Samples
SNJ54ACT16244WD	ACTIVE	CFP	WD	48	1	TBD	SNPB	N / A for Pkg Type		5962-9202201MX A SNJ54ACT16244W D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74ACT16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16244DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
74ACT16244DLR	SSOP	DL	48	1000	367.0	367.0	55.0

DL (R−PDSO−G48)   PLASTIC SMALL−OUTLINE PACKAGE
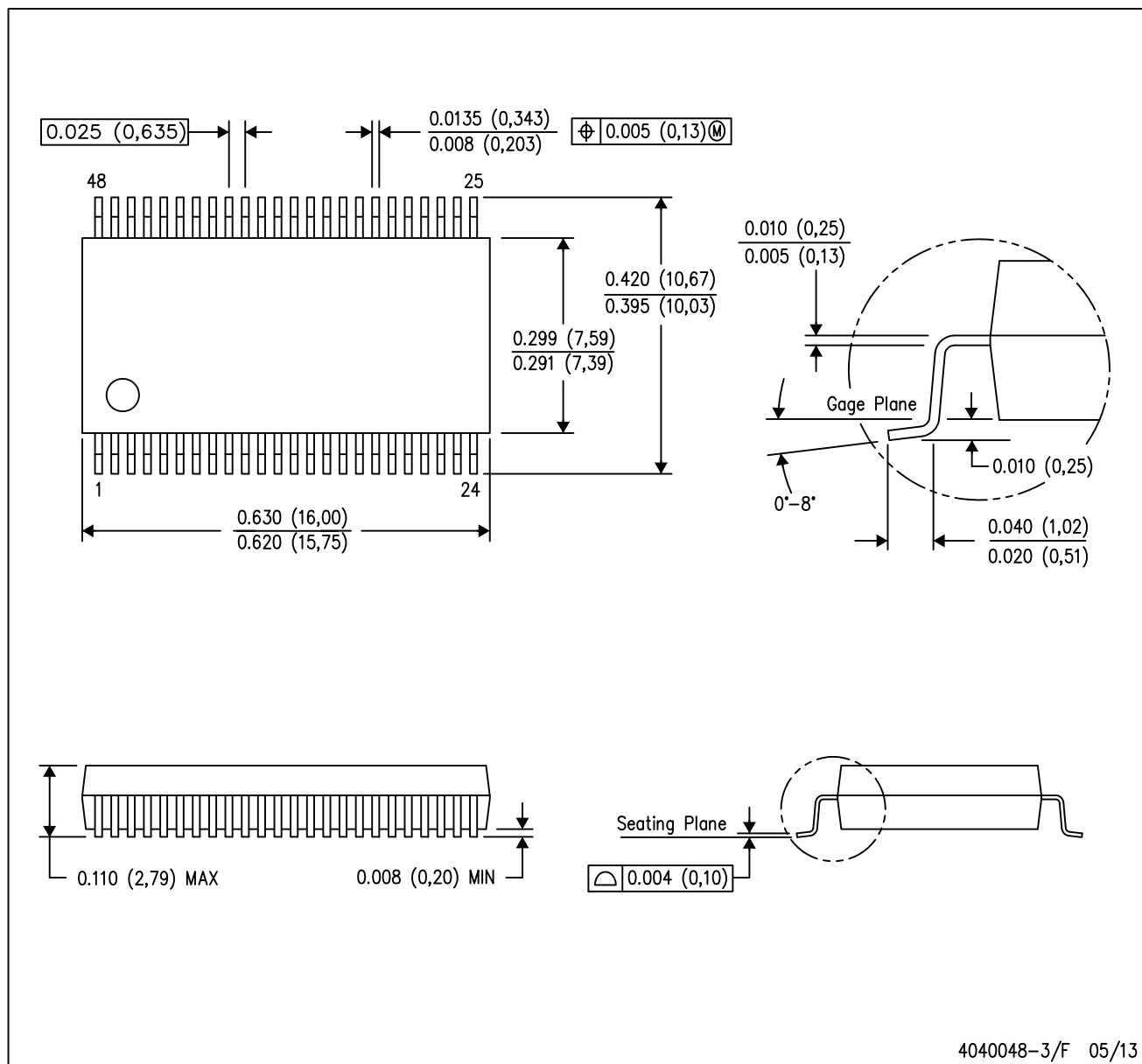
4040048−3/F   05/13

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

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DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ****** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

WD (R-GDFP-F**)   **CERAMIC DUAL FLATPACK**

48 LEADS SHOWN
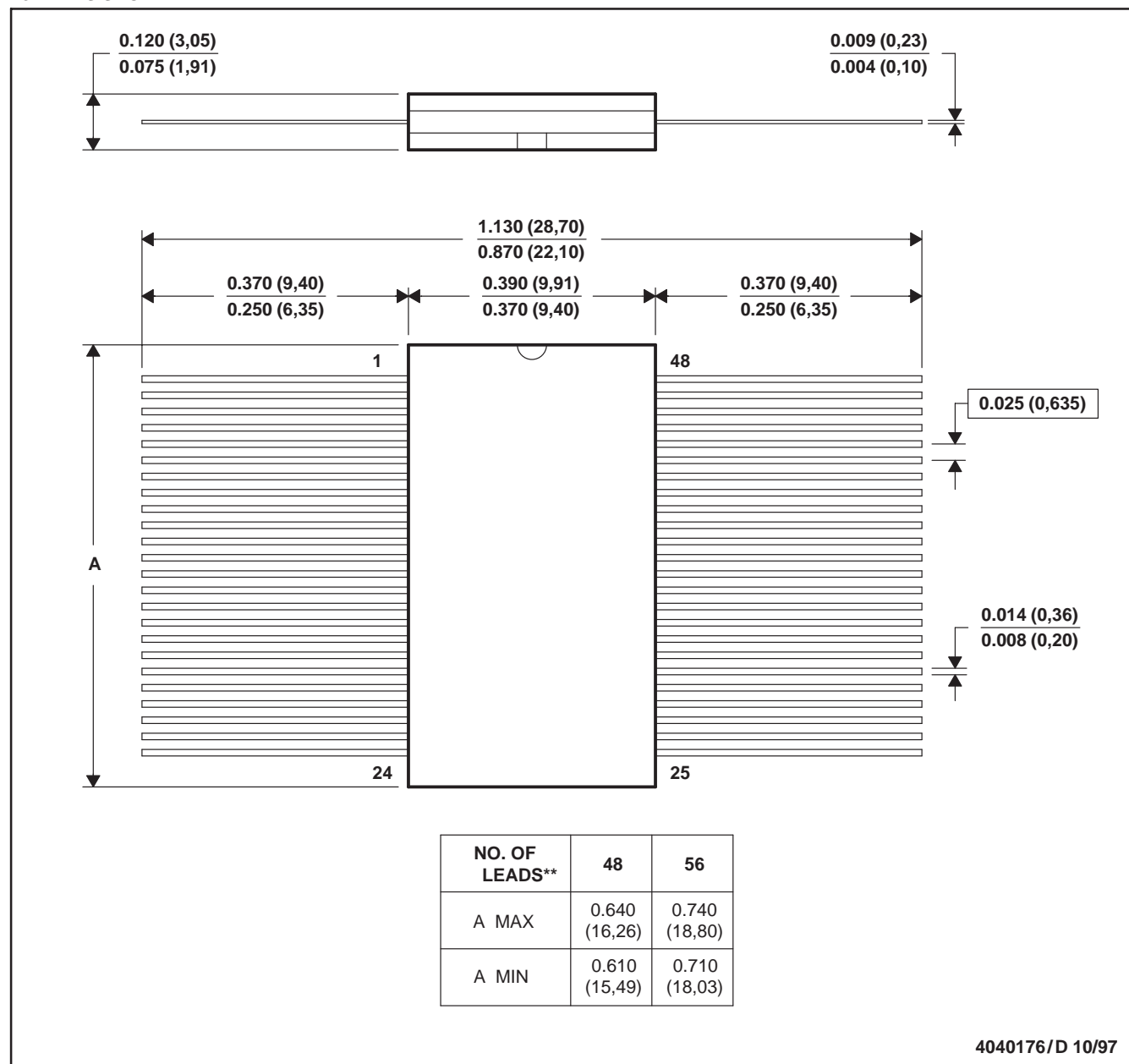
0.120 (3,05)
0.075 (1,91)

0.009 (0,23)
0.004 (0,10)

1.130 (28,70)
0.870 (22,10)

0.370 (9,40)
0.250 (6,35)

0.390 (9,91)
0.370 (9,40)

0.370 (9,40)
0.250 (6,35)

1

48

0.025 (0,635)

A

0.014 (0,36)
0.008 (0,20)

24

25

NO. OF LEADS**	48	56
A MAX	0.640 (16,26)	0.740 (18,80)
A MIN	0.610 (15,49)	0.710 (18,03)

4040176 / D 10/97

NOTES: A. All linear dimensions are in inches (millimeters).
            B. This drawing is subject to change without notice.
            C. This package can be hermetically sealed with a ceramic lid using glass frit.
            D. Index point is provided on cap for terminal identification only
            E. Falls within MIL STD 1835:   GDFP1-F48 and JEDEC MO-146AA
                                             GDFP1-F56 and JEDEC MO-146AB