Dual Schmitt-Trigger Inverter

NL27WZ14

The NL27WZ14 is a high performance dual inverter with Schmitt−Trigger inputs operating from a 1.65 to 5.5 V supply.

ON Semiconductor®

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 3.2 ns t_{PD} at V_{CC} = 5 V (Typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Sink 32 mA at 4.5 V
- Available in SC−88, SC−74, TSOP−6 and UDFN6 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
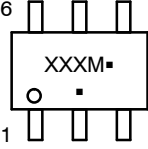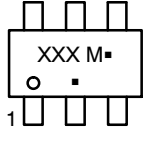- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
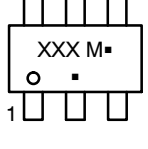
Figure 1. Logic Symbol

MARKING DIAGRAMS

SC−88 DF SUFFIX CASE 419B−02	XXXM▪
SC−74 CASE 318F−05	XXX M▪
TSOP−6 CASE 318G−02	XXX M▪
UDFN6 1.45x1.0, 0.5P CASE 517AQ	XM
UDFN6 1x1, 0.35P CASE 517BX	X M

X, XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NL27WZ14
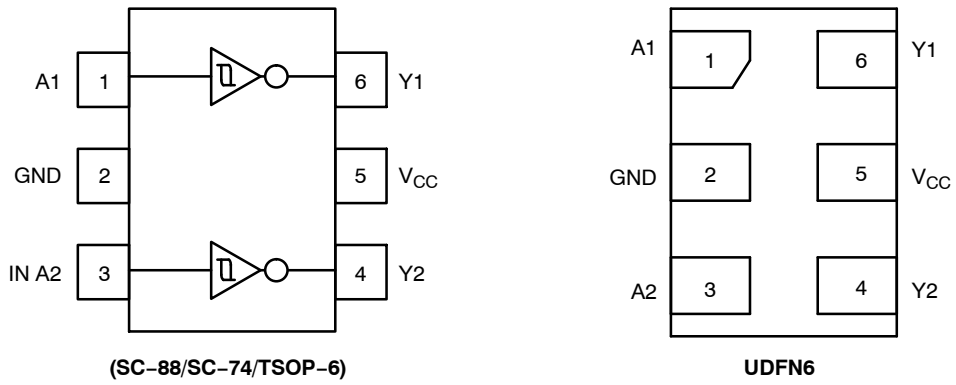
Figure 2. Pinout (Top View)

PIN ASSIGNMENT

Pin	Function
1	A1
2	GND
3	A2
4	Y2
5	V_{CC}
6	Y1

FUNCTION TABLE

A Input	Y Output
L	H
H	L

NL27WZ14

MAXIMUM RATINGS

Symbol	Characteristics		Value	Units
V_{CC}	DC Supply Voltage	TSOP−6, SC−88 (NLV) SC−88, SC−74, UDFN6	−0.5 to +7.0 −0.5 to +6.5	V
V_{IN}	DC Input Voltage	TSOP−6, SC−88 (NLV) SC−88, SC−74, UDFN6	−0.5 to +7.0 −0.5 to +6.5	V
V_{OUT}	DC Output Voltage TSOP−6, SC−88 (NLV)	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} +0.5 −0.5 to +7.0 −0.5 to +7.0	V
	DC Output Voltage SC−88, SC−74, UDFN6	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} +0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IK}	DC Input Diode Current, V_{IN} < GND		−50	mA
I_{OK}	DC Output Diode Current, V_{OUT} < GND		−50	mA
I_{OUT}	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SC−88 SC−74 UDFN6	377 320 154	°C/W
P_D	Power Dissipation in Still Air	SC−88 SC−74 UDFN6	332 390 812	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flamebility Rating	Oxygen Index: 28 to 34	UL 94−V−0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model (NLV) Charged Device Model	2000 1000 N/A	V
$I_{LATCHUP}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to EIA/JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115−A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 5.5	V
T_A	Operating Temperature Range		−55	+125	°C
t_r , t_f	Input Transition Rise or Fall Rate	V_{CC} = 1.65 V to 1.95 V V_{CC} = 2.3 V to 2.7 V V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0 0 0	No Limit No Limit No Limit No Limit	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V$_{CC}$ (V)	T$_A$ = 25°C			−40°C ≤ T$_A$ ≤ 85°C		−55°C ≤ T$_A$ ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V$_{T+}$	Positive Input Threshold Voltage		1.65	–	1.0	1.4	–	1.4	–	1.4	V
			2.3	–	1.5	1.8	–	1.8	–	1.8	
			2.7	–	1.7	2	–	2	–	2	
			3	–	1.9	2.2	–	2.2	–	2.2	
			4.5	–	2.7	3.1	–	3.1	–	3.1	
			5.5	–	3.3	3.6	–	3.6	–	3.6	
V$_{T−}$	Negative Input Threshold Voltage		1.65	0.2	0.5	–	0.2	–	0.2	–	V
			2.3	0.4	0.75	–	0.4	–	0.4	–	
			2.7	0.5	0.87	–	0.5	–	0.5	–	
			3	0.6	1.0	–	0.6	–	0.6	–	
			4.5	1.0	1.5	–	1.0	–	1.0	–	
			5.5	1.2	1.9	–	1.2	–	1.2	–	
V$_H$	Input Hysteresis Voltage		1.65	0.1	0.48	0.9	0.1	0.9	0.1	0.9	V
			2.3	0.25	0.75	1.1	0.25	1.1	0.25	1.1	
			2.7	0.3	0.83	1.15	0.3	1.15	0.3	1.15	
			3	0.4	0.93	1.2	0.4	1.2	0.4	1.2	
			4.5	0.6	1.2	1.5	0.6	1.5	0.6	1.5	
			5.5	0.7	1.4	1.7	0.7	1.7	0.7	1.7	
V$_{OH}$	High−Level Output Voltage V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OH}$ = −100 μA	1.65 to 5.5	V$_{CC}$ − 0.1	V$_{CC}$	–	V$_{CC}$ − 0.1	–	V$_{CC}$ − 0.1	–	V
		I$_{OH}$ = −4 mA	1.65	1.29	1.52	–	1.29	–	1.29	–	
		I$_{OH}$ = −8 mA	2.3	1.9	2.1	–	1.9	–	1.9	–	
		I$_{OH}$ = −12 mA	2.7	2.2	2.4	–	2.2	–	2.2	–	
		I$_{OH}$ = −16 mA	3	2.4	2.7	–	2.4	–	2.4	–	
		I$_{OH}$ = −24 mA	3	2.3	2.5	–	2.3	–	2.3	–	
		I$_{OH}$ = −32 mA	4.5	3.8	4	–	3.8	–	3.8	–	
V$_{OL}$	Low−Level Output Voltage V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OL}$ = 100 μA	1.65 to 5.5	–	–	0.1	–	0.1	–	0.1	V
		I$_{OL}$ = 4 mA	1.65	–	0.08	0.24	–	0.24	–	0.24	
		I$_{OL}$ = 8 mA	2.3	–	0.2	0.3	–	0.3	–	0.3	
		I$_{OL}$ = 12 mA	2.7	–	0.22	0.4	–	0.4	–	0.4	
		I$_{OL}$ = 16 mA	3	–	0.28	0.4	–	0.4	–	0.4	
		I$_{OL}$ = 24 mA	3	–	0.38	0.55	–	0.55	–	0.55	
		I$_{OL}$ = 32 mA	4.5	–	0.42	0.55	–	0.55	–	0.55	
I$_{IN}$	Input Leakage Current	V$_{IN}$ = 5.5 V or GND	1.65 to 5.5	–	–	±0.1	–	±1.0	–	±1.0	μA
I$_{OFF}$	Power Off Leakage Current	V$_{IN}$ = 5.5 V or V$_{OUT}$ = 5.5 V	0	–	–	1	–	10	–	10	μA
I$_{CC}$	Quiescent Supply Current	V$_{IN}$ = 5.5 V or GND	5.5	–	–	1	–	10	–	10	μA

NL27WZ14

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25°C$			$-40°C \leq T_A \leq 85°C$		$-55°C \leq T_A \leq 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
tPLH, tPHL	Propagation Delay, A to Y (Figures 3 and 4)	$R_L = 1\ M\Omega$, $C_L = 15\ pF$	1.65 to 1.95	–	7.1	13	–	14.5	–	15.5	ns
		$R_L = 1\ M\Omega$, $C_L = 15\ pF$	2.3 to 2.7	–	4.3	7.4	–	8.1	–	9.1	
			3.0 to 3.6	–	3.3	5	–	5.5	–	6.5	
			4.5 to 5.5	–	2.7	4.1	–	4.5	–	5.5	
		$R_L = 500\ \Omega$, $C_L = 50\ pF$	3.0 to 3.6	–	4	6	–	6.6	–	7.6	
			4.5 to 5.5	–	3.2	4.9	–	5.4	–	6.4	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5\ V$, $V_I = 0\ V$ or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.5\ V$, $V_I = 0\ V$ or V_{CC}	4.0	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, $V_{CC} = 3.3\ V$, $V_{IN} = 0\ V$ or V_{CC} 10 MHz, $V_{CC} = 5.0\ V$, $V_{IN} = 0\ V$ or V_{CC}	11 12.5	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in}$) I_{CC}. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in}$) $I_{CC} \cdot V_{CC}$.

NL27WZ14

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 3. Test Circuit

Test	Switch Position	C_L, pF	R_L, Ω	R_1, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	2 x V_{CC}	–	–	–
		See AC Characteristics Table		
t_{PHZ} / t_{PZH}	GND	–	–	–
		See AC Characteristics Table		

X = Don't Care

Figure 4. Switching Waveforms

		V_{mo}, V		
V_{CC}, V	V_{mi}, V	t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}	V_Y, V
1.65 to 1.95	$V_{CC}/2$	V_{CC} / 2	V_{CC} / 2	0.15
2.3 to 2.7	$V_{CC}/2$	V_{CC} / 2	V_{CC} / 2	0.15
3.0 to 3.6	$V_{CC}/2$	V_{CC} / 2	V_{CC} / 2	0.3
4.5 to 5.5	$V_{CC}/2$	V_{CC} / 2	V_{CC} / 2	0.3

NL27WZ14

ORDERING INFORMATION

Device	Package	Specific Device Code	Pin1 Orientation (See below)	Shipping†
NL27WZ14DFT2G	SC−88	MA	Q4	3000 / Tape & Reel
NL27WZ14DFT4G	SC−88	MA	Q4	10000 / Tape & Reel
NLV27WZ14DFT2G*	SC−88	MA	Q4	3000 / Tape & Reel
NL27WZ14DTT1G	TSOP−6	MA	Q4	3000 / Tape & Reel
NL27WZ14DBVT1G	SC−74	MA	Q4	3000 / Tape & Reel
NL27WZ14MU1TCG	UDFN6, 1.45 x 1.0, 0.5P	P (Rotated 90° CW)	Q4	3000 / Tape & Reel
NL27WZ14MU3TCG	UDFN6, 1.0 x 1.0, 0.35P	3 (Rotated 90° CW)	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel
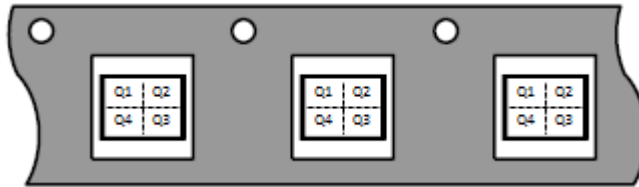
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−74
CASE 318F−05
ISSUE N

DATE 08 JUN 2012

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SCALE 2:1

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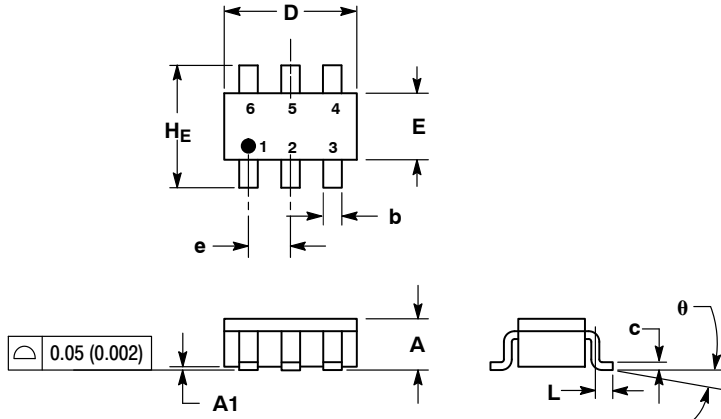
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

SOLDERING FOOTPRINT*
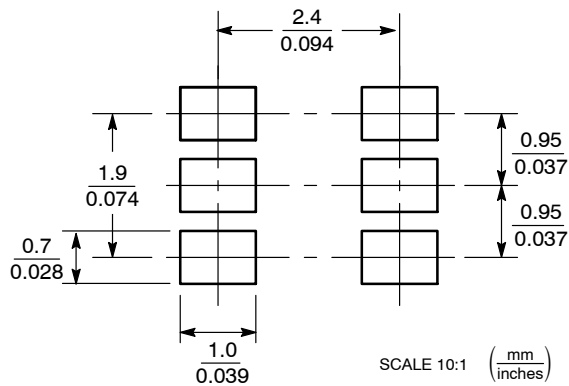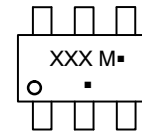
2.4
0.094

1.9
0.074

0.7
0.028

0.95
0.037

0.95
0.037

1.0
0.039

SCALE 10:1 $\left(\dfrac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXX M■

O   ■

XXX = Specific Device Code
M = Date Code
■ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ■", may or may not be present.

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3

STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1

STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

DOCUMENT NUMBER:	98ASB42973B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−74		PAGE 1 OF 1

TSOP−6
CASE 318G−02
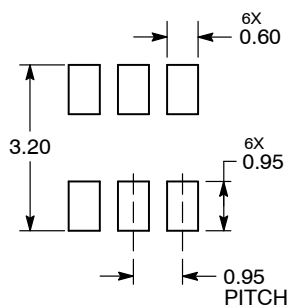ISSUE V

SCALE 2:1

DATE 12 JUN 2012

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DETAIL Z

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	−	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

RECOMMENDED SOLDERING FOOTPRINT*

6X
0.60

3.20

6X
0.95

0.95
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXAYW▪

IC

XXX M▪

STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present.

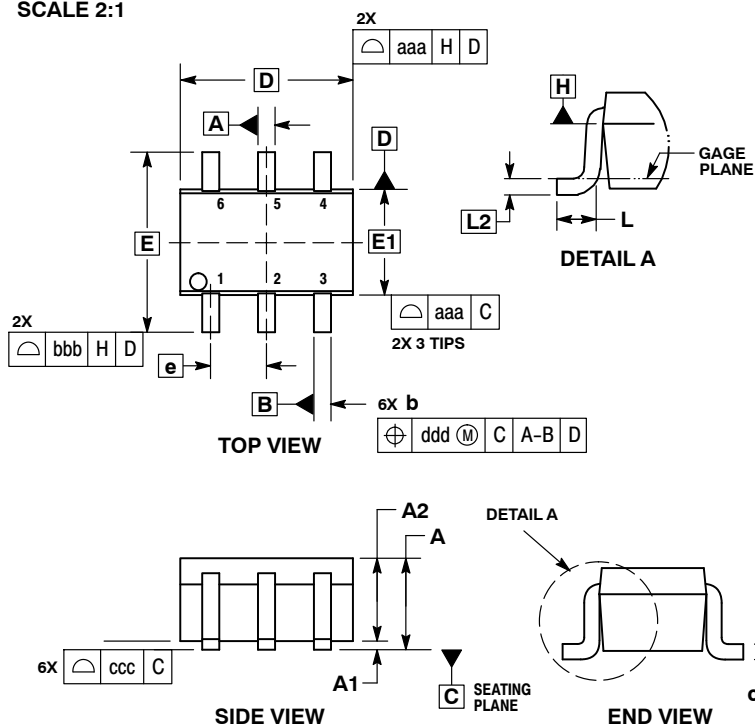| DOCUMENT NUMBER:	98ASB14888C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TSOP−6		PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

1
SCALE 2:1

TOP VIEW

DETAIL A

SIDE VIEW

END VIEW
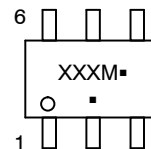
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–––	–––	1.10	–––	–––	0.043
A1	0.00	–––	0.10	0.000	–––	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*

6X
0.30

6X
0.66

2.50

0.65
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

6

XXXM■
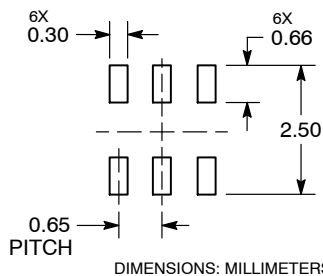
1

XXX = Specific Device Code
M = Date Code*
■ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ■", may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−88/SC70−6/SOT−363		PAGE 1 OF 2

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
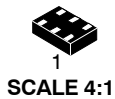2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−88/SC70−6/SOT−363		PAGE 2 OF 2

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ–01
ISSUE O

DATE 15 MAY 2008

SCALE 4:1

1

TOP VIEW

| 0.10 | C |

| 0.10 | C |

PIN ONE
REFERENCE

D
A
B
E

SIDE VIEW

| 0.05 | C |

6X | 0.05 | C |

DETAIL B

A
A1
A2
C SEATING PLANE

BOTTOM VIEW

e
6X L
6X b

DETAIL A

1 3
6 4

| ⊕ | 0.10 | C | A | B |
| | 0.05 | C | NOTE 3 |
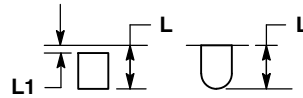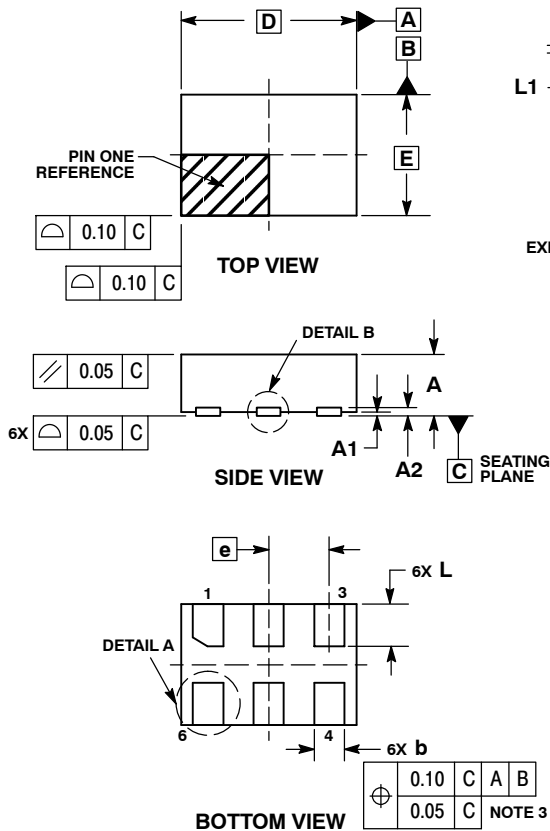
DETAIL A
OPTIONAL CONSTRUCTIONS

L
L1
L
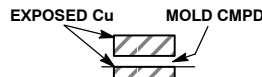
DETAIL B
OPTIONAL CONSTRUCTIONS

EXPOSED Cu
MOLD CMPD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

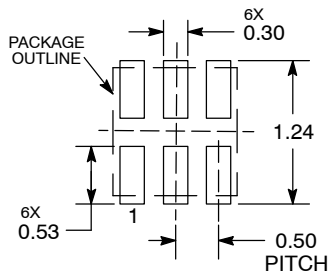| DIM | MILLIMETERS | |
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	–––	0.15

GENERIC MARKING DIAGRAM*

XM

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present.

MOUNTING FOOTPRINT

PACKAGE OUTLINE

6X
0.30

1.24

6X
0.53

1

0.50
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY K. VAN TYNE.	15 MAY 2008

UDFN6, 1x1, 0.35P
CASE 517BX–01
ISSUE O

SCALE 4:1

DATE 18 MAY 2011

PIN ONE REFERENCE

2X ⌓ 0.10 C

2X ⌓ 0.10 C **TOP VIEW**

⫽ 0.05 C

⌓ 0.05 C **SIDE VIEW**

A3

A

A1

Ⓒ SEATING PLANE

BOTTOM VIEW

⊕ | 0.10 Ⓜ | C | A | B
| 0.05 Ⓜ | C | NOTE 3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

GENERIC MARKING DIAGRAM*

X M

1 ○

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*

5X
0.48

6X
0.22

1.18

0.53

1

PKG OUTLINE

0.35

PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON56787E	
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	UDFN6, 1X1, 0.35P	PAGE 1 OF 2

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O	RELEASED FOR PRODUCTION. REQ. BY I. CAMBALIZA.	18 MAY 2011

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