ON Semiconductor®

FDC6506P

Dual P-Channel Logic Level PowerTrench™ MOSFET

General Description

These P-Channel logic level MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

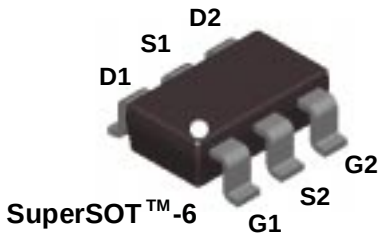
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

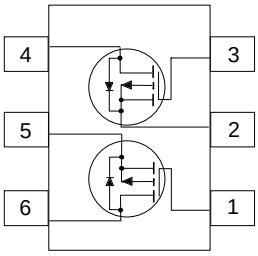
Applications

- Load switch
- Battery protection
- Power management

Features

- -1.8 A, -30 V. $R_{DS(on)}$ = 0.170 Ω @ V_{GS} = -10 V
  $R_{DS(on)}$ = 0.280 Ω @ V_{GS} = -4.5 V
- Low gate charge (2.3nC typical).
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$.
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick).





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current - Continuous	(Note 1a)	-1.8	A
	- Pulsed		-10	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.96	W
		(Note 1b)	0.9	
		(Note 1c)	0.7	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60	°C/W

Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.506	FDC6506P	7''	8mm	3000 units

October-2017, Rev. 3

Publication Order Number:
FDC6506P/D

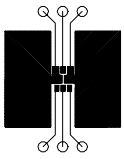
Electrical Characteristics

T_A = 25°C unless otherwise noted

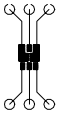
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		-20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -1.8 A V_{GS} = -10 V, I_D = -1.8 A @125°C V_{GS} = -4.5 V, I_D = -1.4 A		0.14 0.20 0.22	0.17 0.27 0.28	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = - 5 V	-10			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -1.8 A		3		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		190		pF
C_{oss}	Output Capacitance			70		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -15 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		7	14	ns
t_r	Turn-On Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			14	25	ns
t_f	Turn-Off Fall Time			2	6	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -1.8 A, V_{GS} = -10 V		2.3	3.5	nC
Q_{gs}	Gate-Source Charge			1		nC
Q_{gd}	Gate-Drain Charge			0.8		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.8	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.8 A (Note 2)		-0.8	-1.2	V

Notes:

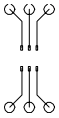
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.Both devices are assumed to be operating and sharing the dissipated heat energy equally.



a) 130 °C/W when mounted on a 0.125 in^2 pad of 2 oz. copper.



b) 140 °C/W when mounted on a 0.005 in^2 pad of 2 oz. copper.



c) 180 °C/W when mounted on a 0.0015 in^2 pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics

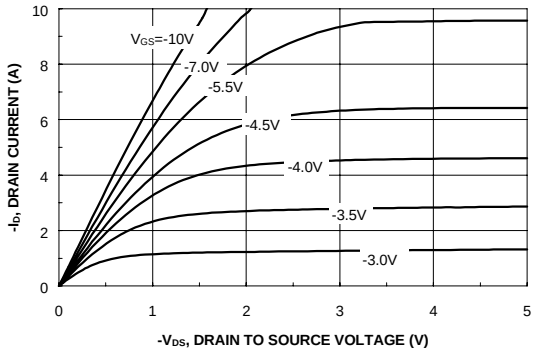


Figure 1. On-Region Characteristics.

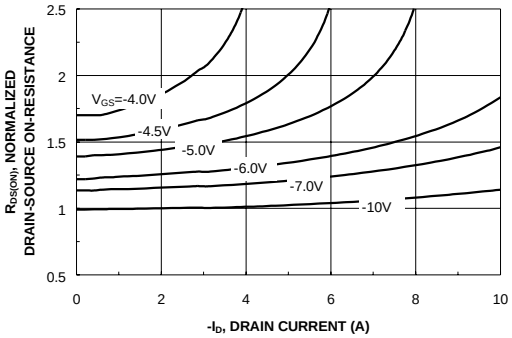


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

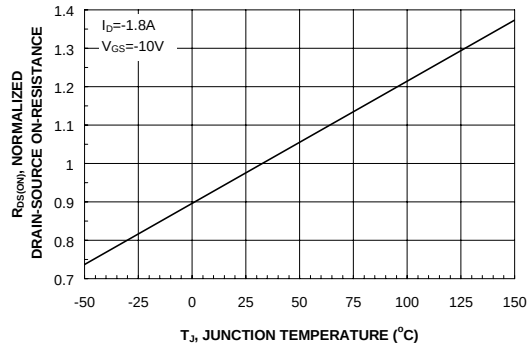


Figure 3. On-Resistance Variation with Temperature.

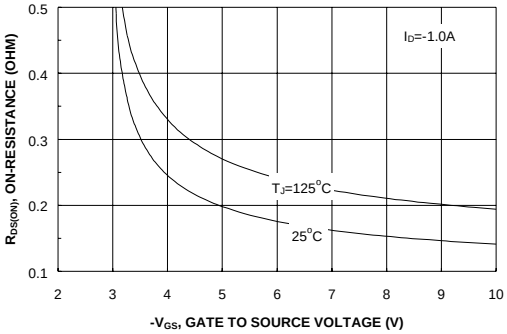


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

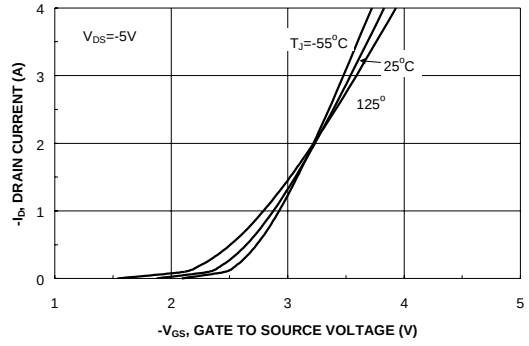


Figure 5. Transfer Characteristics.

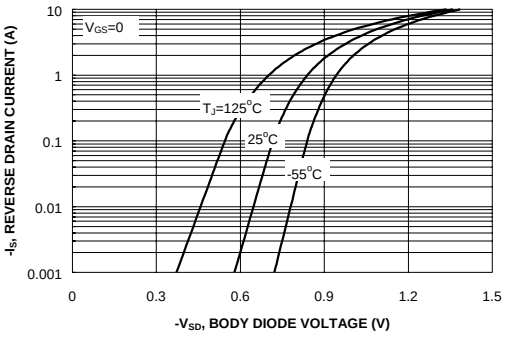


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

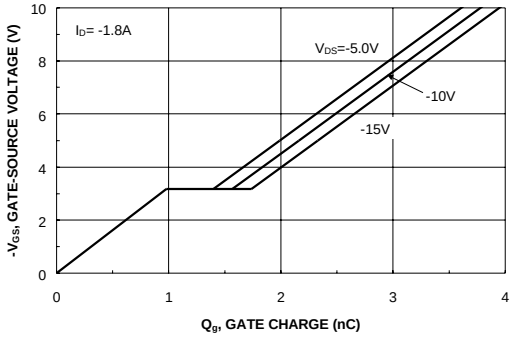


Figure 7. Gate-Charge Characteristics.

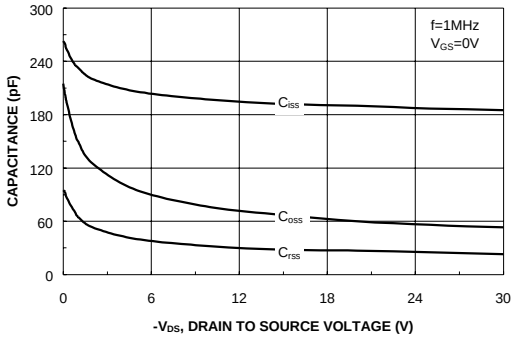


Figure 8. Capacitance Characteristics.

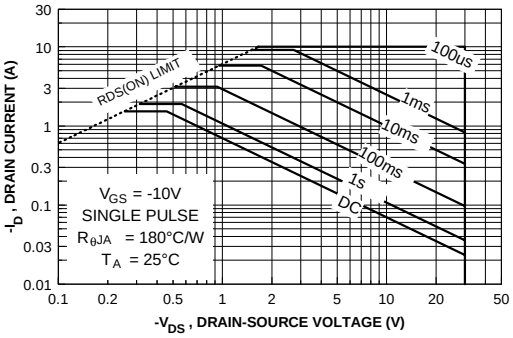


Figure 9. Maximum Safe Operating Area.

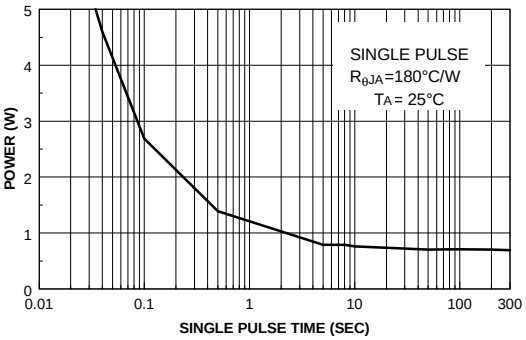


Figure 10. Single Pulse Maximum Power Dissipation.

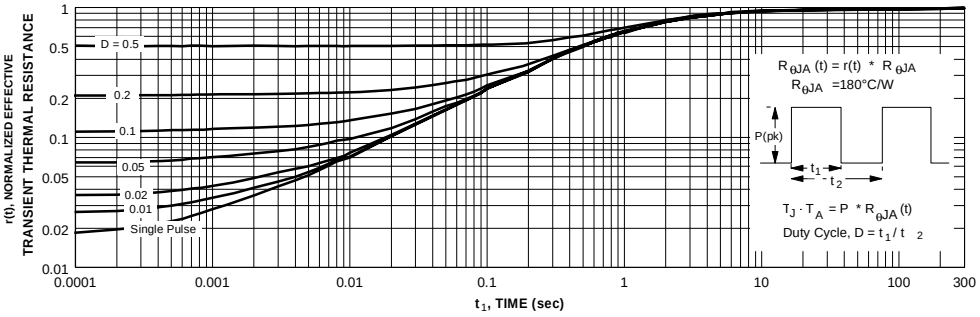


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient themal response will change depending on the circuit board design.

PUBLICATION ORDERING INFORMATION

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