



# PJT7601

## 20V Complementary Enhancement Mode MOSFET – ESD Protected

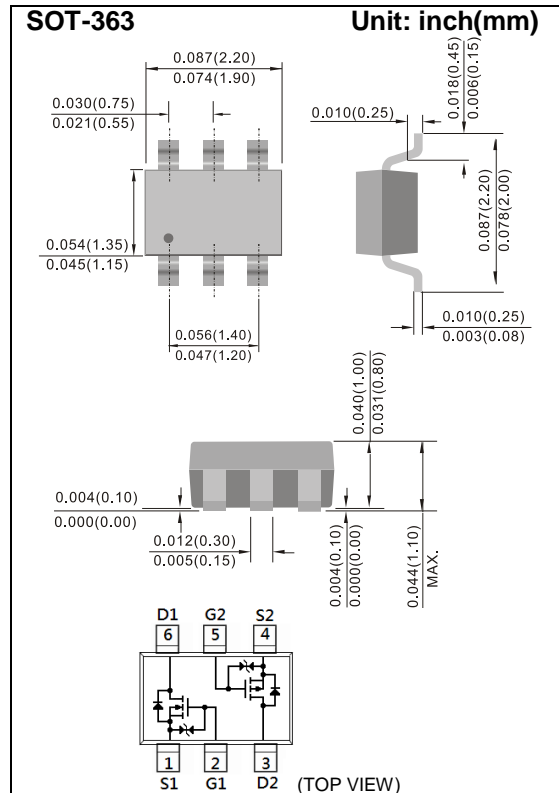
**Voltage** 20/-20V **Current** 0.5/-0.5A

### Features

- Low Voltage Drive (1.2V)
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- ESD Protected
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std. (Halogen Free)

### Mechanical Data

- Case: SOT-363 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0002 ounces, 0.006 grams



### Maximum Ratings and Thermal Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER		SYMBOL	N-Ch LIMIT	P-Ch LIMIT	UNITS
Drain-Source Voltage		V <sub>DS</sub>	20	-20	V
Gate-Source Voltage		V <sub>GS</sub>	±10	±10	V
Continuous Drain Current		I <sub>D</sub>	0.5	-0.5	A
Pulsed Drain Current (Note 4)		I <sub>DM</sub>	1.0	-1.0	A
Power Dissipation	T <sub>a</sub> =25°C	P <sub>D</sub>	350		mW
	Derate above 25°C		2.8		mW/°C
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55~150		°C
Typical Thermal resistance		R <sub>θJA</sub>	357		°C/W
- Junction to Ambient (Note 3)					



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## N-Channel Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.3	0.65	0.9	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=500mA$	-	280	400	m $\Omega$
		$V_{GS}=2.5V, I_D=200mA$	-	350	650	
		$V_{GS}=1.8V, I_D=100mA$	-	400	800	
		$V_{GS}=1.5V, I_D=50mA$	-	500	1200	
		$V_{GS}=1.2V, I_D=20mA$	-	700	3000	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=16V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 8V, V_{DS}=0V$	-	$\pm 0.5$	$\pm 10$	$\mu A$
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$Q_g$	$V_{DS}=10V, I_D=500mA,$ $V_{GS}=4.5V$ (Note 1,2)	-	1.4	-	nC
Gate-Source Charge	$Q_{gs}$		-	0.22	-	
Gate-Drain Charge	$Q_{gd}$		-	0.21	-	
Input Capacitance	$C_{iss}$	$V_{DS}=10V, V_{GS}=0V,$ $f=1.0MHz$	-	67	-	pF
Output Capacitance	$C_{oss}$		-	19	-	
Reverse Transfer Capacitance	$C_{rss}$		-	6	-	
<b>Switching</b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=150mA,$ $V_{GS}=4.0V, R_G=10\Omega$ (Note 1,2)	-	2.8	-	ns
Turn-On Rise Time	$t_r$		-	20	-	
Turn-Off Delay Time	$t_{d(off)}$		-	23	-	
Turn-Off Fall Time	$t_f$		-	23	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$	---	-	-	500	mA
Diode Forward Voltage	$V_{SD}$	$I_S=500mA, V_{GS}=0V$	-	0.87	1.3	V



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PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.3	-0.6	-1	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-500mA$	-	850	1200	m $\Omega$
		$V_{GS}=-2.5V, I_D=-200mA$	-	990	1500	
		$V_{GS}=-1.8V, I_D=-100mA$	-	1160	2200	
		$V_{GS}=-1.5V, I_D=-50mA$	-	1330	3600	
		$V_{GS}=-1.2V, I_D=-10mA$	-	1500	6000	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-16V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 8V, V_{DS}=0V$	-	$\pm 2$	$\pm 10$	$\mu A$
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$Q_g$	$V_{DS}=-10V, I_D=-500mA,$ $V_{GS}=-4.5V$ (Note 1,2)	-	1.4	-	nC
Gate-Source Charge	$Q_{gs}$		-	0.19	-	
Gate-Drain Charge	$Q_{gd}$		-	0.2	-	
Input Capacitance	$C_{iss}$	$V_{DS}=-10V, V_{GS}=0V,$ $f=1.0MHz$	-	38	-	pF
Output Capacitance	$C_{oss}$		-	15	-	
Reverse Transfer Capacitance	$C_{rss}$		-	9	-	
<b>Switching</b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-500mA,$ $V_{GS}=-4.5V, R_G=6\Omega$ (Note 1,2)	-	7.2	-	ns
Turn-On Rise Time	$t_r$		-	21	-	
Turn-Off Delay Time	$t_{d(off)}$		-	85	-	
Turn-Off Fall Time	$t_f$		-	116	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$	---	-	-	-500	mA
Diode Forward Voltage	$V_{SD}$	$I_S=-500mA, V_{GS}=0V$	-	-0.93	-1.3	V

NOTES :

1. Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.



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## N-Channel TYPICAL CHARACTERISTIC CURVES

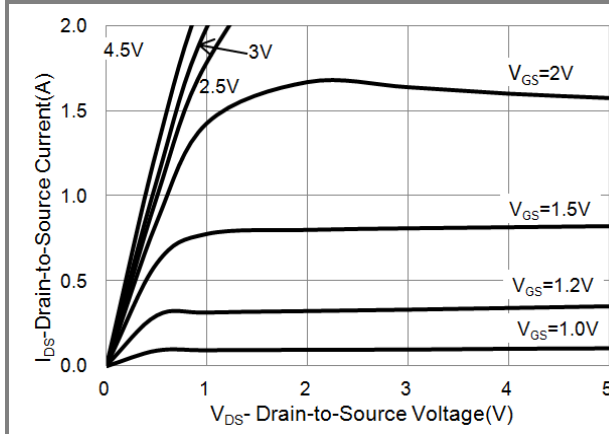


Fig.1 On-Region Characteristics

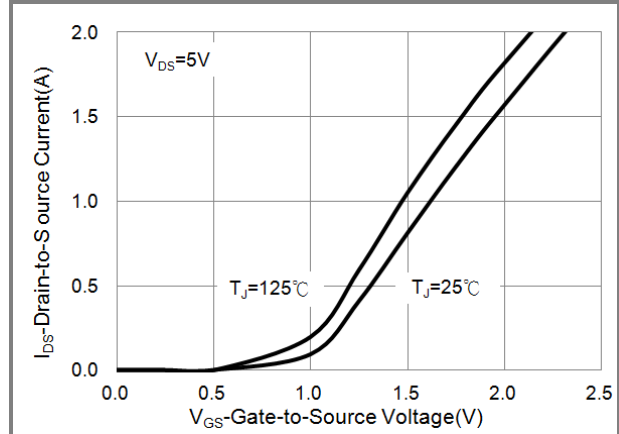


Fig.2 Transfer Characteristics

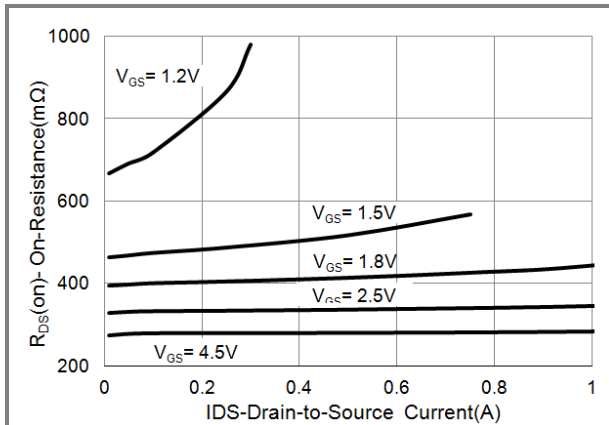


Fig.3 On-Resistance vs. Drain Current

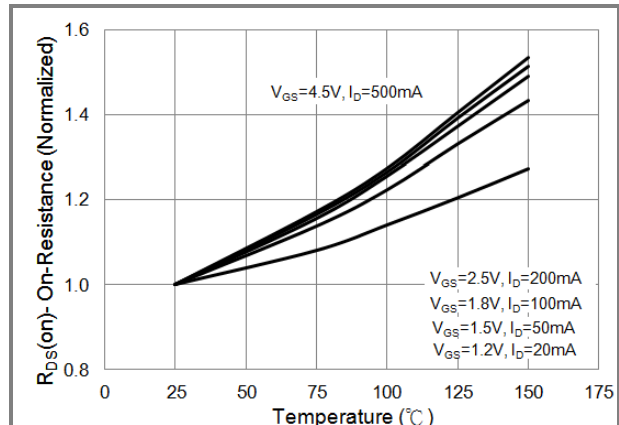


Fig.4 On-Resistance vs. Junction temperature

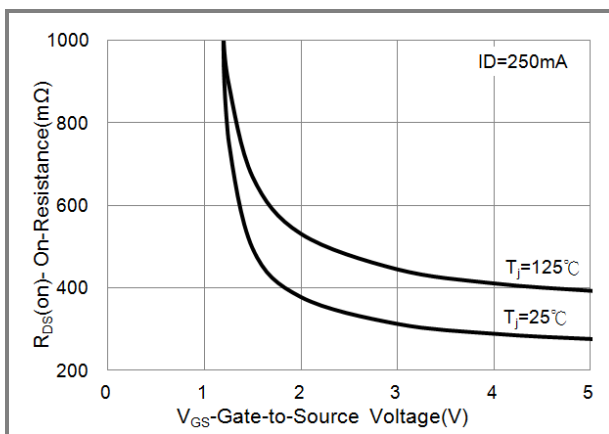


Fig.5 On-Resistance Variation with VGS.

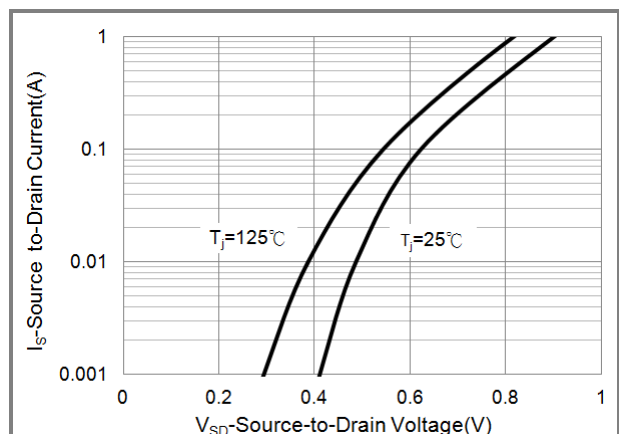


Fig.6 Body Diode Characteristics



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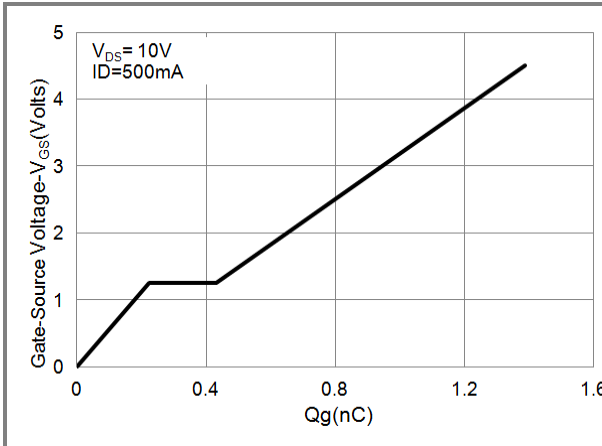


Fig.7 Gate-Charge Characteristics

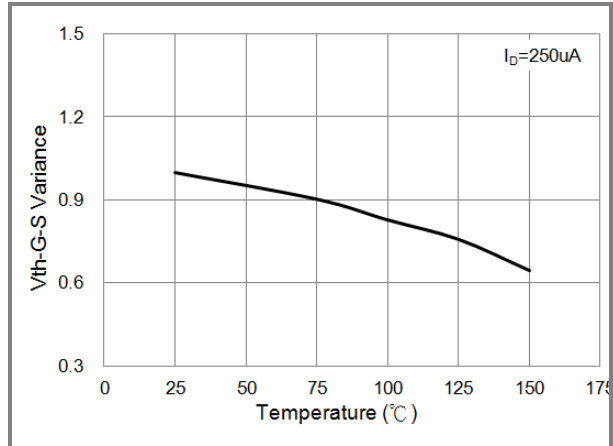


Fig.8 Threshold Voltage Variation with Temperature.

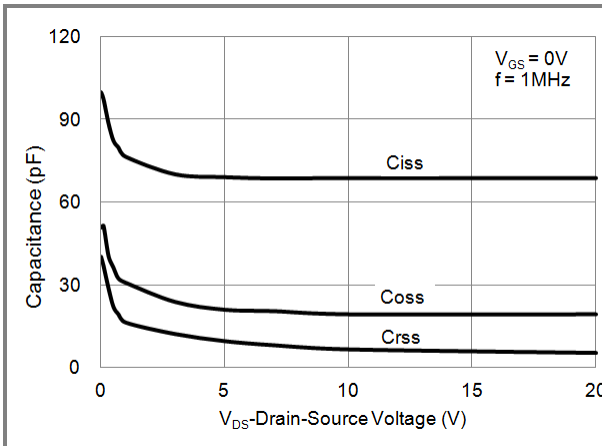


Fig.9 Capacitance vs. Drain-Source Voltage.



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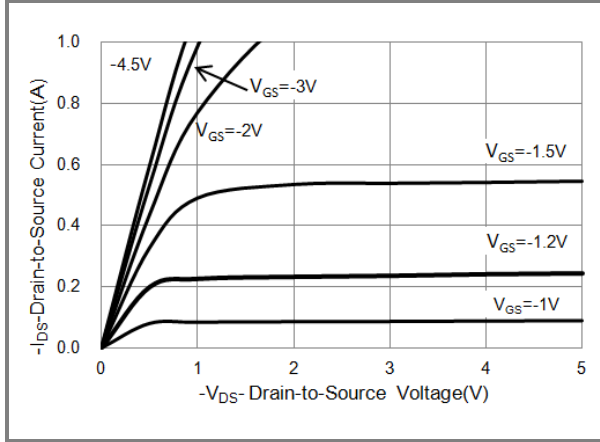


Fig.1 On-Region Characteristics

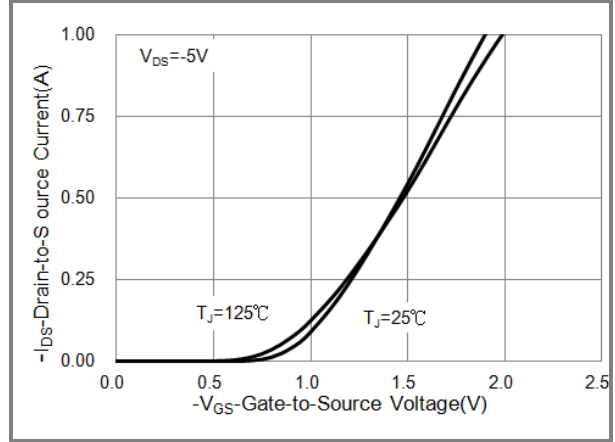


Fig.2 Transfer Characteristics

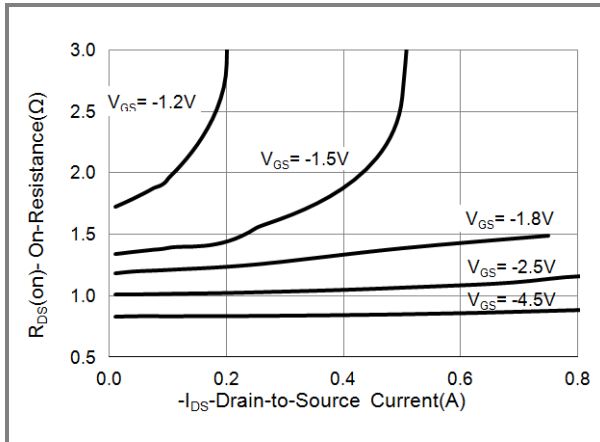


Fig.3 On-Resistance vs. Drain Current

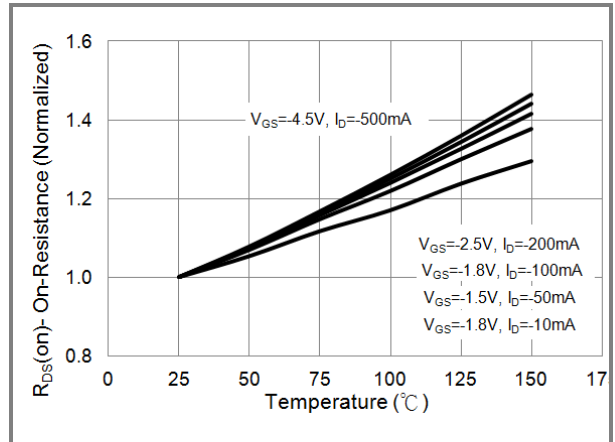


Fig.4 On-Resistance vs. Junction temperature

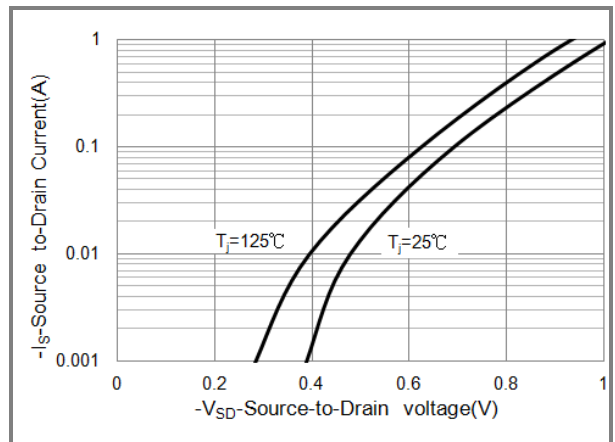
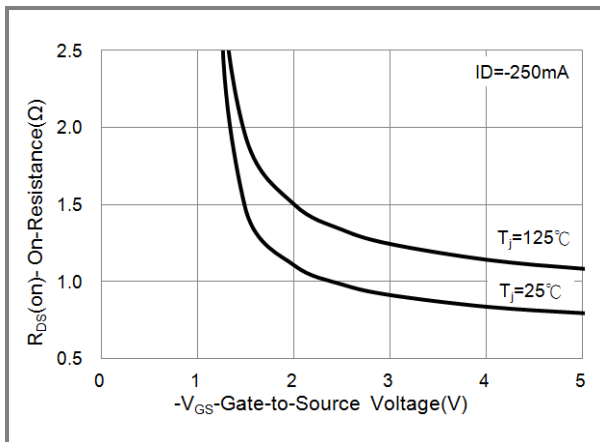


Fig.6 Body Diode Characteristics



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## P-Channel TYPICAL CHARACTERISTIC CURVES

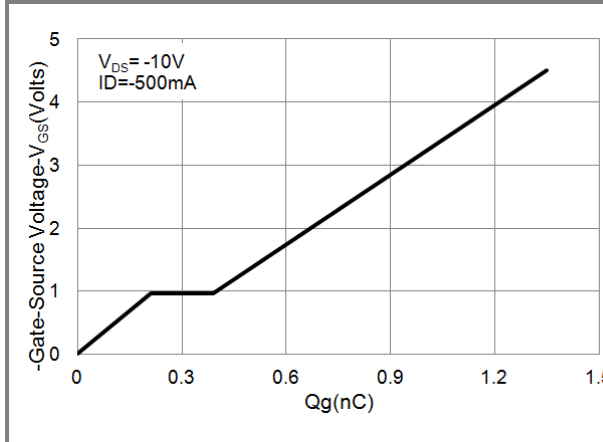


Fig.7 Gate-Charge Characteristics

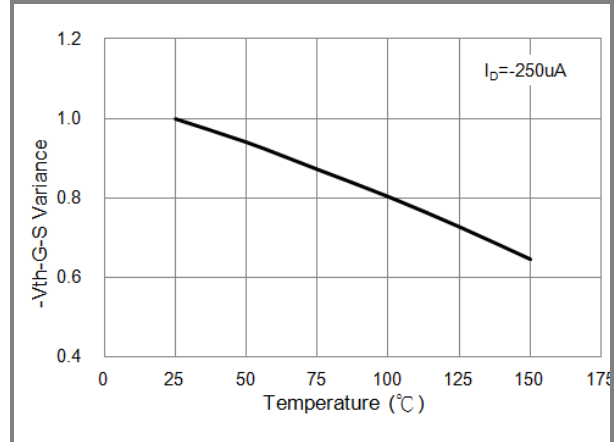


Fig.8 Threshold Voltage Variation with Temperature.

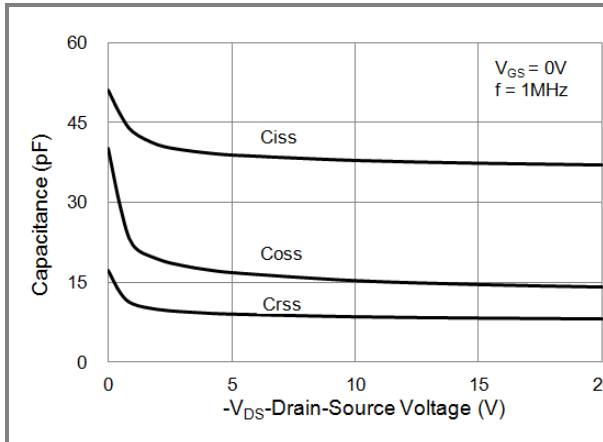


Fig.9 Threshold Voltage Variation with Temperature.

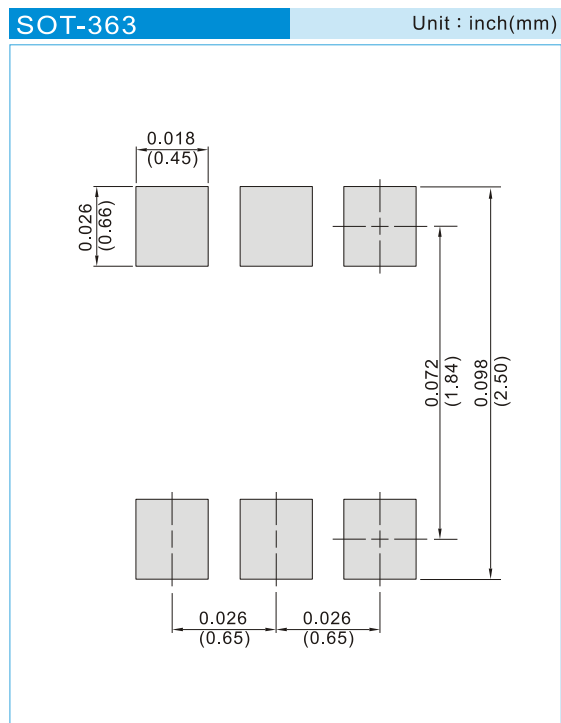


# PJT7601

## PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJT7601_R1_00001	SOT-363	3K pcs / 7" reel	T61	Halogen free
PJT7601_R2_00001	SOT-363	10K pcs / 13" reel	T61	Halogen free

## MOUNTING PAD LAYOUT







## PJT7601

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