



PJS6835

20V P-Channel Enhancement Mode MOSFET – ESD Protected

Voltage **-20 V** **Current** **-500mA**

Features

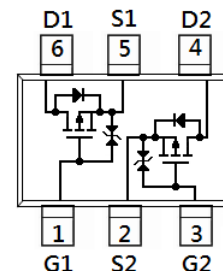
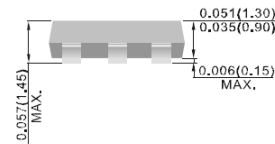
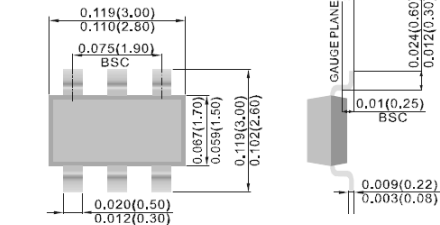
- Low Voltage Drive (1.2V).
- Advanced Trench Process Technology
- Specially Designed for Load switch, PWM Application, etc.
- ESD Protected
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOT-23 6L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0005 ounces, 0.0141 grams
- Marking: SG5

SOT-23 6L

Unit: inch(mm)



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	V _{DS}	-20	V	
Gate-Source Voltage	V _{GS}	±10	V	
Continuous Drain Current	I _D	-500	mA	
Pulsed Drain Current (Note 4)	I _{DM}	-1000	mA	
Power Dissipation	P _D	T _a =25°C	500	mW
		Derate above 25°C	4	mW/°C
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C	
Typical Thermal resistance	R _{θJA}	250	°C/W	
- Junction to Ambient (Note 3)				



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.3	-0.59	-1.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-500mA$	-	0.85	1.2	Ω
		$V_{GS}=-2.5V, I_D=-200mA$	-	0.98	1.5	
		$V_{GS}=-1.8V, I_D=-100mA$	-	1.15	2.2	
		$V_{GS}=-1.5V, I_D=-50mA$	-	1.33	3.6	
		$V_{GS}=-1.2V, I_D=-10mA$	-	1.5	6.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-16V, V_{GS}=0V$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 8V, V_{DS}=0V$	-	± 2	± 10	μA
Dynamic ^(Note 5)						
Total Gate Charge	Q_g	$V_{DS}=-10V, I_D=-500mA,$ $V_{GS}=-4.5V$ ^(Note 1,2)	-	1.4	-	nC
Gate-Source Charge	Q_{gs}		-	0.19	-	
Gate-Drain Charge	Q_{gd}		-	0.2	-	
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V,$ $f=1.0MHz$	-	38	-	pF
Output Capacitance	C_{oss}		-	15	-	
Reverse Transfer Capacitance	C_{rss}		-	9	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-500mA,$ $V_{GS}=-4.5V,$ $R_G=6\Omega$ ^(Note 1,2)	-	7.2	-	ns
Turn-On Rise Time	t_r		-	21	-	
Turn-Off Delay Time	$t_{d(off)}$		-	85	-	
Turn-Off Fall Time	t_f		-	116	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-500	mA
Diode Forward Voltage	V_{SD}	$I_S=-500mA, V_{GS}=0V$	-	-0.93	-1.3	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

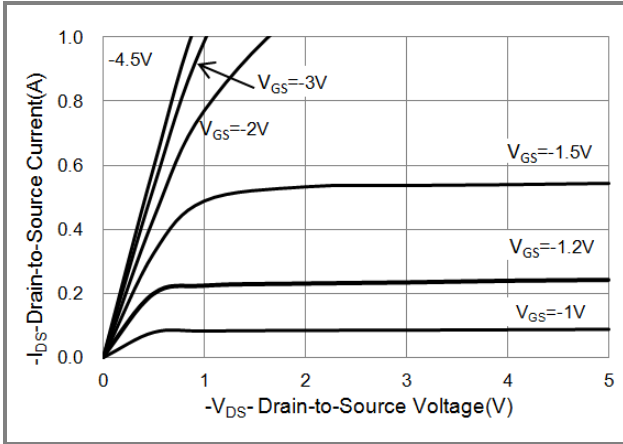


Fig.1 On-Region Characteristics

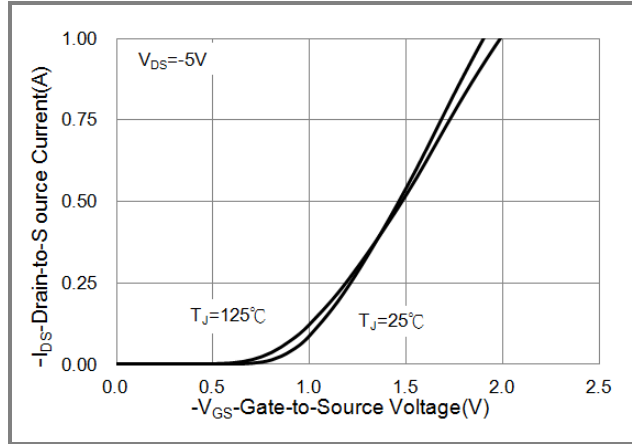


Fig.2 Transfer Characteristics

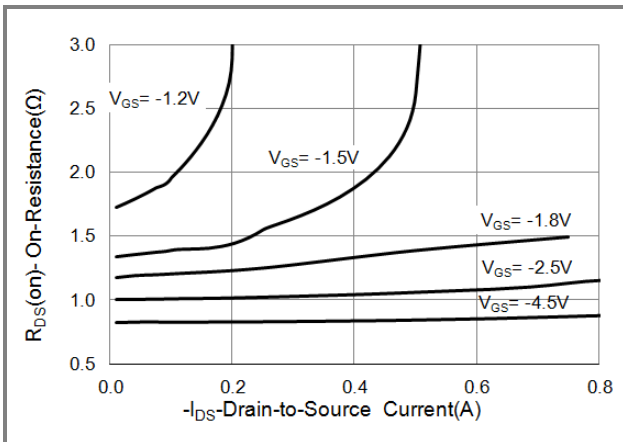


Fig.3 On-Resistance vs. Drain Current

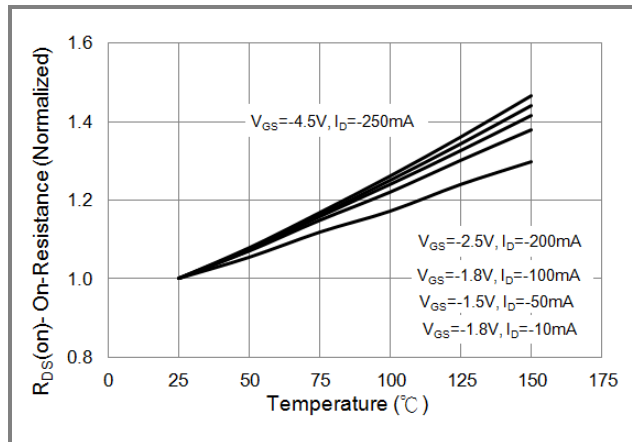


Fig.4 On-Resistance vs. Junction temperature

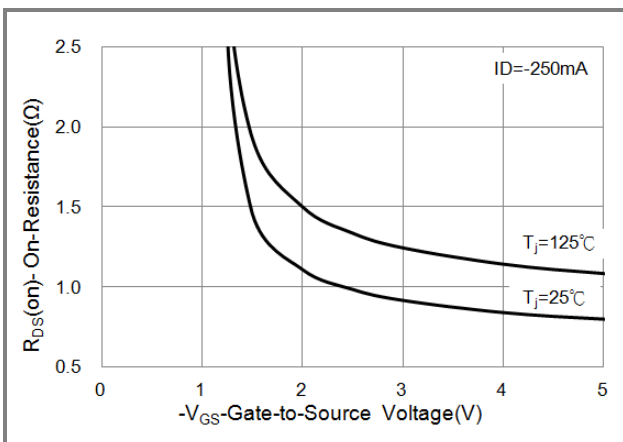


Fig.5 On-Resistance Variation with VGS.

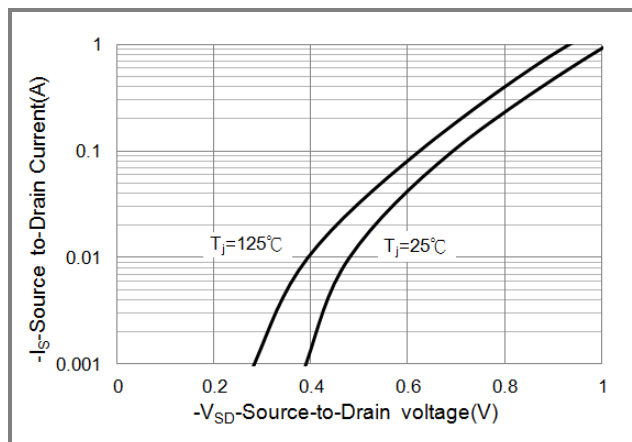


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

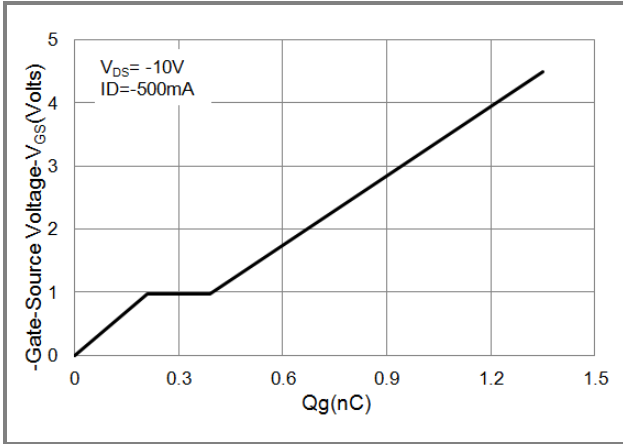


Fig.7 Gate-Charge Characteristics

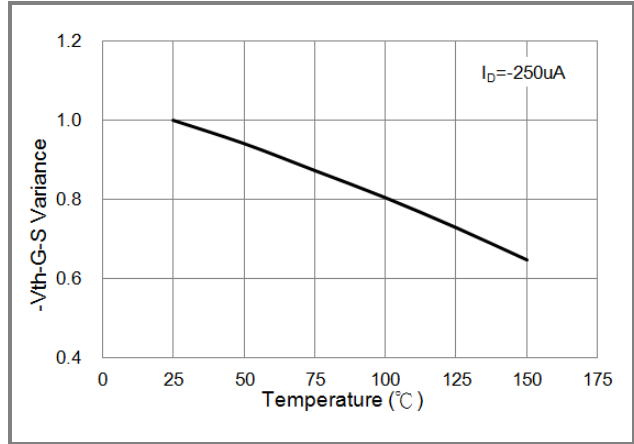


Fig.8 Threshold Voltage Variation with Temperature.

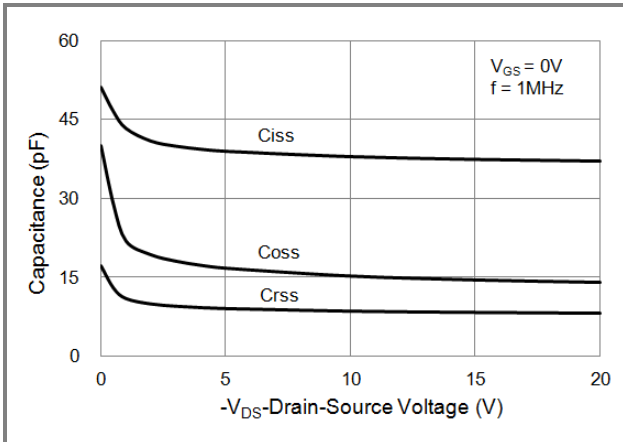


Fig.9 Capacitance vs. Drain-Source Voltage.

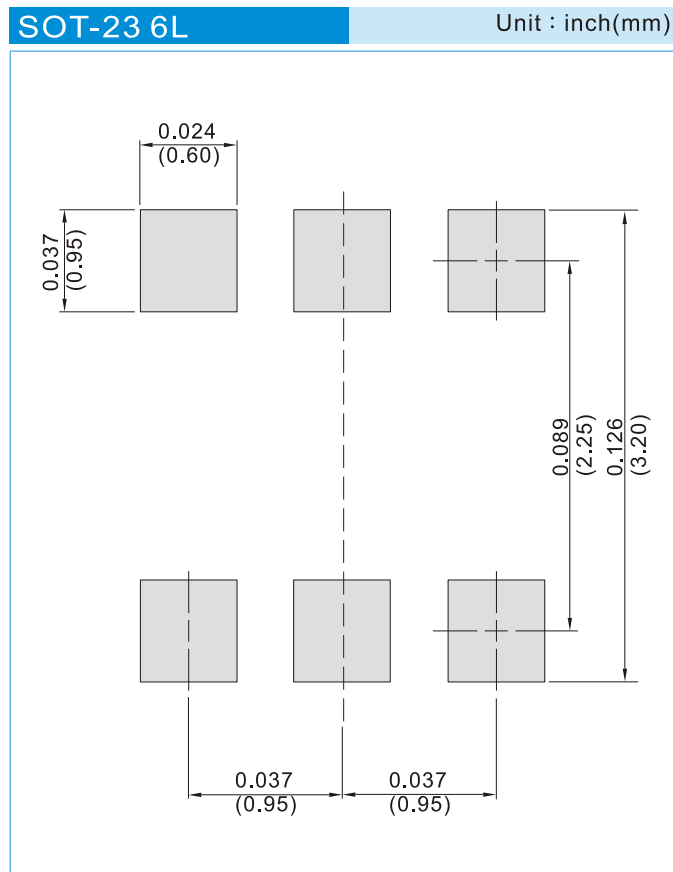


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PART NO PACKING CODE VERSION

PART NO PACKING CODE	Package Type	Packing type	Marking	Version
PJS6835_S1_00001	SOT-23 6L	3K pcs / 7" reel	SG5	Halogen free
PJS6835_S2_00001	SOT-23 6L	10K pcs / 13" reel	SG5	Halogen free

MOUNTING PAD LAYOUT





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