



#### 20V N-Channel Enhancement Mode MOSFET

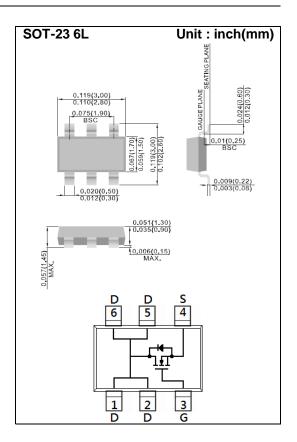
Voltage 20 V Current 7.4A

#### **Features**

- RDS(ON), VGS@4.5V, ID@7.4A<27m $\Omega$
- RDS(ON) , VGS@2.5V, ID@4.7A<41mΩ</li>
- RDS(ON) , VGS@1.8V, ID@1.8A<85mΩ</li>
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc..
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

#### **Mechanical Data**

- Case: SOT-23 6L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0005 ounces, 0.014 grams
- Marking: S16



### Maximum Ratings and Thermal Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V <sub>DS</sub>	20	V
Gate-Source Voltage		$V_{GS}$	<u>+</u> 12	V
Continuous Drain Current		I <sub>D</sub>	7.4	Α
Pulsed Drain Current		I <sub>DM</sub>	29.6	Α
Power Dissipation	T <sub>a</sub> =25°C	P <sub>D</sub>	2	W
	Derate above 25°C		16	mW/°C
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~150	°C
Typical Thermal resistance - Junction to Ambient (Note 3)		$R_{\theta JA}$	62.5	°C/W





## **Electrical Characteristics** (T<sub>A</sub>=25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS		
Static								
Drain-Source Breakdown Voltage	$BV_{DSS}$	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20	-	-	V		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=250uA$	0.5	0.77	1.2	V		
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =7.4A	-	24	27	mΩ		
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =4.7A	-	33	41			
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =1.8A	-	62	85			
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ =20V, $V_{GS}$ =0V	-	0.01	1	uA		
Gate-Source Leakage Current	$I_{GSS}$	V <sub>GS</sub> = <u>+</u> 12V, V <sub>DS</sub> =0V	1	<u>+</u> 10	<u>+</u> 100	nA		
Dynamic			_					
Total Gate Charge	$Q_g$	V <sub>DS</sub> =10V, I <sub>D</sub> =7.4A, V <sub>GS</sub> =4.5V <sup>(Note 1,2)</sup>	-	6.8	-	nC		
Gate-Source Charge	$Q_gs$		-	1.3	-			
Gate-Drain Charge	$Q_gd$		-	2	-			
Input Capacitance	Ciss	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V,	-	513	-	pF		
Output Capacitance	Coss		-	74	-			
Reverse Transfer Capacitance	Crss	f=1.0MHZ	-	60	-			
Switching								
Turn-On Delay Time	td <sub>(on)</sub>	101/1 7.44	-	7	-	ns		
Turn-On Rise Time	tr	$V_{DD}$ =10V, $I_{D}$ =7.4A, $V_{GS}$ =4.5V, $R_{G}$ =6 $\Omega$ (Note 1,2)	-	57	-			
Turn-Off Delay Time	td <sub>(off)</sub>		-	24	-			
Turn-Off Fall Time	tf		-	14	-			
Drain-Source Diode								
Maximum Continuous Drain-Source Diode Forward Current	Is		-	-	2.0	А		
Diode Forward Voltage	$V_{SD}$	I <sub>S</sub> =1.0A, V <sub>GS</sub> =0V	-	0.69	1.2	V		

#### NOTES:

- 1. Pulse width<300us, Duty cycle<2%
- 2. Essentially independent of operating temperature typical characteristics.
- 3. R<sub>OJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper
- 4. The maximum current rating is package limited





#### **TYPICAL CHARACTERISTIC CURVES**

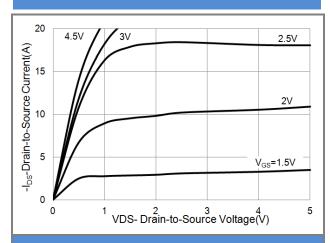
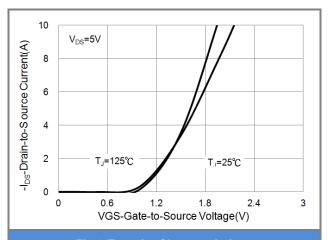


Fig.1 On-Region Characteristics



**Fig.2 Transfer Characteristics** 

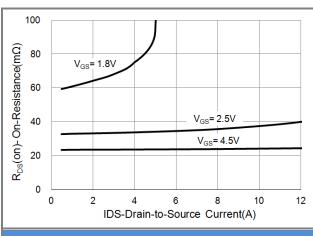


Fig.3 On-Resistance vs. Drain Current

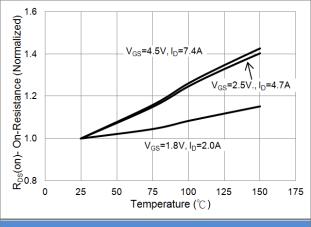


Fig.4 On-Resistance vs. Junction temperature

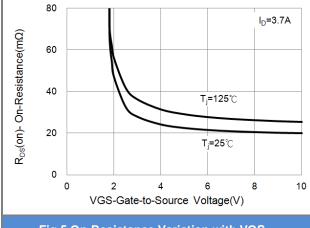


Fig.5 On-Resistance Variation with VGS.

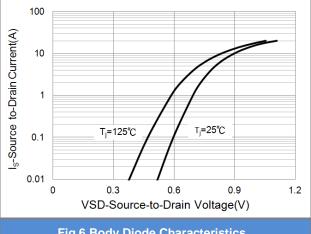
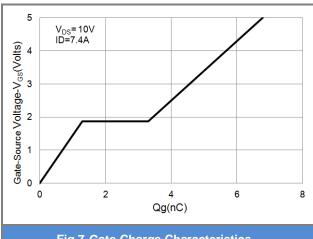


Fig.6 Body Diode Characteristics





#### **TYPICAL CHARACTERISTIC CURVES**



**Fig.7 Gate-Charge Characteristics** 

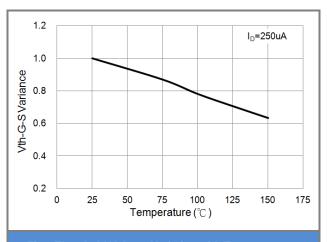


Fig.8 Threshold Voltage Variation with Temperature.

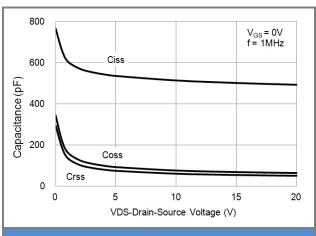


Fig.9 Capacitance vs. Drain-Source Voltage.

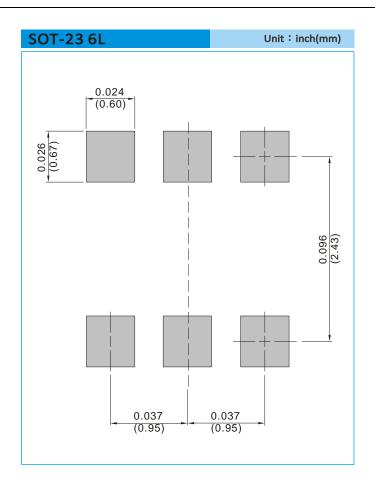




#### PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJS6416_S1_00001	SOT-23 6L	3K pcs / 7" reel	S16	Halogen free
PJS6416_S2_00001	SOT-23 6L	10K pcs / 13" reel	S16	Halogen free

#### **MOUNTING PAD LAYOUT**







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