



# PJL9433

## 60V P-Channel Enhancement Mode MOSFET

**Voltage**

**-60 V**

**Current**

**-3.2 A**

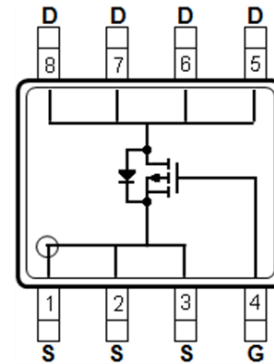
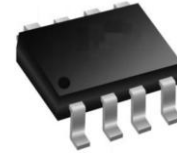
### Features

- $R_{DS(ON)}$ ,  $V_{GS}@-10V, I_D@-3.2A < 115m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@-4.5V, I_D@-1.6A < 160m\Omega$
- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

### Mechanical Data

- Case: SOP-8 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams
- Marking: L9433

SOP-8



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_A=25^\circ\text{C}$	-3.2
		$T_A=70^\circ\text{C}$	-2.5
Pulsed Drain Current <sup>(Note 1)</sup>	$I_{DM}$	-12.8	A
Power Dissipation	$P_D$	$T_A=25^\circ\text{C}$	2.5
		$T_A=70^\circ\text{C}$	1.6
Single Pulse Avalanche Energy <sup>(Note 5)</sup>	$E_{AS}$	8.2	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~150	$^\circ\text{C}$
Typical Thermal resistance	$R_{\theta JA}$	50	$^\circ\text{C/W}$
- Junction to Ambient, $t \leq 10s$ <sup>(Note 6)</sup>			

- Limited only By Maximum Junction Temperature



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## Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-2.0	-2.42	-3.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-3.2A$	-	88	115	m $\Omega$
		$V_{GS}=-4.5V, I_D=-1.6A$	-	120	160	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-55V, V_{GS}=0V$	-	-0.01	-1.0	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	$\pm 10$	$\pm 100$	nA
<b>Dynamic</b> (Note 7)						
Total Gate Charge	$Q_g$	$V_{DS}=-30V, I_D=-3.2A,$ $V_{GS}=-10V$ (Note 1,2)	-	13.4	-	nC
Gate-Source Charge	$Q_{gs}$		-	3.4	-	
Gate-Drain Charge	$Q_{gd}$		-	3.0	-	
Input Capacitance	$C_{iss}$	$V_{DS}=-30V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	685	-	pF
Output Capacitance	$C_{oss}$		-	63	-	
Reverse Transfer Capacitance	$C_{rss}$		-	29	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=-30V, R_L=10\Omega$ $V_{GS}=-10V, R_G=6.2\Omega$ (Note 1,2)	-	7	-	ns
Turn-On Rise Time	$t_r$		-	40	-	
Turn-Off Delay Time	$t_{d(off)}$		-	23	-	
Turn-Off Fall Time	$t_f$		-	10	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$	---	-	-	-3.2	A
Diode Forward Voltage	$V_{SD}$	$I_S=-1A, V_{GS}=0V$	-	-0.78	-1.0	V

NOTES :

1. Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature  $T_J(\text{MAX})=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .
5. The test condition is  $L=0.1\text{mH}, I_{AS}=12.8A, V_{DD}=25V, V_{GS}=10V$
6.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
7. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

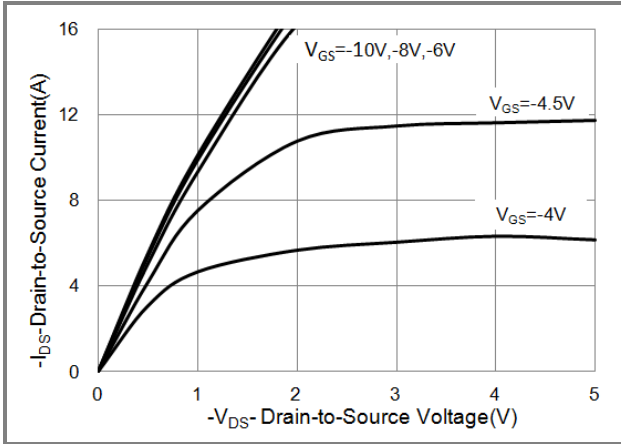


Fig.1 On-Region Characteristics

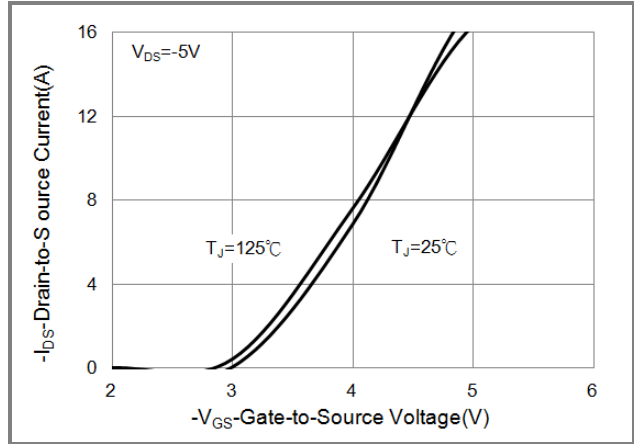


Fig.2 Transfer Characteristics

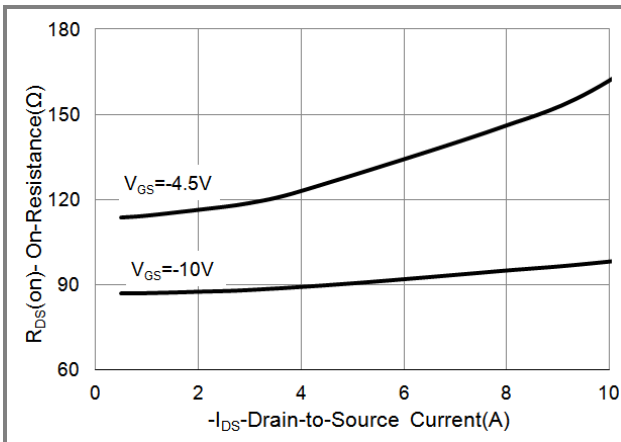


Fig.3 On-Resistance vs. Drain Current

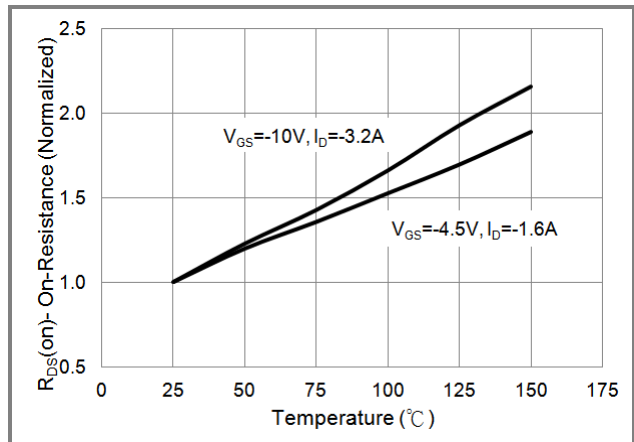


Fig.4 On-Resistance vs. Junction temperature

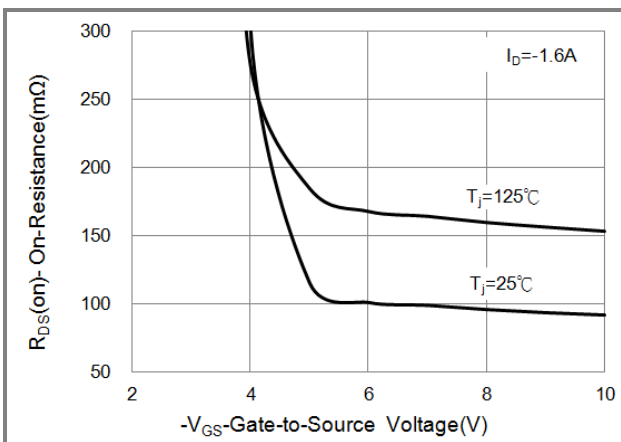


Fig.5 On-Resistance Variation with  $V_{GS}$ .

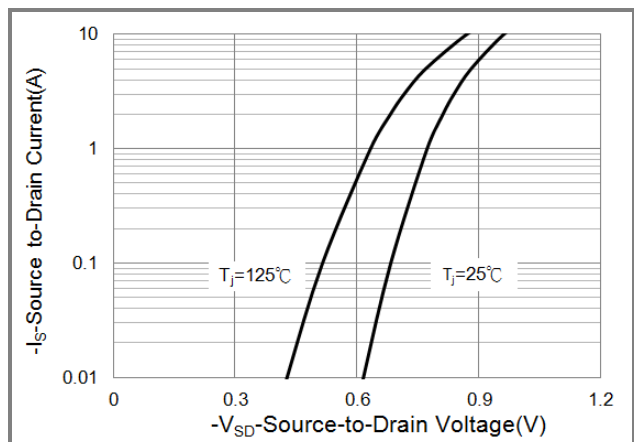


Fig.6 Body Diode Characteristics



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## TYPICAL CHARACTERISTIC CURVES

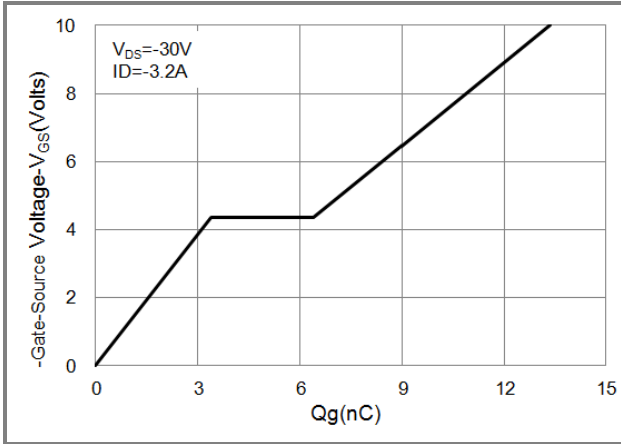


Fig.7 Gate-Charge Characteristics

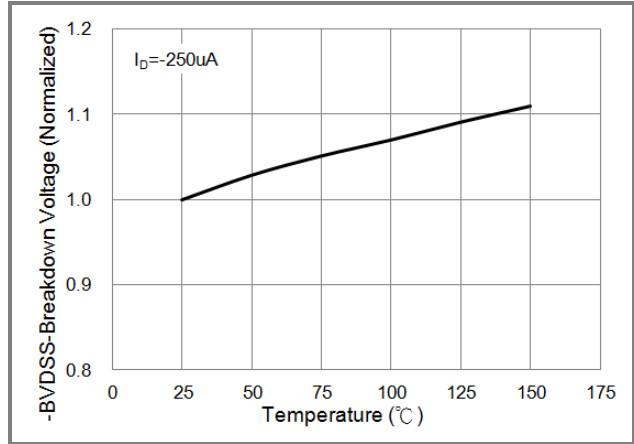


Fig.8 Breakdown Voltage Variation vs. Temperature

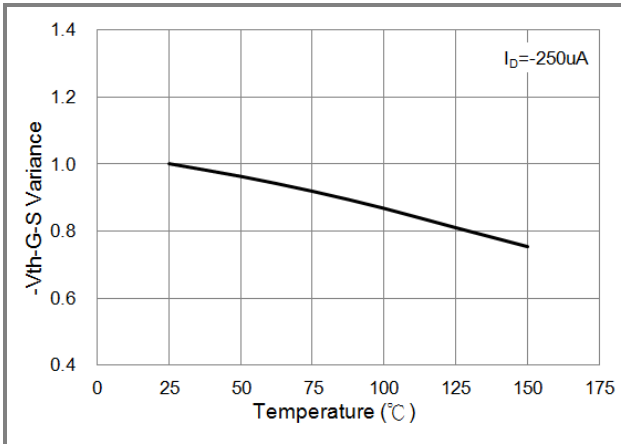


Fig.9 Threshold Voltage Variation with Temperature.

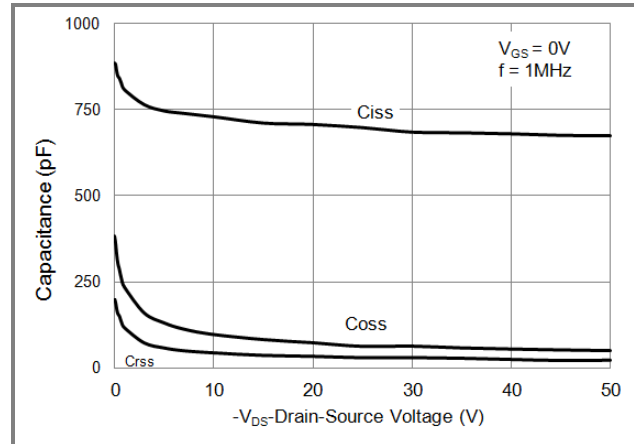


Fig.10 Capacitance vs. Drain-Source Voltage.

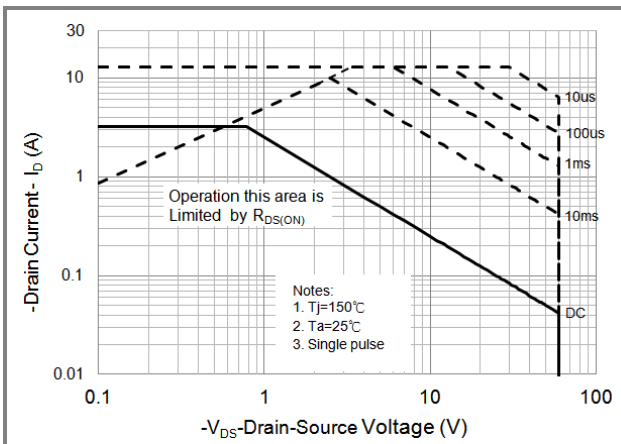


Fig.11 Maximum Safe Operating Area



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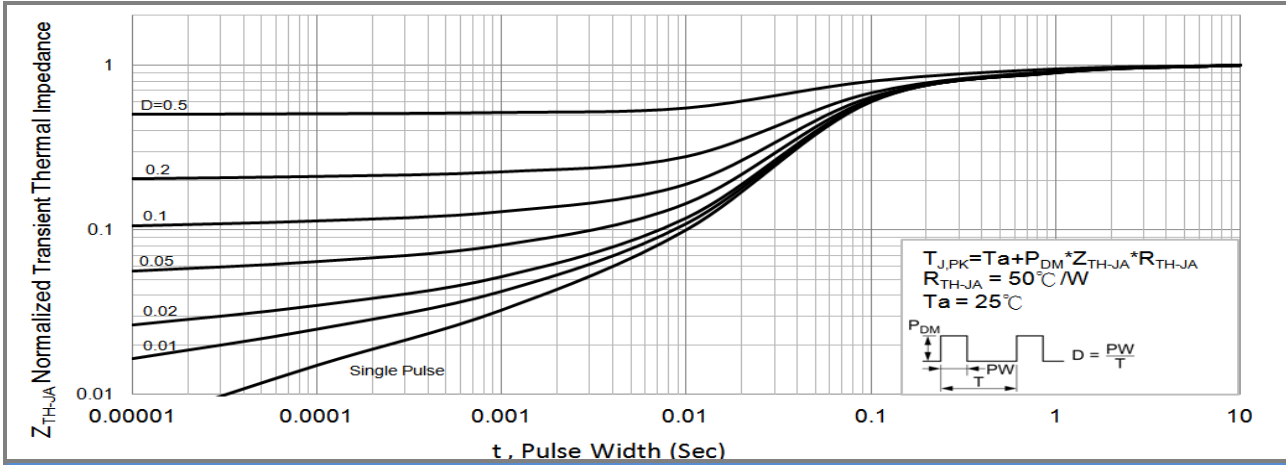


Fig.12 Normalized Thermal Transient Impedance

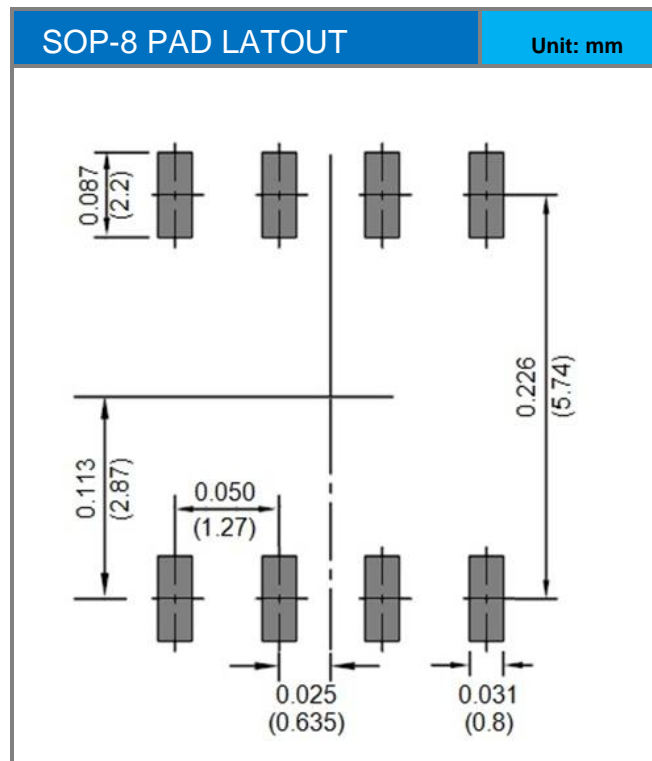
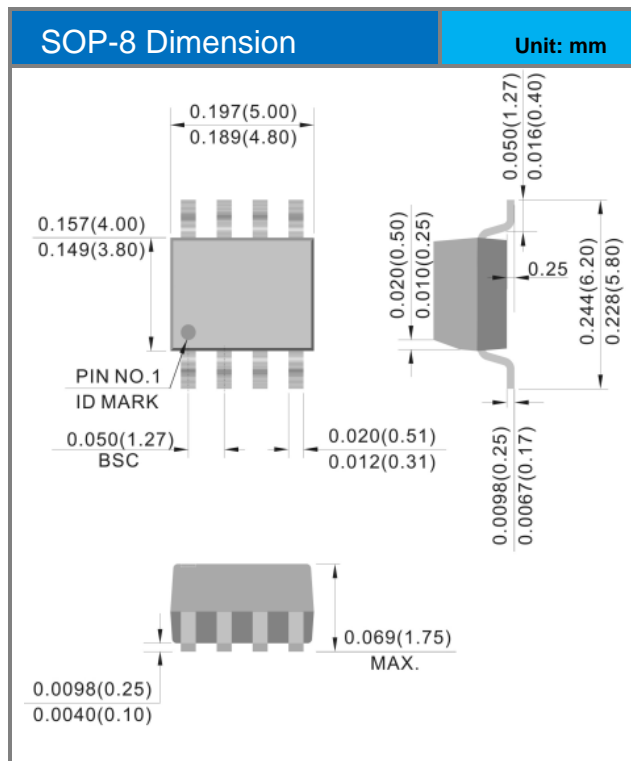


# PJL9433

## PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9433_R2_00001	SOP-8	2.5K pcs / 13" reel	L9433	Halogen free

## Packaging Information & Mounting Pad Layout





## PJL9433

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