



30V P-Channel Enhancement Mode MOSFET

Voltage

-30 V

Current

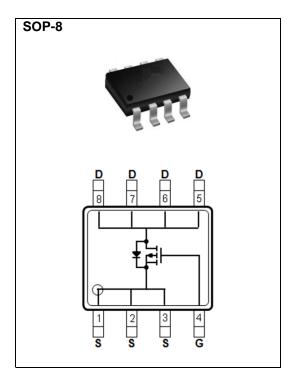
-6 A

Features

- $\begin{array}{l} \bullet \ \ R_{DS(ON)} \ , \ V_{GS}@\text{-}10V, \ I_{D}@\text{-}4A{<}30m\Omega \\ \bullet \ \ R_{DS(ON)} \ , \ V_{GS}@\text{-}4.5V, \ I_{D}@\text{-}2A{<}45m\Omega \end{array}$
- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS2.0 (2011/65/EU & 2015/865/EU directive)
- Green molding compound as per IEC61249 Std.. (Halogen Free)

Mechanical Data

- Case: SOP-8 package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams



Maximum Ratings and Thermal Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER		LIMIT	UNITS	
Drain-Source Voltage		-30	V	
Gate-Source Voltage		<u>+</u> 20	V	
T _A =25°C		-6.0		
T _A =70°C	I _D	-4.8	Α	
Pulsed Drain Current (Note 1)]	
T _A =25°C		1.7	W	
T _A =70°C	\Box P_{D}	1.1		
Operating Junction and Storage Temperature Range		-55~150	°C	
Typical Thermal Resistance - Junction to Ambient (Note 5)		73.5	°C/W	
	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$ $T_A=25^{\circ}C$ $T_A=70^{\circ}C$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	





Electrical Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS	
Static							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V,I _D =-250uA	-30	-	-	V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_{D}=-250uA$	-1.0	-1.6	-2.5		
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V,I _D =-4A	-	26	30	mΩ	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-4.5V,I _D =-2A	-	36	45		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V,V _{GS} =0V	-	-	-1.0	uA	
Gate-Source Leakage Current	I _{GSS}	V _{GS} = <u>+</u> 20V,V _{DS} =0V	-	-	<u>+</u> 100	nA	
Dynamic (Note 6)							
Total Gate Charge	Q_g	V _{DS} =-15V, I _D =-5A, V _{GS} =-4.5V (Note 1,2)	-	7.8	-	nC	
Gate-Source Charge	Q_gs		-	2.7	-		
Gate-Drain Charge	Q_gd		-	2.8	-		
Input Capacitance	Ciss	V _{DS} =-15V, V _{GS} =0V, f=1.0MHZ	-	870	-	pF	
Output Capacitance	Coss		-	130	-		
Reverse Transfer Capacitance	Crss		-	93	-		
Turn-On Delay Time	td _(on)	\/ 45\/\ID 44	-	6.5	-	ns	
Turn-On Rise Time	tr	V_{DS} =-15V,ID=-1A, V_{GS} =-10V, R_{G} =6 Ω (Note 1,2)	-	8.8	-		
Turn-Off Delay Time	td _(off)		-	73	-		
Turn-Off Fall Time	tf		-	44	-		
Drain-Source Diode							
Maximum Continuous Drain-Source					9-	А	
Diode Forward Current	I _S		_	-	-6		
Diode Forward Voltage	V_{SD}	I _S =-1A, V _{GS} =0V	-	-0.75	-1.0	V	

NOTES:

- 1. Pulse width<300us, Duty cycle<2%
- 2. Essentially independent of operating temperature typical characteristics.
- 3. The maximum current rating is package limited.
- 4. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
- 5. Rejah is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 6. Guaranteed by design, not subject to production testing.





TYPICAL CHARACTERISTIC CURVES

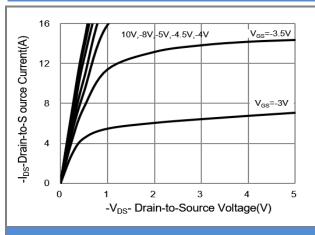


Fig.1 On-Region Characteristics

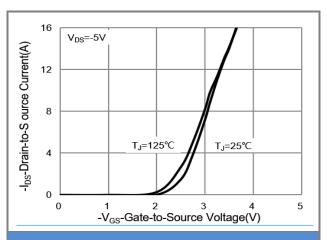


Fig.2 Transfer Characteristics

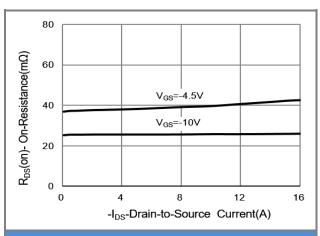


Fig.3 On-Resistance vs. Drain Current

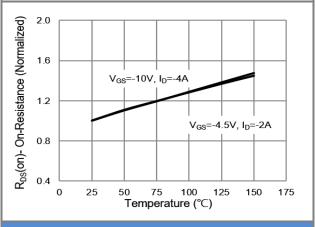
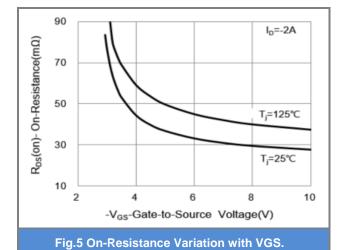
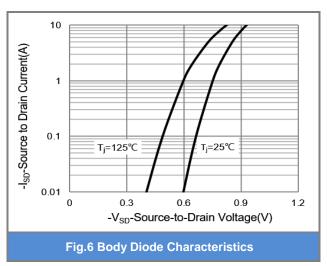


Fig.4 On-Resistance vs. Junction temperature









TYPICAL CHARACTERISTIC CURVES

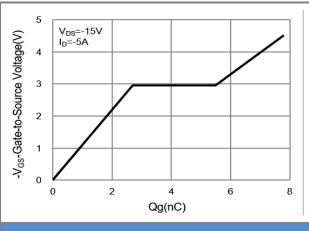


Fig.7 Gate-Charge Characteristics

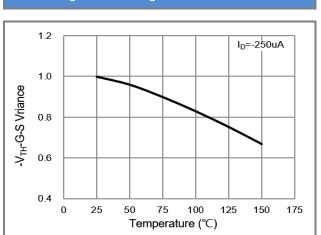


Fig.9 Threshold Voltage Variation with Temperature.

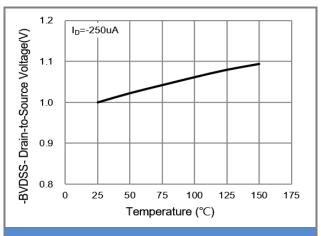


Fig.8 Breakdown Voltage Variation vs. Temperature

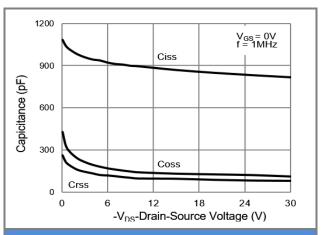


Fig.10 Capacitance vs. Drain-Source Voltage.

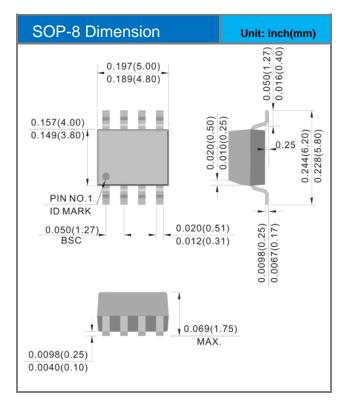


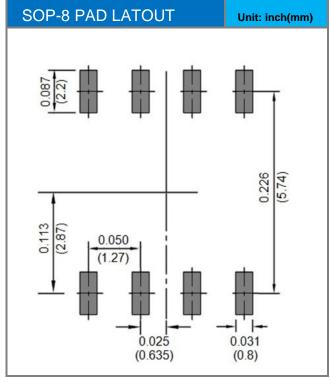


Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJL9409_R2_00001	SOP-8	2.5K pcs / 13" reel	L9409	Halogen free

Packaging Information & Mounting Pad Layout









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