CMOSTEK

CMT2180APW

240 – 480 MHz SoC OOK Transmitter

Features

- High-Performance RISC Microcontroller Core
  - Compatible with MCU such as EM78P153, FM8P53
  - All Single-Cycle Instructions Except Branches
  - Up to 8 MHz Clock
  - Multiple Interruption Supported
  - 49 Bytes SRAM / 1024 Words OTP ROM
- High-Performance OOK Transmitter
  - All Features Programmable on the RFPDK
  - 240 to 480 MHz, OOK Modulation
  - Symbol Rate: up to 30 kbps for OOK
  - Configurable Single-Ended or Differential PA Output
  - Output Power: -10 to +13 dBm
- Supply Voltage: 2.3 to 3.6 V
- 1-pin Crystal
- FCC / ETSI Compliant
- RoHS Compliant
- 14-pin SOP Package

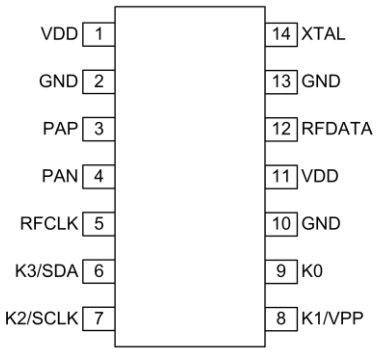
Applications

- Remote Keyless Entry (RKE)
- Garage and gate door openers
- Home/Building Automation and Security
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Consumer Electronics Applications

Ordering Information

Part Number	Frequency	Package Option	MOQ
CMT2180APW-ESR	433.92 MHz	T&R	2,500 pcs
CMT2180APW-ESB	433.92 MHz	Tube	1,000 pcs
More Ordering Info: See Page 37			

SOP14



CMT2180APW

Descriptions

The CMT2180APW is a fully integrated, highly flexible, high performance, SoC OOK transmitter with an embedded RISC microcontroller core for various 240 to 480 MHz wireless applications. It is part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The device includes a 1024-word OTP ROM for programming the user's application, supports up to 4 push buttons to implement the user defined functions. All the device features (such as frequency, output power, WDT, Security and etc.) and programs can be burned into the device using the CMOSTEK USB Programmer and RFPDK. The CMT2180APW uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the BOM counts. The device can deliver up to +13 dBm output power and the PA output can be either single-ended or differential. The device operates from 2.3 V to 3.6 V. Its low power design enables superior operation life for battery powered application. The CMT2180APW transmitter together with CMOSTEK NextGenRF™ receiver enables a highly flexible, low cost RF link.

Typical Application

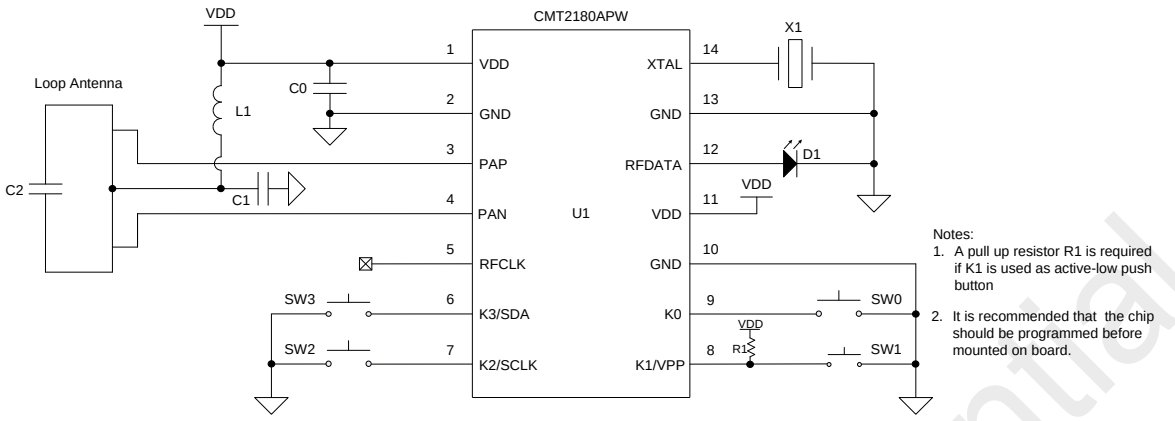


Figure 1. CMT2180APW Typical Application with Differential PA Output

Table 1. BOM of 433.92 MHz Application with Differential PA Output

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2180APW, 240 – 480 MHz SoC OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
R1	±5%, 0402	10	kΩ	
R2	±5%, 0402	470	Ω	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±0.25 pF, 0402 NP0, 50 V	2.2	pF	Murata GRM15
C2	±0.25 pF, 0402 NP0, 50 V	2.2	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	nH	Murata LQG18
D1	D0603, red LED	-	-	-

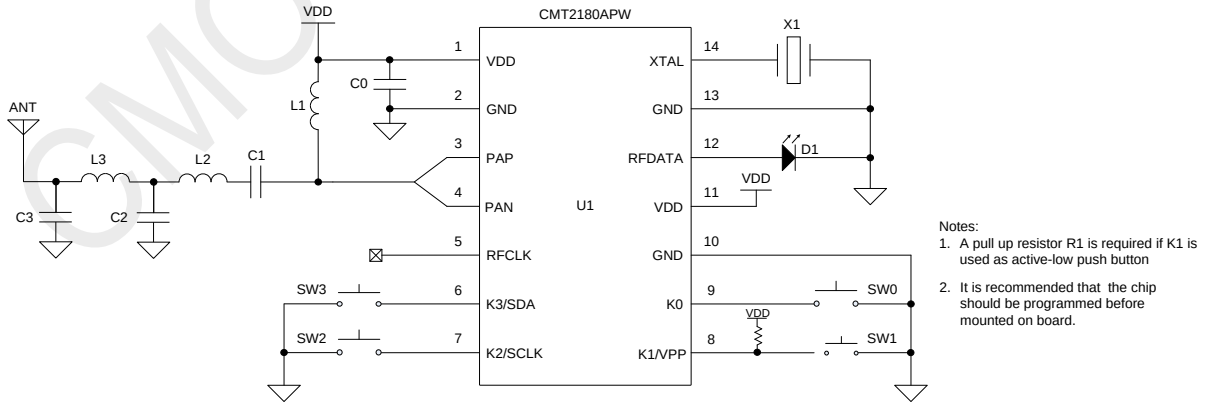


Figure 2. CMT2180APW Typical Application with Single-ended PA Output

Table 2. BOM of 433.92 MHz Application with Single-ended PA Output

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2180APW, 240 – 480 MHz SoC OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
R1	±5%, 0402	10	kΩ	
R2	±5%, 0402	470	Ω	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	15	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	15	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	36	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	18	nH	Murata LQG18
D1	D0603, red LED	-	-	-

Abbreviations

Abbreviations used in this data sheet are described below

AN	Application Notes
BOM	Bill of Materials
BSC	Basic Spacing between Centers
BW	Bandwidth
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
GUI	Graphical User Interface
IC	Integrated Circuit
LDO	Low Drop-Out
Max	Maximum
MCU	Microcontroller Unit
Min	Minimum
MOQ	Minimum Order Quantity
NP0	Negative-Positive-Zero
OBW	Occupied Bandwidth
OOK	On-Off Keying
OTP	One Time Programmable
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PN	Phase Noise
RBW	Resolution Bandwidth
RCLK	Reference Clock
RF	Radio Frequency
RFPDK	RF Product Development Kit
RoHS	Restriction of Hazardous Substances
Rx	Receiving, Receiver
SOT	Small-Outline Transistor
TBD	To Be Determined
Tx	Transmission, Transmitter
Typ	Typical
XO/XOSC	Crystal Oscillator
XTAL	Crystal

Table of Contents

1. Electrical Characteristics

V_{DD} = 3.3 V, T_{OP} = 25 ℃, F_{RF} = 433.92 MHz, OOK modulation, output power is +10 dBm terminated in a matched 50 Ω impedance with single-ended PA output, unless otherwise noted.

1.1 Recommended Operating Conditions

Table 3. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}		2.3		3.6	V
Operation Temperature	T_{OP}		-20		85	℃
Supply Voltage Slew Rate			1			mV/us

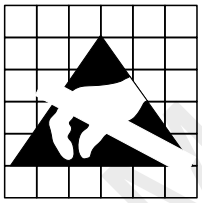
1.2 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Transmitter Specifications

Table 5. Transmitter Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range[1]	F_{RF}		240		480	MHz
Synthesizer Frequency Resolution	F_{RES}			198		Hz
Symbol Rate	SR		0.5		30	ksps
Maximum Output Power[2]	$P_{OUT(Max)}$			+13		dBm
Minimum Output Power	$P_{OUT(Min)}$			-10		dBm
Output Power Step Size	P_{STEP}			1		dB
PA Ramping Time[3]	t_{RAMP}		0		1024	us
Current Consumption, Single-ended	I_{DD-S}	0 dBm, 50% duty cycle, 433.92 MHz		7.7		mA
		+10 dBm, 50% duty cycle, 433.92 MHz		14.4		mA
		+13 dBm, 50% duty cycle, 433.92 MHz		19.1		mA
Current Consumption, Differential	I_{DD-D}	0 dBm, 50% duty cycle, 433.92 MHz		6.3		mA
		+10 dBm, 50% duty cycle, 433.92 MHz		10.5		mA
		+13 dBm, 50% duty cycle, 433.92 MHz		12.2		mA
Sleep Current	I_{SLEEP}			2.5		uA
Frequency Tune Time	t_{TUNE}			370		us
Phase Noise @433.92 MHz	$PN_{433.92}$	100 kHz offset from F_{RF}		-80		dBc/Hz
		200 kHz offset from F_{RF}		-82		dBc/Hz
		400 kHz offset from F_{RF}		-92		dBc/Hz
		600 kHz offset from F_{RF}		-98		dBc/Hz
		1.2 MHz offset from F_{RF}		-107		dBc/Hz
Harmonics Output for 315 MHz[4]	$H2_{315}$	2^{nd} harm @ 630 MHz, +13 dBm P_{OUT}		-60		dBm
	$H3_{315}$	3^{rd} harm @ 945 MHz, +13 dBm P_{OUT}		-65		dBm
Harmonics Output for 433.92 MHz[4]	$H2_{433.92}$	2^{nd} harm @ 867.84 MHz, +13 dBm P_{OUT}		-52		dBm
	$H3_{433.92}$	3^{rd} harm @ 1301.76 MHz, +13 dBm P_{OUT}		-60		dBm
OOK Extinction Ration				60		dB
Occupied Bandwidth @ 315 MHz	F_{OBW315}	Measured @ -20 dBc, RBW = 1 kHz, SR = 1.2 ksps, t_{RAMP} = 256 us		6		kHz
Occupied Bandwidth @ 433.92 MHz	$F_{OBW433.92}$	Measured @ -20 dBc, RBW = 1 kHz, SR = 1.2 ksps, t_{RAMP} = 256 us		7		kHz
Internal RC	IRC	When selecting 4 MHz	3.7	4	4.3	MHz

Notes:

[1]. The frequency range is continuous over the specified range.

[2]. Measured with single-ended PA output, and it is not applicable for when the device is configured as differential PA output.

[3]. 0 and 2^n us, n = 0 to 10, when set to “0”, the PA output power will ramp to its configured value in the shortest possible time.

[4]. The harmonics output is measured with the application shown as Figure 11.

1.4 Crystal Oscillator

Table 6. Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency[1]	F_{XTAL}		26	26	26	MHz
Crystal Tolerance[2]				±20		ppm
Load Capacitance[3]	C_{LOAD}			15		pF
Crystal ESR	Rm				60	Ω
XTAL Startup Time[4]	t_{XTAL}			400		us

Notes:

[1]. The CMT2180APW can directly work with external 26 MHz reference clock input to XTAL pin (a coupling capacitor is required) with amplitude 0.3 to 0.7 Vpp.

[2]. This is the total tolerance including (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

[3]. The required crystal load capacitance is integrated on-chip to minimize the number of external components.

[4]. This parameter is to a large degree crystal dependent.

2. Pin Descriptions

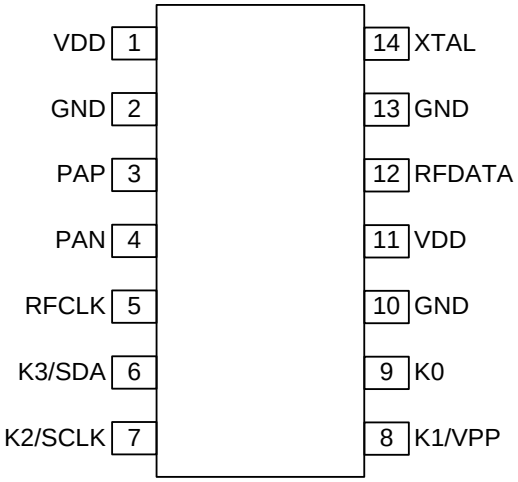


Figure 3. CMT2180APW Pin Assignments

Table 7. CMT2180APW Pin Descriptions

Pin Number	Name	I/O	Descriptions
1	VDD	I	Power supply input
2	GND	I	Ground
3	PAP	O	The differential power amplifier output, when using as singled-ended output, PAN/PAP should be connected together before connect to the matching network
4	PAN	O	
5	RFCLK[1]	I	Clock pin to access the embedded EEPROM
6	K3/SDA[1]	IO	Push button key 3 and Serial programming data for MCU
7	K2/SCLK[1]	IO	Push button key 2 and Serial programming clock for MCU
8	K1/VPP[1]	IO	Push button key 1 (external pull-up resistor needed for active-low push button) and Serial programming voltage for MCU
9	K0[1]	IO	Push button key 0
10	GND	I	Ground
11	VDD	I	Power supply input
12	RFDATA[1]	IO	Data input to be transmit and Data pin to access the embedded EEPROM
13	GND	I	Ground
14	XTAL	I	26 MHz single-ended crystal oscillator input or External 26 MHz reference clock input

Note

[1]. See Table 15 for the mapping from pin names to microcontroller core port names and function descriptions

3. Typical Performance Characteristics

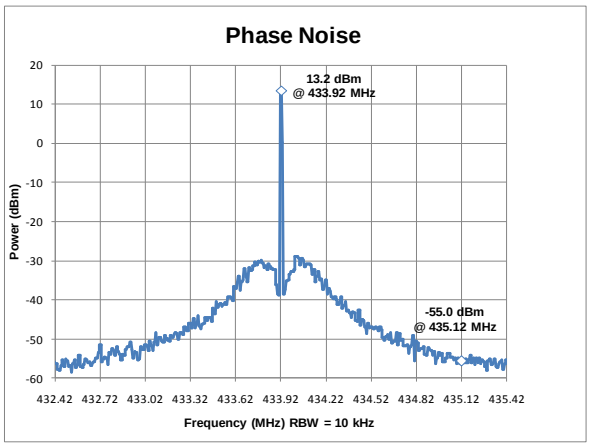


Figure 4. Phase Noise, F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm, Unmodulated

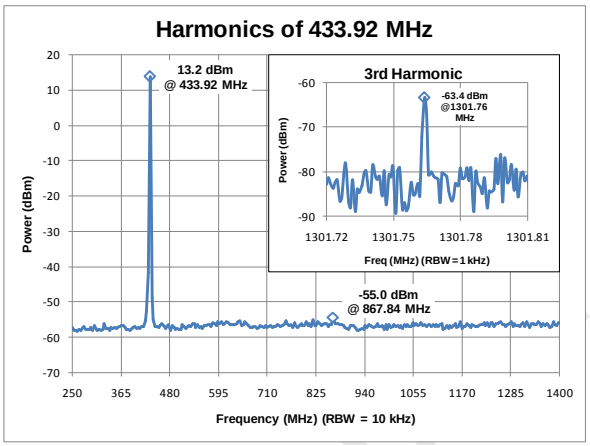


Figure 5. Harmonics of 433.92 MHz, P_{OUT} = +13 dBm

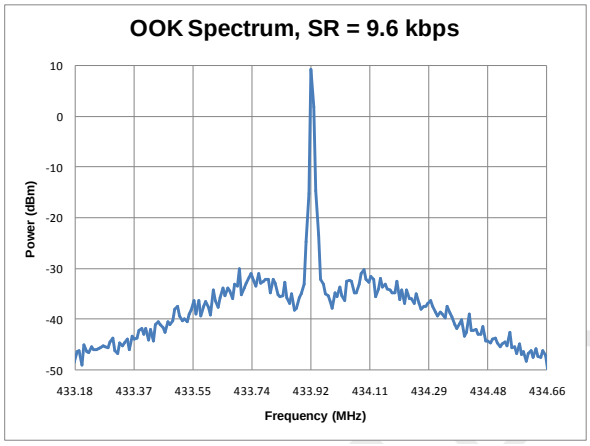


Figure 7. OOK Spectrum, SR = 9.6 ksps, P_{OUT} = +10 dBm, t_{RAMP} = 32 us

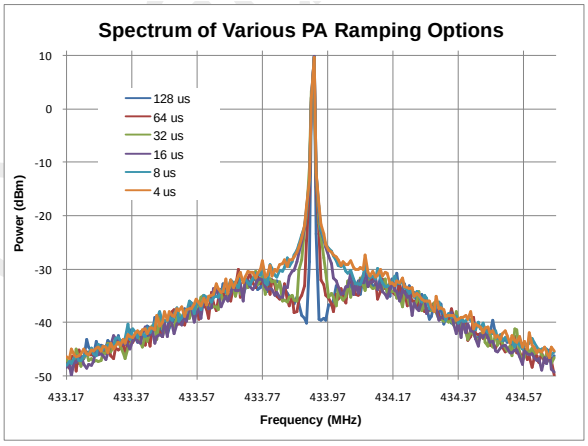


Figure 6. Spectrum of PA Ramping, SR = 9.6 ksps, P_{OUT} = +10 dBm

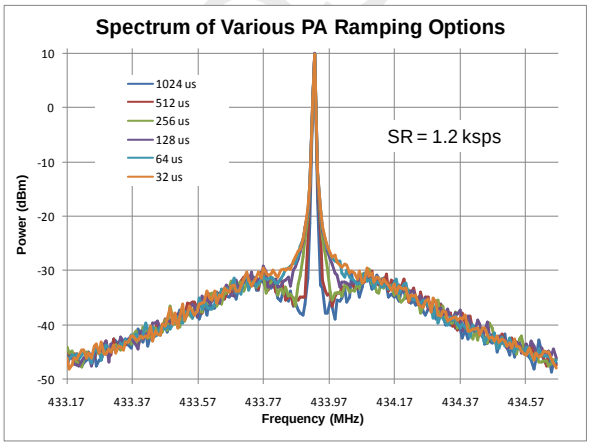


Figure 8. Spectrum of PA Ramping, SR = 1.2 ksps, P_{OUT} = +10 dBm

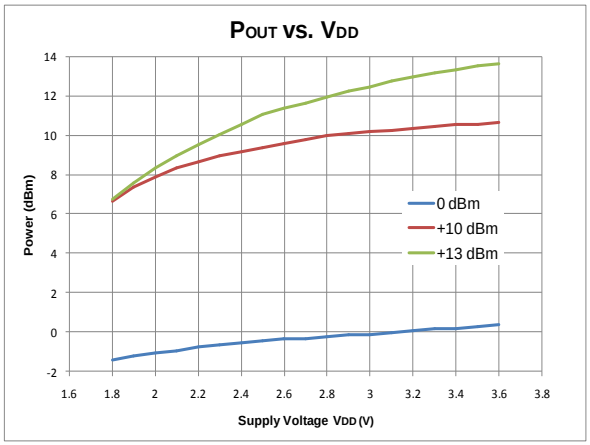


Figure 9. Output Power vs. Supply Voltages, F_{RF} = 433.92 MHz

4. Typical Application Schematics

4.1 Typical Application with Differential PA Output

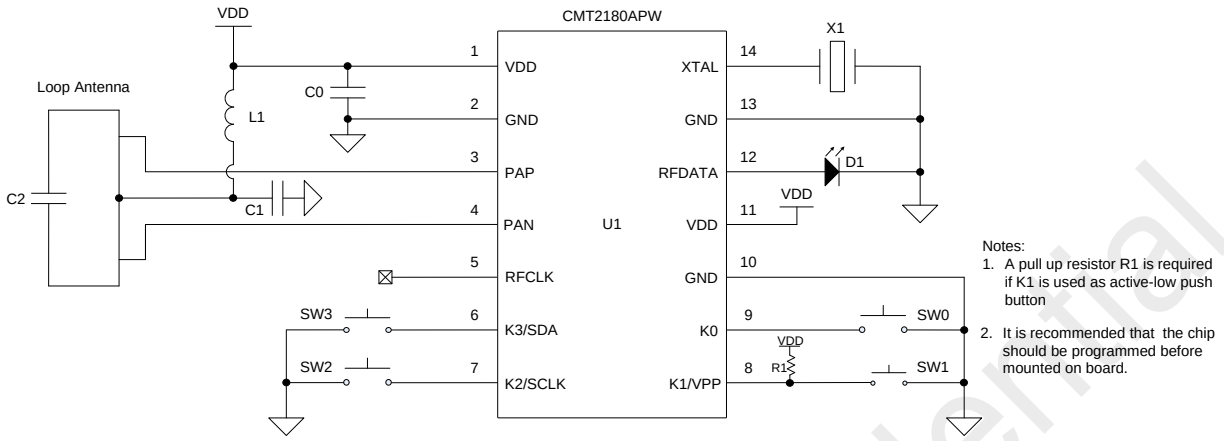


Figure 10. CMT2180APW Typical Application with Differential PA Output

Notes:

1. It is recommended that the chip should be programmed before mounted on board.
2. The general layout guidelines are listed below. For more design details, please refer to “AN131 CMT218xA Schematic and PCB Layout Design Guideline”.
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2180APW as possible for better filtering.
3. The table below shows the BOM of 433.92 Application with Differential PA Output. For the BOM of 315 MHz application, please refer to “AN131 CMT218xA Schematic and PCB Layout Design Guideline”.

Table 8. BOM of 433.92 MHz Application with Differential PA Output

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2180APW, 240 – 480 MHz SoC OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
R1	±5%, 0402	10	kΩ	
R2	±5%, 0402	470	Ω	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±0.25 pF, 0402 NP0, 50 V	2.2	pF	Murata GRM15
C2	±0.25 pF, 0402 NP0, 50 V	2.2	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	nH	Murata LQG18
D1	D0603, red LED	-	-	-

4.2 Typical Application with Single-ended PA Output

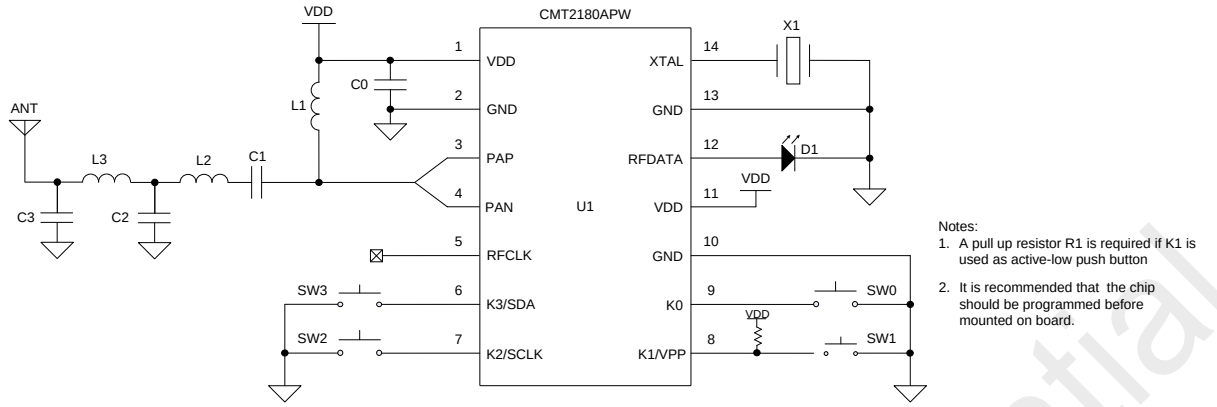


Figure 11. CMT2180APW Typical Application with Single-ended PA Output

Notes:

1. It is recommended that the chip should be programmed before mounted on board.
2. The general layout guidelines are listed below. For more design details, please refer to “AN131 CMT218xA Schematic and PCB Layout Design Guideline”.
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2180APW as possible for better filtering.
3. The table below shows the BOM of 433.92 Application with single-ended PA output. For the BOM of 315 MHz applications, please refer to “AN131 CMT218xA Schematic and PCB Layout Design Guideline”.

Table 9. BOM of 433.92 MHz FCC/ETSI Compliant Application

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2180APW, 240 – 480 MHz SoC OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
R1	±5%, 0402	10	kΩ	
R2	±5%, 0402	470	Ω	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	15	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	15	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	36	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	18	nH	Murata LQG18
D1	D0603, red LED	-	-	-

5. Functional Descriptions

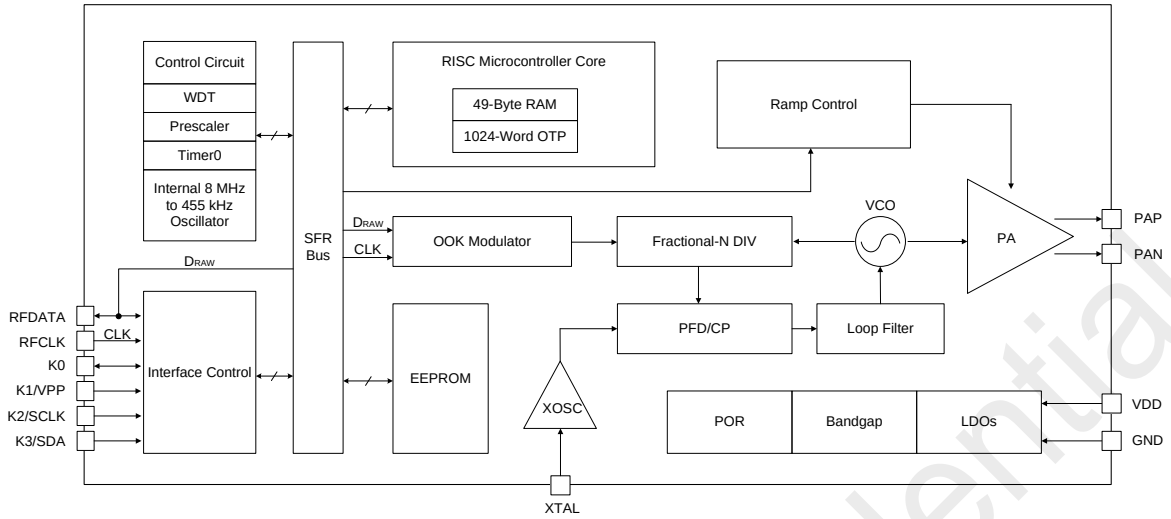


Figure 12. CMT2180APW Functional Block Diagram

5.1 Overview

The CMT2180APW devices are fully integrated, highly flexible, high performance, SoC OOK transmitters with embedded RISC microcontroller core for various 240 to 480 MHz wireless applications. They are part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design.

The functional block diagram of the CMT2180APW is shown in the figure above. The CMT2180APW is based on direct synthesis of the RF frequency, and the frequency is generated by a low-noise fractional-N frequency synthesizer. It uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. Every analog block is calibrated on each Power-on Reset (POR) to the reference voltage generated by Bandgap. The calibration can help the chip to finely work under different temperatures and supply voltages. The CMT2180APW has a highly efficient PA built in, the PA can be configured as single-ended or differential outputs, and the output power can be configured from -10 to +13 dBm in 1 dB step size. The RISC microcontroller core provides the core functionality of the CMT2180APW. A 1024-word of OTP area is available to store the user program of the applications. Up to 4 push buttons are supported with their function customized by the user program. RF Frequency, PA output power, other product features and unique transmit IDs can be programmed into the embedded EEPROM by the RFPDK and USB Programmer. This saves the cost and simplifies the product development and manufacturing effort. The CMT2180APW operates from 2.3 to 3.6 V, only consumes 10.5 mA when transmitting +10 dBm power under 3.3 V supply voltage. The device together with CMOSTEK NextGenRF™ receiver enables a highly flexible, low cost RF link.

5.2 Modulation, Frequency and Symbol Rate

The CMT2180APW supports OOK modulation with the symbol rate up to 30 ksps. The CMT2180APW continuously covers the frequency range from 240 to 480 MHz, including the license free ISM frequency band around 315 MHz and 433.92 MHz. The device contains a high spectrum purity low power fractional-N frequency synthesizer with output frequency resolution better than 198 Hz within the supported frequency range. See the table below for the modulation, frequency and symbol rate specifications.

Table 10. Modulation, Frequency and Symbol Rate

Parameter	Value	Unit
Modulation	OOK	-
Frequency	240 to 480	MHz
Frequency Resolution	<198	Hz
Symbol Rate	0.5 to 30	ksps

5.3 Embedded OTP / EEPROM and RFPDK

The RFPDK (RF Products Development Kit) is a very user-friendly software tool delivered for the user configuring the CMT2180APW in the most intuitional way. The user only needs to fill in/select the proper value of each parameter and click the "Burn" button to complete the chip configuration. No register access and control is required in the application program. See the figure below for the accessing of the EEPROM and Table 11 for the summary of all the configurable parameters of the CMT2180APW in the RFPDK.

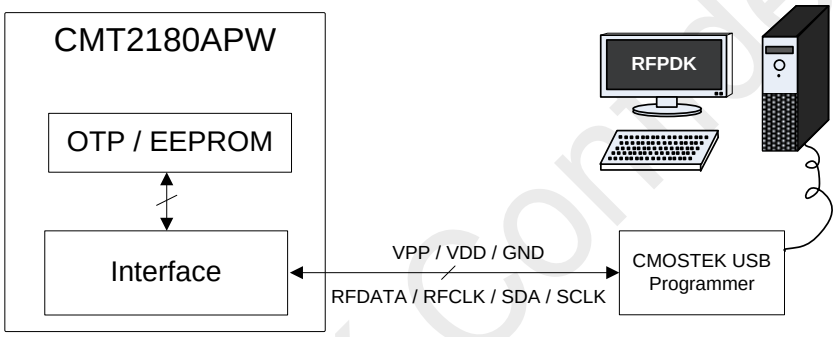


Figure 13. Accessing Embedded OTP / EEPROM

For the detail of CMT2180APW configurations with the RFPDK, please refer to "AN132 CMT2180/89A Configuration Guideline".

Table 11. Configurable Parameters in RFPDK

Category	Parameters	Descriptions	Default	Mode
RF Settings	Frequency	To input a desired transmitting radio frequency in the range from 240 to 480 MHz. The step size is 0.001 MHz.	433.92 MHz	Basic Advanced
	Tx Power	To select a proper transmitting output power from -10 dBm to +14 dBm, 1 dB margin is given above +13 dBm.	+13 dBm	Basic Advanced
	Xtal Load	On-chip XOSC load capacitance options: from 10 to 22 pF. The step size is 0.33 pF.	15.00 pF	Basic Advanced
	PA Ramping	To control PA output power ramp up/down time, options are 0 and 2^n us (n from 0 to 10).	0 us	Advanced
	PA Output	To select the PA output mode, the option is Single-ended or Differential.	Differential	Basic Advanced
Transmitting Settings	Start by	Start condition of a transmitting cycle, by Data Pin Rising Edge.	Data Pin Rising Edge	Advanced

Category	Parameters	Descriptions	Default	Mode
	Stop by	Stop condition of a transmitting cycle, by Data Pin Holding Low for 20 to 90 ms.	Data Pin Holding Low for 20 ms	Advanced
SN Settings	Start Addr (Hex)	Defines the starting address of a consecutive address space in the OTP ROM to store the series number.	0008	Basic Advanced
	End Addr (Hex)	Defines the ending address to store the series number to the OTP ROM.	000A	Basic Advanced
	Init SN	Defines the initial SN value (in Dec), this value will be stored in the OTP ROM with address defined from Start Addr (Hex) to End Addr (Hex).	1193046	Basic Advanced
	Step Size	Defines the incremental step size of the SN value, it can be a positive integer or zero.	1	Basic Advanced
	Current SN	Displays the next SN value to be burned into the device in the next burning operation.	1193046	Basic Advanced
Feature Bits	Clock Source	To select the internal clock source for the microcontroller, the options are: 4MHz, 8 MHz, 1MHz and 455 kHz.	4 MHz	Basic Advanced
	Clock Div	To select the divided ratio of the system clock for the microcontroller, the options are Clock/4, Clock/2 and Clock/8,	Clock/4	Basic Advanced
	Security	To enable or disable the code protection. When it is enabled, the readouts of bit11-7, bit4-0 in each word are fixed at 1. The options are Disable or Enable.	Enable	Basic Advanced
	WDT	To enable or disable the watchdog timer, the options are Enable or Disable.	Disable	Basic Advanced
	K1/MCLR	To configure the K1 pin as Master Clear (MCLR) or push button key.	K1	Basic Advanced
	PED	Defines the power edge detection threshold, the options are: Low Level, Mid Level, High Level and Disable	Low Level	Basic Advanced
ID Memory Settings	-	This is a 12 x 7-bit ID area in the microcontroller section that allows the user to store any data.	-	Basic Advanced
Key Settings	Start Addr (Hex)	Defines the starting address of a consecutive address space in the OTP ROM to store the Key.	3F0	Basic Advanced
	End Addr (Hex)	Defines the ending address in the OTP ROM to store the Key	3F7	Basic Advanced
	Key(Hex)	Defines the Key in the OTP ROM	1234567890ABCDEF	Basic Advanced

5.4 Power Amplifier

A highly efficient Power Amplifier (PA) is integrated in the CMT2189A to transmit the modulated signal out. Depending on the application, the PA can be configured as single-ended or differential output on the RFPDK, and the user can design a matching network for the PA to exhibit optimum efficiency at the desired output power for a wide range of antennas, such as loop or monopole antenna. Typical application schematics and the required BOM are shown in “Chapter 4 Typical Application

Schematic". For the schematic, layout guideline and the other detailed information please refer to "AN131 CMT218xA Schematic and PCB Layout Design Guideline".

The output power of the PA can be configured by the user within the range from -10 dBm to +13 dBm in 1 dB step size using the CMOSTEK USB Programmer and the RFPDK.

5.5 PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter or spurs in the output spectrum around the desired carrier frequency. By gradually ramping the PA on and off, PA transient spurs are minimized. The CMT2180APW has built-in PA ramping configurability with options of 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024 us, as shown in Figure 14. When the option is set to "0", the PA output power will ramp up to its configured value in the shortest possible time. The ramp down time is identical to the ramp up time in the same configuration.

CMOSTEK recommends that the maximum symbol rate should be no higher than 1/2 of the PA ramping "rate", as shown in the formula below.

$$SR_{Max} \leq 0.5 * (\frac{1}{t_{RAMP}})$$

In which the PA ramping "rate" is given by ($1/t_{RAMP}$). In other words, by knowing the maximum symbol rate in the application, the PA ramping time can be calculated by formula below.

$$t_{RAMP} \leq 0.5 * (\frac{1}{SR_{MAX}})$$

The user can select one of the values of the t_{RAMP} in the available options that meet the above requirement. If somehow the t_{RAMP} is set to be longer than "0.5 * ($1/SR_{Max}$)", it will possibly bring additional challenges to the OOK demodulation of the Rx device. For more detail of calculating t_{RAMP}, please refer to "AN132 CMT2180/89A Configuration Guideline".

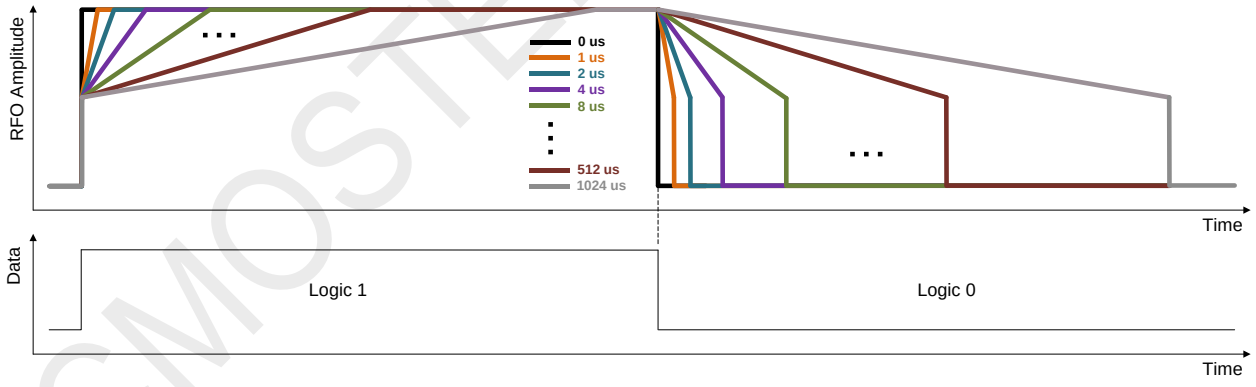


Figure 14. PA Ramping Time

5.6 Crystal Oscillator and RCLK

The CMT2180APW uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip. Figure 16 shows the configuration of the XTAL circuitry and the crystal model. The recommended specification for the crystal is 26 MHz with ±20 ppm, ESR (Rm) < 60 Ω, load capacitance C_{LOAD} of 15 pF. To save the external load capacitors, a set of variable load capacitors C_L is built inside the CMT2180APW to support the oscillation of the crystal.
The value of load capacitors is configurable with the CMOSTEK USB Programmer and RFPDK. To achieve the best performance, the user only needs to input the desired value of the XTAL load capacitance C_{LOAD} of the crystal (can be found in the datasheet of the crystal) to the RFPDK, then finely tune the required XO load capacitance according to the actual XO

frequency.

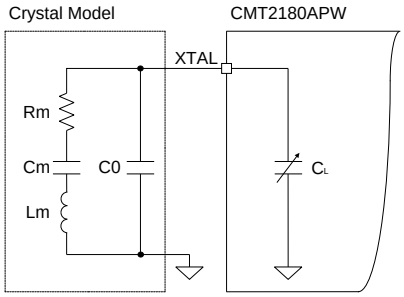


Figure 16. XTAL Circuitry and Crystal Model

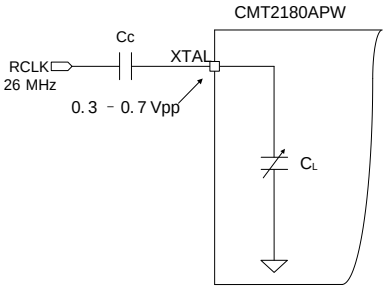


Figure 15. RCLK Circuitry

If a 26 MHz RCLK (reference clock) is available in the system, the user can directly use it to drive the CMT2180APW by feeding the clock into the chip via the XTAL pin. This further saves the system cost due to the removal of the crystal. A coupling capacitor is required if the RCLK is used. The recommended amplitude of the RCLK is 0.3 to 0.7 Vpp on the XTAL pin. Also, the user should set the internal load capacitor C_L to its minimum value. See Figure 15 for the RCLK circuitry.

6. Working States and Control Interface

6.1 Working States

The CMT2180APW has following 4 different working states: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

SLEEP

When the CMT2180APW is in the SLEEP state, all the internal blocks are turned off and the current consumption is minimized. The 4 push buttons keys are ready to sense valid pressing actions to start a transmitting cycle.

XO-STARTUP

Once the modulator of the CMT2180APW detect valid signal on the D_{RAW} wire (see Figure 12), the RF section will go into the XO-STARTUP state, and the internal XO starts to work. The user has to wait for the t_{XTAL} to allow the XO to get stable. The t_{XTAL} is to a large degree crystal dependent. A typical value of t_{XTAL} is provided in the Table 12.

TUNE

The frequency synthesizer will tune the CMT2180APW to the desired frequency in the time t_{TUNE}. The PA can be turned on to transmit the data only after the TUNE state is done, before that the data will not be transmitted.

TRANSMIT

The CMT2180APW starts to modulate and transmit the data (D_{RAW}) generated by the microcontroller core responding to the push buttons. The transmission can be ended in 2 methods: firstly, driving the DATA pin low for t_{STOP} time, where the t_{STOP} can be configured from 20 to 90 ms on the RFPDK; secondly, issuing SOFT_RST command over the two-wire interface, this will stop the transmission in 1 ms. See section 6.2.2 for details of the two-wire interface.

Table 12.Timing in Different Working States

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	t_{XTAL}		400		us
Time to Tune to Desired Frequency	t_{TUNE}		370		us
Hold Time After Rising Edge	t_{HOLD}	10			ns
Time to Stop The Transmission[2]	t_{STOP}	20		90	ms
Notes: [1]. This parameter is to a large degree crystal dependent. [2]. Configurable from 20 to 90 ms in 10 ms step size.					

6.2 Transmission Control Interface

The CMT2180APW uses the D_{RAW} wire for the microcontroller core to send in data for modulation and transmission. The D_{RAW} wire, which also connects to the DATA pin, can be used as pin for EEPROM programming, data transmission, as well as controlling the transmission. The transmission can be started by detecting rising or falling edge on the D_{RAW} wire (DATA Pin), and stopped by driving the D_{RAW} wire low for t_{STOP} as shown in the table above. Besides communicating over the D_{RAW} wire, the microcontroller core can also communicate with the RF section over the two-wire interface, so that the transmission is more robust, and consumes less current.

Please note that the user is recommended to use the Tx Enabled by DATA pin Rising Edge.

6.2.1 Tx Enabled by DATA Pin Rising Edge

As shown in the figure below, once the CMT2180APW detects a rising edge on the D_{RAW} wire (DATA pin), it goes into the XO-STARTUP state. The user has to pull the D_{RAW} wire high for at least 10 ns (t_{HOLD}) after detecting the rising edge, as well as wait for the sum of t_{XTAL} and t_{TUNE} before sending any useful information (data to be transmitted) into the chip on the D_{RAW} wire. The logic state of the D_{RAW} wire is “Don't Care” from the end of t_{HOLD} till the end of t_{TUNE}. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the D_{RAW} wire low for t_{STOP} in order to end the transmission.

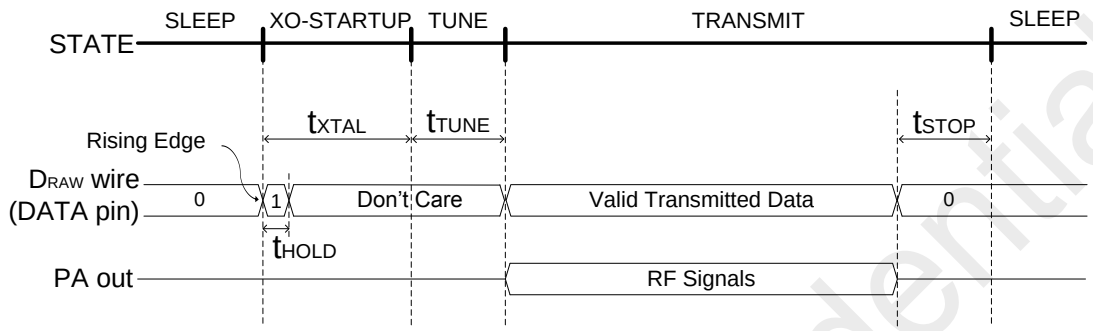


Figure 17. Transmission Enabled by DATA Pin Rising Edge

6.2.2 Two-wire Interface

For power-saving and reliable transmission purposes, the CMT2180APW RF part is recommended to communicate with the microcontroller core over a two-wire interface (TWI): D_{RAW} (RFDATA) and RFCLK. The TWI is designed to operate at a maximum of 1 MHz. The timing requirement and data transmission control through the TWI are shown in this section.

Table 13. TWI Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input Level High	V_{IH}		0.8			V_{DD}
Digital Input Level Low	V_{IL}				0.2	V_{DD}
RFCLK Frequency	F_{CLK}		10		1,000	kHz
RFCLK High Time	t_{CH}		500			ns
RFCLK Low Time	t_{CL}		500			ns
RFCLK Delay Time	t_{CD}	RFCLK delay time for the first falling edge of the TWI_RST command.	20		15,000	ns
RFDATA Delay Time	t_{DD}	The data delay time from the last RFCLK rising edge of the TWI command to the time RFDATA return to default state			15,000	ns
RFDATA Setup Time	t_{DS}	From RFDATA change to RFCLK falling edge	20			ns
RFDATA Hold Time	t_{DH}	From RFCLK falling edge to RFDATA change	200			ns

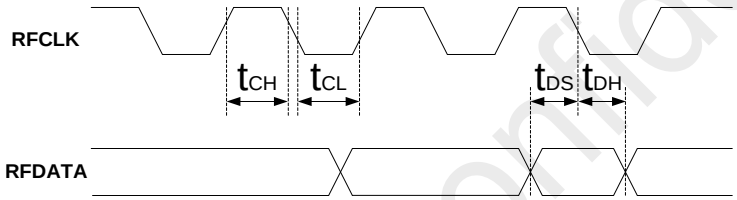


Figure 18. Two-wire Interface Timing Diagram

Once the device is powered up, TWI_RST and SOFT_RST should be issued to make sure the device works in SLEEP state robustly. On every transmission, TWI_RST and TWI_OFF should be issued before the transmission to make sure the TWI circuit functions correctly. TWI_RST and SOFT_RST should be issued again after the transmission for the device going back to SLEEP state reliably till the next transmission. The operation flow with TWI is shown as the figure below.

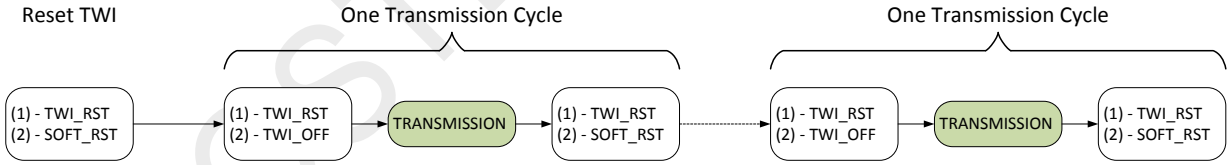


Figure 19. CMT21810APW Operation Flow with TWI

Table 14. TWI Commands Descriptions

Command	Descriptions
TWI_RST	Implemented by pulling the RFDATA pin low for 32 clock cycles and clocking in 0x8D00, 48 clock cycles in total. It only resets the TWI circuit to make sure it functions correctly. The RFDATA pin cannot detect the Rising/Falling edge to trigger transmission after this command, until the TWI_OFF command is issued. **Notes:** a) Please ensure the RFDATA pin is firmly pulled low during the first 32 clock cycles. b) When the device is configured as Transmission Enabled by RFDATA Pin Falling Edge, in order to

Command	Descriptions
	issue the TWI_RST command correctly, the first falling edge of the RFCLK should be sent t_{CD} after the RFDATA falling edge, which should be longer than the minimum RFDATA setup time 20 ns, and shorter than 15 us. c) When the device is configured as Transmission Enabled by RFDATA Pin Rising Edge, the default state of the RFDATA is low, there is no t_{CD} requirement, as shown in Figure 20.
TWI_OFF	Implemented by clocking in 0x8D02, 16 clock cycles in total. It turns off the TWI circuit, and the RFDATA pin is able to detect the Rising/Falling edge to trigger transmission after this command, till the TWI_RST command is issued. The command is shown as Figure 21.
SOFT_RST	Implemented by clocking in 0xBD01, 16 clock cycles in total. It resets all the other circuits of the chip except the TWI circuit. This command will trigger internal calibration for getting the optimal device performance. After issuing the SOFT_RST command, the host MCU should wait 1 ms before sending in any new command. After that, the device goes to SLEEP state. The command is shown as Figure 22.

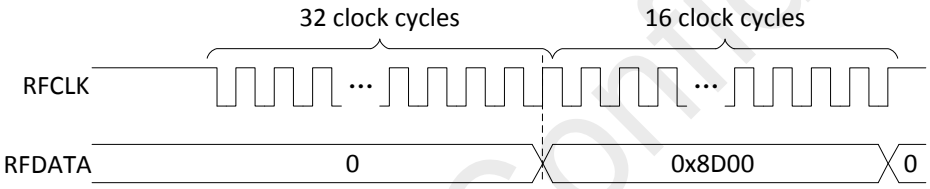


Figure 20. TWI_RST Command When Transmission Enabled by DATA Pin Rising Edge

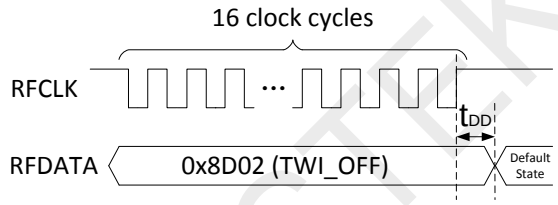


Figure 21. TWI_OFF Command

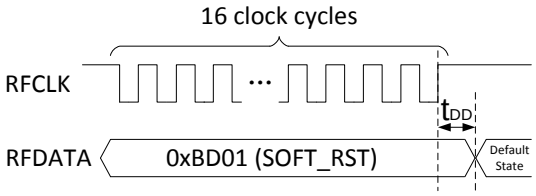


Figure 22. SOFT_RST Command

The RFDATA is generated by the host MCU on the rising edge of RFCLK, and is sampled by the device on the falling edge. The RFCLK should be pulled up by the host MCU during the TRANSMISSION shown in Figure 19. The TRANSMISSION process should refer to Figure 17 for its timing requirement, depending on the “Start By” setting configured on the RFPDK.

The device will go to SLEEP state by driving the DATA low for t_{STOP}, or issuing SOFT_RST command. A helpful practice for the device to go to SLEEP is to issue TWI_RST and SOFT_RST commands right after the useful data is transmitted, instead of waiting the t_{STOP}, this can save power significantly.

7. RISC Microcontroller Core

The embedded MCU core is a high performance RISC Microcontroller. It includes the following features.

- 8-bit data bus
- 1024 words OTP ROM, 49 bytes SRAM
- 42 Instructions to Learn
- 14-bit instructions
- 8-Level Stack
- Direct, indirect and relative addressing modes
- 5 types of oscillator
  - IRC－Internal 8M/4M/1M/455K RC oscillator
  - ERC－Low cost RC oscillator
- 2 or 4 clocks per instruction cycle (/2, /4)
- Power-Saving Sleep mode
- Watchdog timer with on-chip RC oscillator

- WDT enable by option or programmable
- Power edge-detector Reset (PED) .
- Power-on Reset (POR)
- Wake-on-Pin Change
- 4 I/O Pins with Individual Direction Control
- Timer0 : 8-bit timer with 6-bit prescaler
- PortB 0~5 own independent weak pull_up control.
- PortB 0~2 own independent weak pull_low control.
- PortB 0~5 own independent direction control.
- PortB 0~5 own independent Open-drain control.

The pins related to the MCU core ports can be mapped to the port names with the I/O and description shown in the table below.

Table 15. MCU Core Port Function Description

Pin Name	Port Name	I/O	Descriptions
K2/SCLK	PB0	I/O	Pull_up / pull_low / open drain enable by software. Wake-up from Sleep on Input mode pin change.
K3/SDA	PB1	I/O	Pull_up / pull_low / open drain enable by software. Wake-up from Sleep on Input mode pin change.
RFCLK	PB2	I/O	Pull_up / pull_low / open drain enable by software. Wake-up from Sleep on Input mode pin change. Can be software programmed for 8 bit counter clock input.
K1/VPP	PB3	I/O	Open drain enable by software. Wake-up from Sleep on Input mode pin change.
	/MCLR	I	ST input level. pull_up resistor always enable. System clear (Reset) input. Active low Reset to the device.
K0	PB4	I/O	Pull_up / open drain enable by software. Wake-up from Sleep on Input mode pin change. Outputs with the instruction cycle rate (RCOUT optional in IRC/ERIC, ERC mode).
RFDATA	PB5	I/O	Pull_up / open drain enable by software. Wake-up from Sleep on Input mode pin change. External clock source input (ERIC, ERC mode).

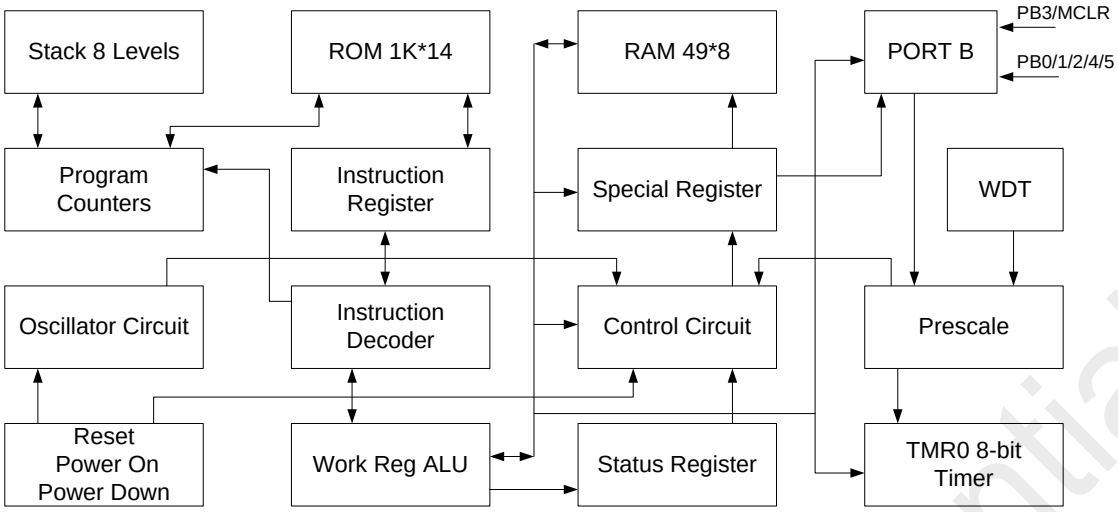


Figure 23. Microcontroller Core Block Diagram

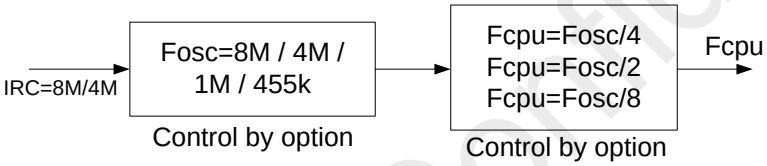


Figure 24. Clock Block Diagram

7.1 Memory Map

7.1.1 Program Memory

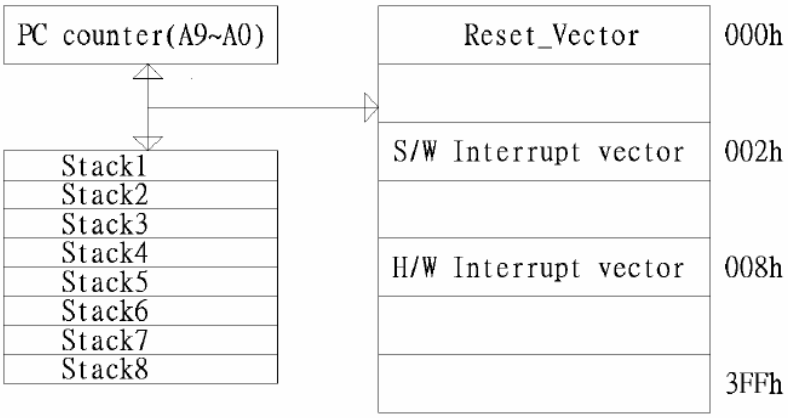


Figure 25. Program Memory

7.1.2 Data Memory Organization

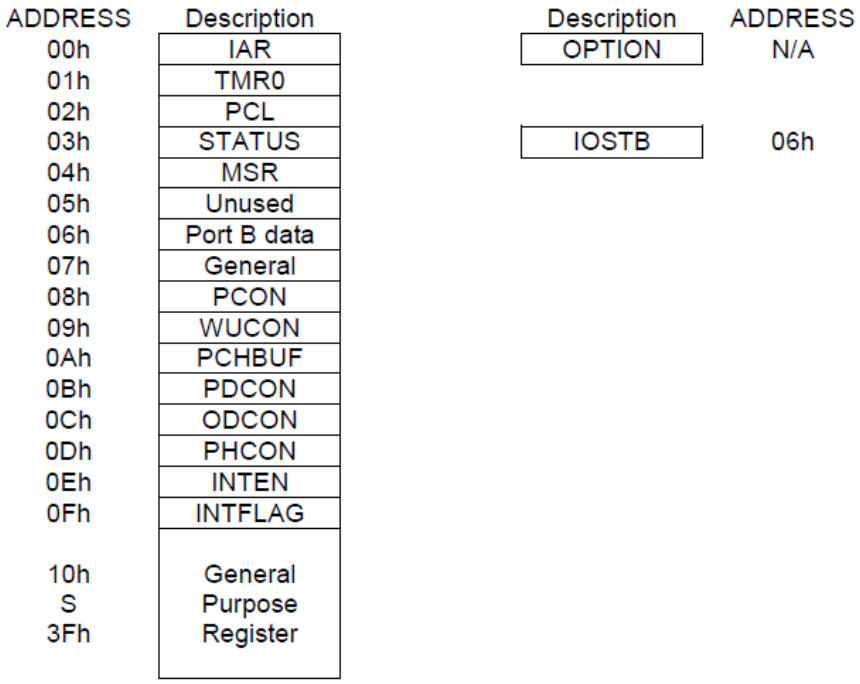


Figure 26. Data Memory Organization

Table 16. The Registers Controlled by TMODE or CPIO Instructions

ADDRESS	NAME	B7	B6	B5	B4	B3	B2	B1	B0
NA(W)	OPTION	*	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
06h(W)	Port B	-	-	PB5	PB4	PB3	PB2	PB1	PB0

Table 17. Operational Registers Map

ADDRESS	NAME	B7	B6	B5	B4	B3	B2	B1	B0
00h(W/R)	IAR	Uses contents of MSR to address data memory (not a physical register)							
01h(W/R)	TMR0	8-bit real-time clock/counter							
02h(W/R)	PCL	Low order 8 bits of PC							
03h(W/R)	STATUS	PBWUF	RP1	RP0	/TO	/PD	Z	DC	C
04h(W/R)	MSR	*	*	Indirect data memory address pointer					
05h	-	Unused							
06h(W/R)	Port B	-	-	PB5	PB4	PB3	PB2	PB1	PB0
07h(W/R)	SRAM	General Purpose Register							
08h(W/R)	PCON	WDTE	EIS	LVDTE	*	*	*	*	*
09h(W/R)	WUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0
0Ah(W/R)	PCHBUF	-	-	-	-	-	-	PCH1	PCH0
0Bh(W/R)	PDCON	GP	PDB2	PDB1	PDB0	-	-	-	-
0Ch(W/R)	ODCON	-	-	ODB5	ODB4	GP	ODB2	ODB1	ODB0
0Dh(W/R)	PHCON	-	-	PHB5	PHB4	GP	PHB2	PHB1	PHB0
0Eh(W/R)	INTEN	GIE	*	*	*	*	INTIE	PBIE	T0IE
0Fh(W/R)	INTFLAG	-	-	-	-	-	INTIF	PBIF	T0IF

Legend: - = unimplemented, read as '0' , * = unimplemented, read as '1',

7.1.3 Operational Registers

Table 18. IAR (Indirect Address Register) :

Power on Initial		x	x	x	x	x	x	x	x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h(w/r)	IAR	Uses contents of MSR to address data memory (not a physical register)							

The IAR Register is not a physical register. Any instruction accessing the IAR register can actually access the register pointed by MSR Register. Reading the IAR register itself indirectly (MSR="0") will read 00h. Writing to the IAR register indirectly results in a no-operation (although status bits may be affected).

The bits 5-0 of MSR register are used to select up to 64 registers (address: 00h ~ 3Fh).

Ex : Indirect Addressing

- Register address 0A\H contains the value 55\H
- Register address 0B\H contains the value 3A\H
- Load the value 0A\H into the MSR register
- A read of the IAR register will return the value of 55\H
- Increment the value of the MSR register by one (MSR = 0B\H)
- A read of the IAR register now will return the value of 3A\H

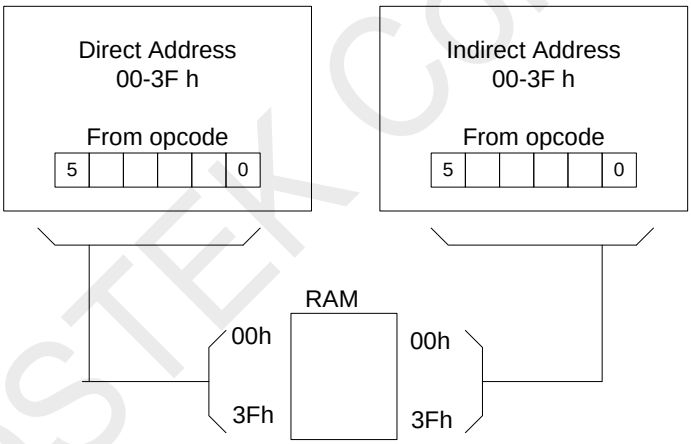


Figure 27. Direct/Indirect Addressing

Table 19. TMR0 (Real Time Counter/Counter Register)

Power on Initial		x	x	x	x	x	x	x	x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
01h(w/r)	TMR0	8-bit real-time clock/counter							

The Timer0 is a 8-bit timer/counter. The clock source of Timer0 can come from the instruction cycle clock or by an external clock source (PB2 pin) defined by T0CS bit 5 (TMR). If PB2 pin is selected, the Timer0 is increased by PB2 signal rising/falling edge (selected by T0SE bit 4 (TMR)).

The prescaler is assigned to Timer0 by clearing the PSA bit 3 (TMR). In this case, the prescaler will be cleared when TMR0 register is written with a value.

Table 20. PC (Program Counter)

Power on Initial		0	0	0	0	0	0	0	0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
02h(w/r)	PCL	Low order 8 bits of PC							

The chip has a 10-bit wide Program Counter (PC) and two-level deep 10-bit hardware push/pop stack. The low byte of PC is called the PCL register. This register is readable and writable. The high byte of PC is called the PCH register. This register contains the PC Bit 9~8 bits and is not directly readable or writable. As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a JUMP instruction, the PC Bit 8~0 is provided by the JUMP instruction word, PC Bit 9 is mapped to STATUS Bit 5. The PCL register is mapped to PC Bit 7~0.

For a CALL instruction, the PC Bit 7~0 is provided by the CALL instruction word, PC Bit 8 is always “0”, PC Bit 9 is mapped to STATUS Bit 5. The next PC will be loaded (Pushed) onto the top of STACK. The PCL register is mapped to PC Bit 7~0.

For a LJUMP instruction, the PC Bit 9~0 is provided by the LJUMP instruction word. The PCL register is mapped to PC Bit 7~0.

For a LCALL instruction, the PC Bit 9~0 is provided by the LCALL instruction word. The next PC will be loaded (Pushed) onto the top of STACK. The PCL register is mapped to PC Bit 7~0.

For a RET, or RTIW instruction, the PC are updated (Poped) from the top of STACK. The PCL register is mapped to PC Bit 7~0 .

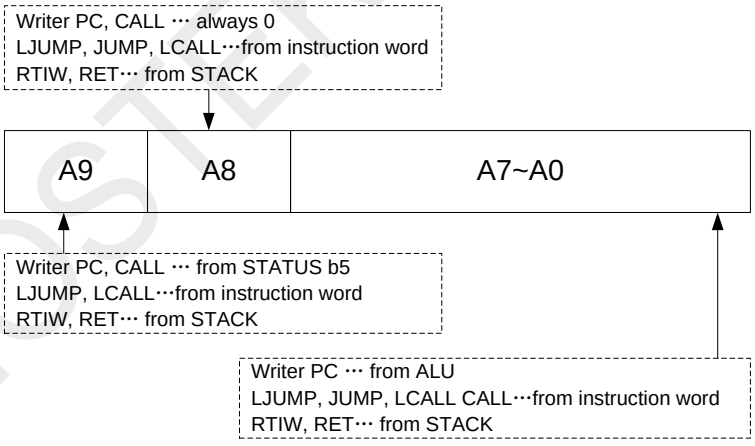


Figure 28. Program Counter

Table 21. STATUS (Status register)

Power on Initial		0	0	0	1	1	x	x	x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
03h(w/r)	STATUS	RST	GP1	GP0	/TO	/PD	Z	DC	C

This register contains the arithmetic status of the ALU, the RESET status. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the /TO and /PD bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, CLRR STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

Table 22. STATUS Register Function

Bit	Symbol	Function
0	C	Carry/Borrow bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PD	Power down flag bit
4	/TO	WDT time-out flag bit
5	GP0	General purpose bit
6	GP1	General purpose bit
7	RST	Bit for wake-up type

Table 23. STATUS Register Description

Bit	EX	Description
C	ADDWR	= 1, a carry occurred. = 0, a carry did not occur.
	SUBWR	= 1, a borrow did not occur. = 0, a borrow occurred.
	RRR, RLR	RRR load bit with LSB or RLR load bit with MSB, respectively
DC	ADDWR	= 1, a carry from the 4th low order bit of the result occurred. = 0, a carry from the 4th low order bit of the result did not occur.
	SUBWR	= 1, a borrow from the 4th low order bit of the result did not occur. = 0, a borrow from the 4th low order bit of the result occurred.
Z		= 1, the result of a logic operation is zero. = 0, the result of a logic operation is not zero.
/PD		= 1, after power-up or by the CLRWT instruction. = 0, by the SLEEP instruction.
/TO		= 1, after power-up or by the CLRWT or SLEEP instruction. = 0, a WDT time out occurred.
RST		= 1, Wake-up from SLEEP on Port B input change. = 0, Wake-up from other reset types.

Table 24. MSR (Memory Select Register)

Power on Initial		1	1	x	x	x	x	x	x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
04h(w/r)	MSR	*	*	Indirect data memory address pointer					

Bit 5 ~ 0: Select registers address in the indirect addressing mode.

Bit 7 ~ 6: Not used. Read always “1”.

Table 25. Port B (Port B Data Output Register)

Power on Initial		0	0	x	x	x	x	x	x
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
06h(w/r)	Port B	-	-	PB5	PB4	PB3	PB2	PB1	PB0

Reading the port (Port B register) reads the status of the pins independent of the pin's input/output modes. Writing to these ports will write to the port data latch. The Port B is a 6 bit port data register, bit 7 & bit 6 read always "0", and PB3 is input only.

Table 26. PCON (Power Control Register)

Power on Initial		1	0	1	-	-	-	-	-
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
08(w/r)	PCON	WDTE	EIS	LVDTE	*	*	*	*	*

Table 27. PCON Register Description

Bit	Symbol	Description
5	LVDTE	LVDT (low voltage detector) enable bit. = 1, Enable LVDT. = 0, Disable LVDT.
6	EIS	Define the function of IOB0/INT pin. = 1, INT (external interrupt pin) is selected. In this case, the I/O control bit of IOB0 must be set to "1". The path of Port B input change of IOB0 pin is masked by hardware, the status of INT pin can also be read by way of reading PORTB. = 0, IOB0 (bi-directional I/O pin) is selected. The path of INT is masked.
7	WDTE	WDT (watch-dog timer) enable bit. = 1, Enable WDT. = 0, Disable WDT.

Table 28. WUCON (Port B Input Change Interrupt/Wake-up Control Register)

Power on Initial		0	0	0	0	0	0	0	0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
09h(w/r)	WUCON	-	-	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0

1, Enable the input change interrupt/wake-up function.

0, Disable the input change interrupt/wake-up function.

Table 29. PCHBUF (High Byte Buffer of Program Counter)

Power on Initial		-	-	-	-	-	-	0	0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Ah(w/r)	PCHBUF	-	-	-	-	-	-	PCH1	PCH0

Table 30. PDCON (Pull-down Control Register)

Power on Initial		1	1	1	1	-	-	-	-
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Bh(w/r)	PDCON	GP	PDB2	PDB1	PDB0	*	*	*	*

1, Disable the internal pull-down of pin.

0, Enable the internal pull-down of pin

Table 31. ODCON (Open-drain Control Register)

Power on Initial		-	-	0	0	0	0	0	0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Ch(w/r)	ODCON	-	-	ODB5	ODB4	GP	ODB2	ODB1	ODB0

1, Enable the internal open-drain of pin.

0, Disable the internal open-drain of pin

Bit3: General purpose read/write bit.

Table 32. PHCON (Pull-high Control Register)

Power on Initial		-	-	1	1	1	1	1	1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Dh(w/r)	PHCON	-	-	PHB5	PHB4	GP	PHB2	PHB1	PHB0

1, Disable the internal pull-high of pin.

0, Enable the internal pull-high of pin.

Bit3: General purpose read/write bit.

Table 33. INTEN (Interrupt Mask Register)

Power on Initial		0	-	-	-	-	0	0	0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Eh(w/r)	INTEN	GIE	-	-	-	-	INTIE	PBIE	T0IE

Table 34. INTEN Register Description

Bit	Symbol	Description
0	T0IE	Timer0 overflow interrupt enable bit. = 1, Enable the Timer0 overflow interrupt. = 0, Disable the Timer0 overflow interrupt.
1	PBIE	Port B input change interrupt enable bit. = 1, Enable the Port B input change interrupt. = 0, Disable the Port B input change interrupt.
2	INTIE	External INT pin interrupt enable bit. = 1, Enable the External INT pin interrupt. = 0, Disable the External INT pin interrupt.
7	GIE	Global interrupt enable bit. = 1, Enable all un-masked interrupts. For wake-up from SLEEP mode through an interrupt event, the device will branch to the interrupt address (008h). = 0, Disable all interrupts. For wake-up from SLEEP mode through an interrupt event, the device will continue execution at the instruction after the SLEEP instruction. Note : When an interrupt event occur with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts. The RETFIE instruction will exit the interrupt routine and set the GIE bit to re-enable interrupt.

Table 35. INTFLAG (Interrupt Status Register)

Power on Initial		-	-	-	-	-	0	0	0
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Fh(w/r)	INTFLAG	-	-	-	-	-	INTIF	PBIF	T0IF

Table 36. INTFLAG Register Description

Bit	Symbol	Description
0	T0IF	Timer0 overflow interrupt flag. Set when Timer0 overflows, reset by software.
1	PBIF	Port B input change interrupt flag. Set when Port B input changes, reset by software.
2	INTIF	External INT pin interrupt flag. Set by rising/falling (selected by INTEDG bit (OPTION<6>)) edge on INT pin, reset by software.

Table 37. TMR (Time Mode Register)

Power on Initial		-	0	1	1	1	1	1	1
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A(w)	TMR	*	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Accessed by TMODE instruction.

By executing the TMODE instruction, the contents of the W Register will be transferred to the TMR Register. The TMR Register is a 8-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler, Timer0 source edge select, Timer0 clock source select, the PB Pull High enable, and the PB wake up enable .

When /ENWU is set to "0", the input pin PB0, 1, 3, 4, 5 bit will initiate the wake-up function in the sleep mode; But input pin PB2 initiate the wake-up function must set T0CS to "0" .

Table 38. TMR Register Function Description

Bit	Symbol	Function		
		Prescaler Value	TMR0 rate	WDT rate
2—0	PS2—0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256	1 : 1 1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128
3	PSA	Prescaler assignment bit : 0 — TMR0 1 — Watchdog Timer		
4	T0SE	TMR0 signal Edge : 0 — Increment on low-to-high transition on PB2 pin 1 — Increment on high-to-low transition on PB2 pin		
5	T0CS	TMR0 signal set : 0 — Internal instruction cycle clock 1 — Transition on PB2 pin		
6	INTEDG	Interrupt edge select bit. = 0, interrupt on falling edge of INT pin. = 1, interrupt on rising edge of INT pin.		

7.2 Reset Condition for all Registers

Table 39. Reset Conditions for All Registers

ADDRESS	NAME	Power-On Reset	MCLR_Reset WDT_Reset
N/A	TMR	-011 1111	-011 1111
N/A	IOSTB	--11 1111	--11 1111
ADDRESS	NAME	Power-On Reset	MCLR_Reset WDT_Reset
00h	IAR	xxxx xxxx	uuuu uuuu
01h	TMR0	xxxx xxxx	uuuu uuuu
02h	PCL	0000 0000	0000 0000
03h	STATUS	0001 1xxx	000# #uuu
04h	MSR	11xx xxxx	11uu uuuu
05h	-	---- ----	---- ----
06h	Port B	--xx xxxx	--uu uuuu
07h	SRAM	xxxx xxxx	uuuu uuuu
08h	PCON	101- ----	101- ----
09h	WUCON	0000 0000	0000 0000
0Ah	PCHBUF	---- --00	---- --00
0Bh	PDCON	1111 1111	1111 1111
0Ch	ODCON	0000 0000	0000 0000
0Dh	PHCON	1111 1111	1111 1111
0Eh	INTEN	0--- -000	0--- -000
0Fh	INTFLAG	---- -000	---- -000

Note : " x "=unknown, " – "=unimplemented, read as "0", "# "=value depends on condition

Table 40. RST/TOB/PDB Status after Reset or Wake-up

RESET	RST	TOB	PDB
Power-on Reset	0	1	1
MCLRB Reset during normal operation	0	u	u
MCLRB Reset during SLEEP	0	1	0
WDT Reset during normal operation	0	0	1
WDT Wake-up during SLEEP	0	0	0
Wake-up on pin change during SLEEP	1	1	0

Note : " u "=unchanged

Table 41. Events Affecting TOB/PDB Status Bits

EVENT	TOB	PDB
Power-on	1	1
WDT Time-Out	0	u
SLEEP instruction	1	0
CLRWDT instruction	1	1

Note : " u "=unchanged

Table 42. Device Reset Time (OST)

Oscillator Mode	Power-on Reset	MCLRB Reset WDT Reset
ERC & IRC/ERIC	20/5/320/80ms or 160us	160us

7.3 Instruction Set

Table 43. Instruction Set

Mnemonic Operands	Function	Operating	Status
NOP	No operation	None	
CLRWT	Clear Watchdog timer	0→WT	/TO, /PD
SLEEP	Sleep mode	0→WT, stop OSC	/TO, /PD
TMODE	Load W to TMODE register	W→TMODE	None
RET	Return	Stack→PC	None
CPIO R	Control I/O port register	W→CPIO r	None
STWR R	Store W to register	W→R	None
LDR R, t	Load register	R→t	Z
LDWI I	Load immediate to W	I→W	None
SWAPR R, t	Swap halves register	[R(0~3) R(4~7)]→t	None
INCR R, t	Increment register	R + 1→t	Z
INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
ADDWR R, t	Add W and register	W + R→t	C, HC, Z
SUBWR R, t	Subtract W from register	R – W→t (R+/W+1→t)	C, HC, Z
DECR R, t	Decrement register	R – 1→t	Z
DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
ANDWR R, t	AND W and register	R ∩ W→t	Z
ANDWI i	AND W and immediate	i ∩ W→W	Z
IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
COMR R, t	Complement register	/R→t	Z
RRR R, t	Rotate right register	R(n)→R(n-1), C→R(7), R(0)→C	C
RLR R, t	Rotate left register	R(n)→R(n+1),C→R(0), R(7)→C	C
CLRW	Clear working register	0→W	Z
CLRR R	Clear register	0→R	Z
BCR R, b	Bit clear	0→R(b)	None
BSR R, b	Bit set	1→R(b)	None
BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
LJUMP n	Long JUMP to address	n→PC	None
CALL n	Call subroutine	n→PC, PC+1→Stack	None
RTIW i	Return, place immediate to W	Stack→PC, i→W	None
JUMP n	JUMP to address	n→PC	None

Mnemonic Operands	Function	Operating	Status
DAA	Adjust W data format from HEX to DEC after any addition operation	W(HEX)→W(DEC)	C
DAS	Adjust W data format from HEX to DEC after any subtraction operation	W(HEX)→W(DEC)	-
INT	S/W interrupt	002h→PC, PC+1→Stack, GIE=0	
ADCAR R,t	Add W and R with Carry	W + R + C→t	C, HC, Z
SBCAR R,t	Subtract W from R with Carry	/W + R + C→t	C, HC, Z

Table 44. Instruction Set Notes

BIT	Description	BIT	Description
W	Working register	B	Bit position
CPIO	Control I/O port register	t	Target
HC	Half carry	0	Working register
Z	Zero flag	1	General register
C	Carry flag		
PF	Power loss flag	R	General register address
PC	Program Counter	I	Immediate data (8 bits)
OSC	Oscillator	N	Immediate address
Inclu	Inclusive '∪'	/	Complement
Exclu	Exclusive '⊕'	x	Don't care
AND	Logic AND '∩'		

7.4 Equivalent Circuit

7.4.1 PB0, PB1, PB5 Equivalent Circuit

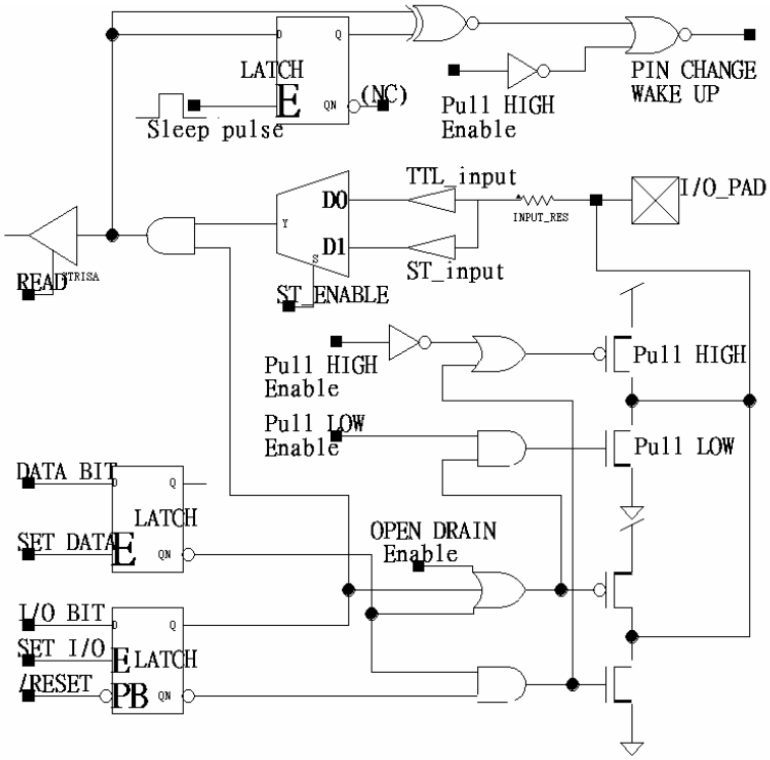


Figure 29. PB0 ,PB1 ,PB5 Equivalent Circuit

7.4.2 PB2 Equivalent Circuit

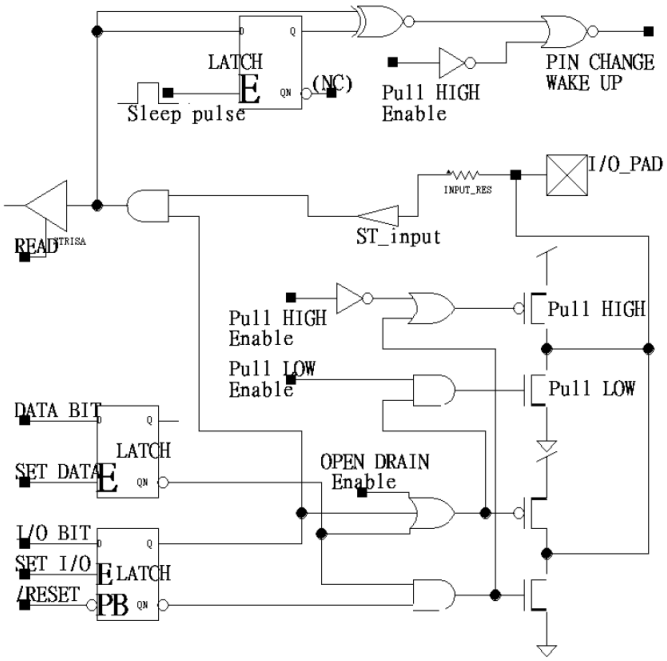


Figure 30. PB2 Equivalent Circuit

7.4.3 PB3 Equivalent Circuit

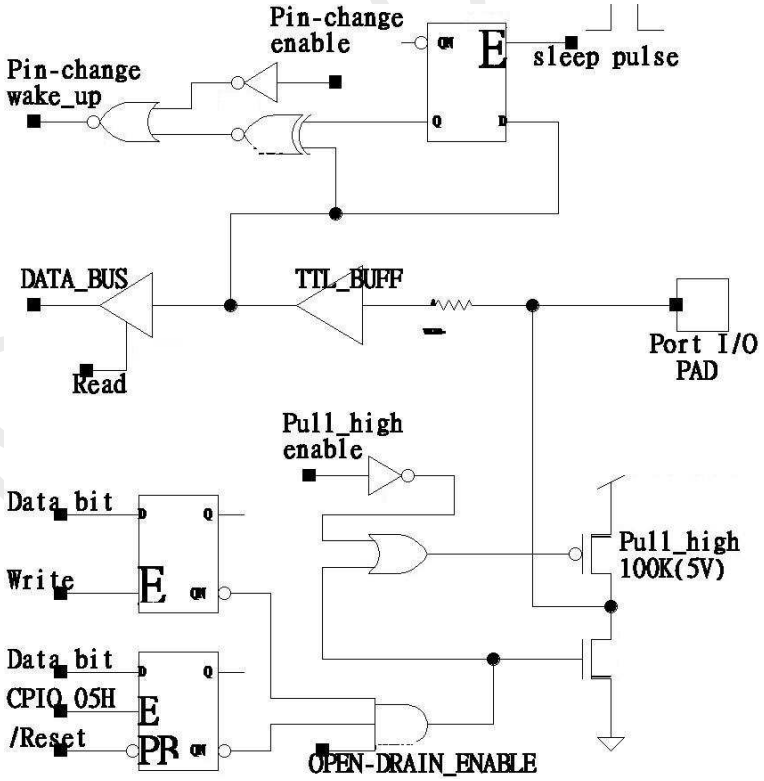


Figure 31. PB3 Equivalent Circuit

7.4.4 /MCLR Equivalent Circuit

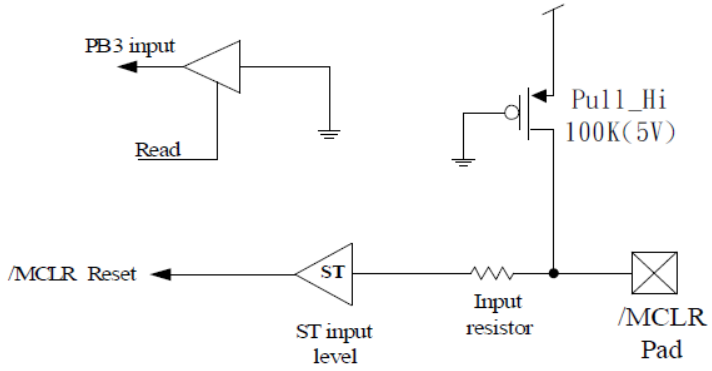


Figure 32. /MCLR Equivalent Circuit

7.4.5 PB4 Equivalent Circuit

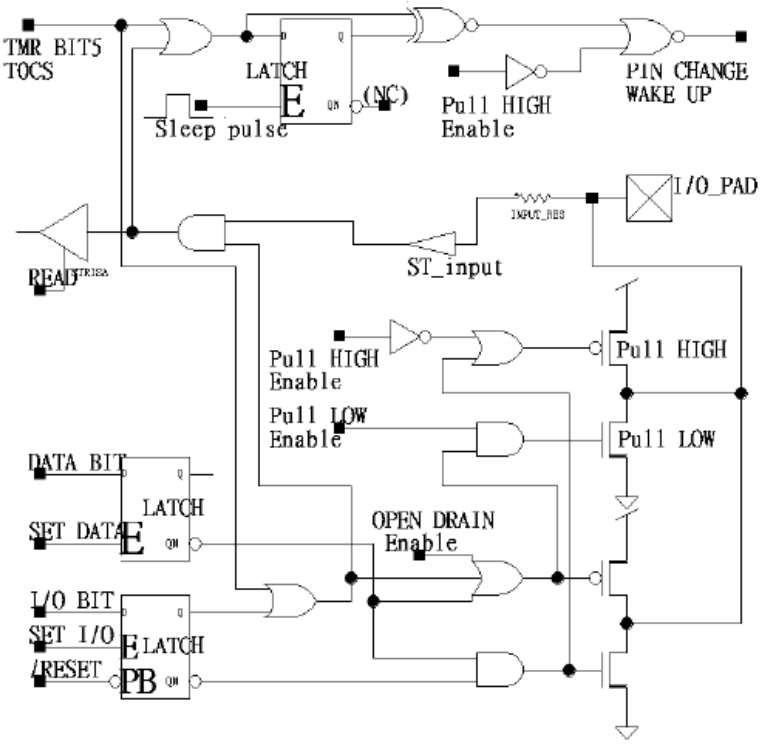


Figure 33. PB4 Equivalent Circuit

8. Ordering Information

Table 45. CMT2180APW Ordering Information

Part Number	Descriptions	Package Type	Package Option	Operating Condition	MOQ / Multiple
CMT2180APW-ESR[1]	240 – 480 MHz SoC OOK Transmitter	SOP14	Tape & Reel	2.3 to 3.6 V, -20 to 85 ℃	2,500
CMT2180APW-ESB[1]	240 – 480 MHz SoC OOK Transmitter	SOP14	Tube	2.3 to 3.6 V, -20 to 85 ℃	1,000

Notes:

[1]. "E" stands for extended industrial product grade, which supports the temperature range from -20 to +85 ℃.
"S" stands for the package type of SOP14.
"R" stands for the tape and reel package option, the minimum order quantity (MOQ) for this option is 2,500 pcs. "B" stands for the tube package option, with the MOQ of 1,000 pcs.

Visit www.cmostek.com/products to know more about the product and product line.
Contact sales@cmostek.com or your local sales representatives for more information.

9. Package Outline

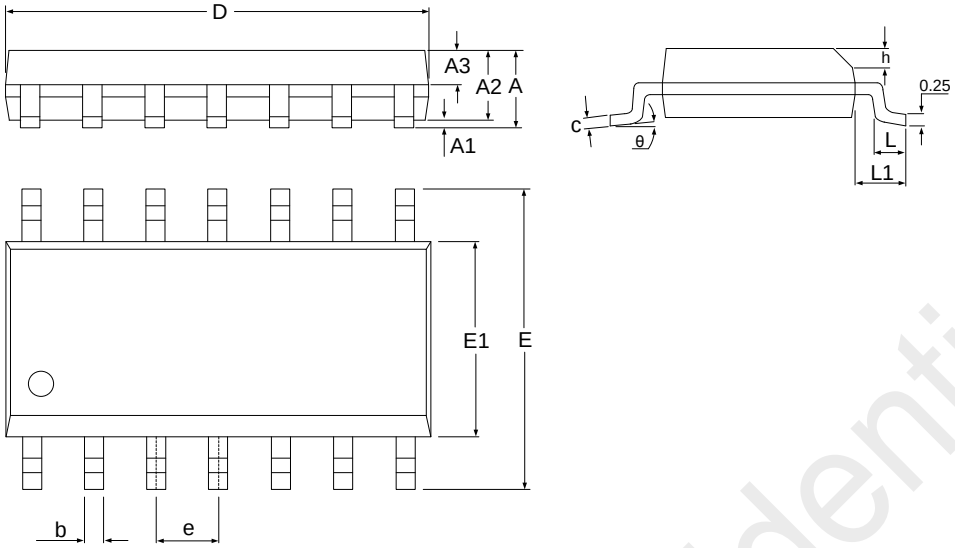


Figure 34. 14-Pin SOP Package

Table 46. 14-Pin SOP Package Dimensions

Symbol	Size (millimeters)		
	Min	Typ	Max
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
C	0.21	-	0.26
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.30	-	0.60
L1	1.05 BSC		
θ	0	-	8°

10. Top Marking

10.1 CMT2180APW Top Marking

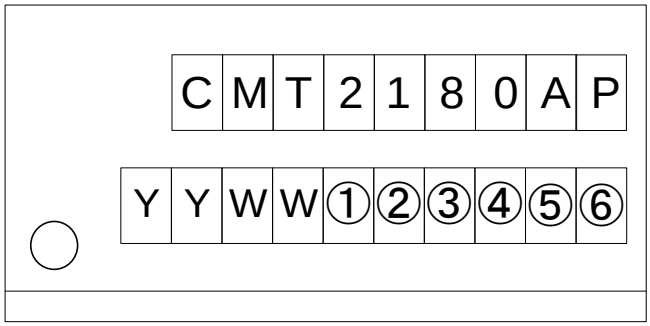


Figure 35. CMT2180APW Top Marking

Table 47. CMT2180APW Top Marking Explanation

Mark Method :	Laser
Pin 1 Mark :	Circle's diameter = 1 mm.
Font Size :	0.35 mm, right-justified.
Line 1 Marking :	CMT2180AP represents part number CMT2180APW
Line 2 Marking :	YYWW is the Date code assigned by the assembly house. YY represents the last two digits of the mold year and WW represents the workweek. ①②③④⑤⑥ is the internal tracking number.

11. Other Documentations

Table 48. Other Documentations for CMT2180APW

Brief	Name	Descriptions
AN131	CMT218xA Schematic and PCB Layout Design Guideline	Details of CMT2180Ax, CMT2189A PCB schematic and layout design rules, RF matching network and other application layout design related issues.
AN132	CMT2180/89A Configuration Guideline	Details of configuring CMT2180/89A features on the RFPDK.

12. Document Change List

Table 49. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.8	All	Initial Released	2016-12-27

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