DM13C

16-bit Constant Current LED Driver

with Error Detection

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with Error Detection

General Description

DM13C is a constant-current sink driver specifically designed for LED display applications. The device incorporates shift registers, data latches, and constant current circuitry on the silicon CMOS chip. The maximum output current value of all 16 channels is adjustable by a single external resistor. Its built-in open/short detection circuits help users detect LED failures. System retrieve the error messages to indicate which channel has failure by serial output data. The thermal shutdown function provides the over temperature protection.

Features

- Constant-current outputs: 5mA to 90mA adjustable by one external resistor

- Maximum output voltage: 17V

- Maximum clock frequency: 25MHz

- Built-in real-time LED open/short detection

- Fast detecting response: 0.1us (min.)

- Over temperature protection: thermal shutdown (junction temperature > 180°C)

- Package and pin assignment compatible to conventional LED drivers (ST2221C, DM134/5/6)

- Power supply voltage: 3.3V to 5.5V

- Bit-to-bit skew : $\pm3\%$ @ 25mA~90mA   Chip-to-chip skew : $\pm6\%$ @ 25mA~90mA

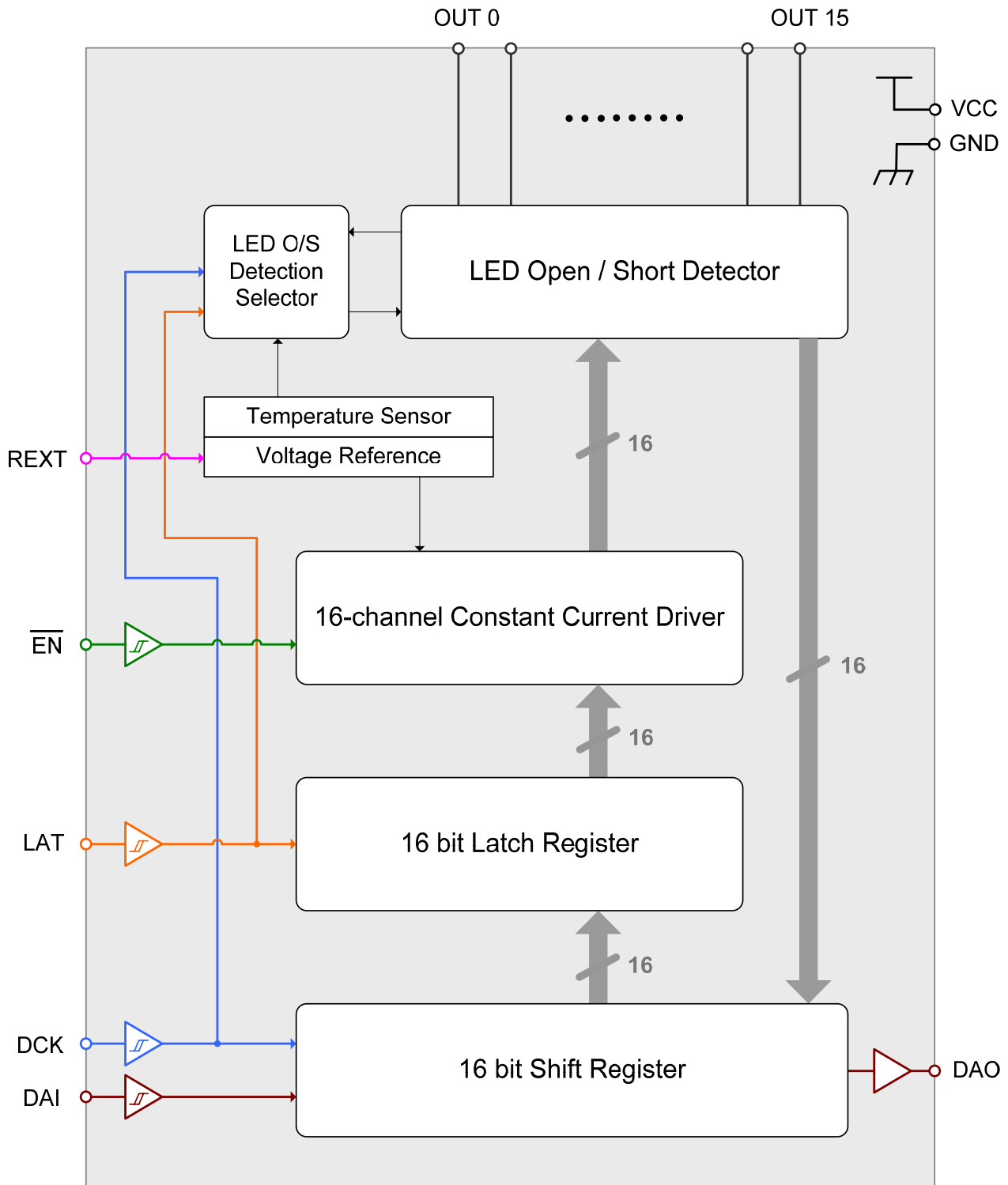 $\pm6\%$ @   5mA~25mA $\pm10\%$ @   5mA~25mA

Applications

- Indoor/Outdoor LED Video Display
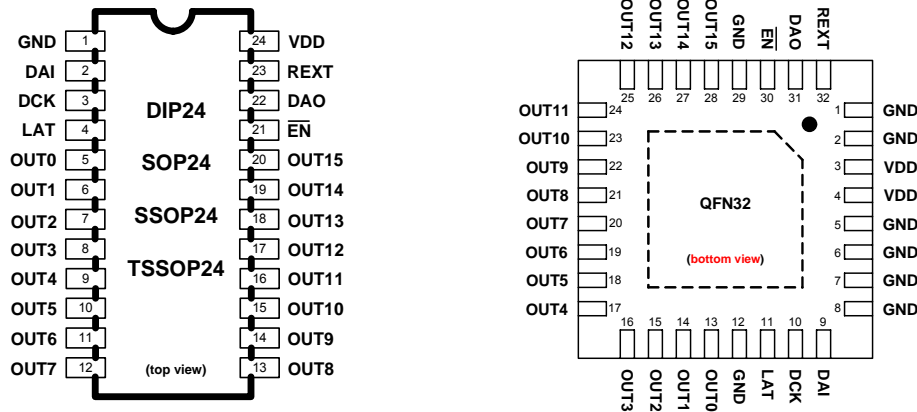
- LED Variable Message Signs (VMS) System

Package Types

- DIP24, SOP24, SOP24B, SSOP24, TSSOP24 (with exposed pad), QFN32 (with exposed pad)

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SiTI Silicon Touch Technology Inc.

Block Diagram

OUT 0   OUT 15

• • • • • • • •

VCC

GND

LED O/S Detection Selector

LED Open / Short Detector

Temperature Sensor

Voltage Reference

REXT

16

16-channel Constant Current Driver

16

EN

LAT

16 bit Latch Register

16

DCK

DAI

16

16 bit Shift Register

DAO

Pin Connection

Pin Description

| PIN No.	PIN NAME	FUNCTION
DIP24/SOP24/SSOP24/TSSOP24: 1 TSSOP24: exposed pad QFN32: 1, 2, 5, 6, 7, 8, 12, 29, exposed pad	GND	Ground terminal.
DIP24/SOP24/SSOP24/TSSOP24: 2 QFN32: 9	DAI	Serial data input terminal.
DIP24/SOP24/SSOP24/TSSOP24: 3 QFN32: 10	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
DIP24/SOP24/SSOP24/TSSOP24: 4 QFN32: 11	LAT	Input terminal of data strobe. Data on shift register goes through at the rising edge of LAT (edge trigger). Otherwise, data is latched.
DIP24/SOP24/SSOP24/TSSOP24: 5~20 QFN32: 13~28	OUT0~15	Sink constant-current outputs (open-drain).
DIP24/SOP24/SSOP24/TSSOP24: 21 QFN32: 30	$\overline{\text{EN}}$	Output enable terminal: **'H'** for all outputs are turned off , **'L'** for all outputs are active.
DIP24/SOP24/SSOP24/TSSOP24: 22 QFN32: 31	DAO	Serial data output terminal.
DIP24/SOP24/SSOP24/TSSOP24: 23 QFN32: 32	REXT	External resistors connected between REXT and GND for output current value setting.

DIP24/SOP24/SSOP24/TSSOP24: 24 QFN32: 3, 4	VCC	Supply voltage terminal.

Equivalent Circuit of Inputs and Outputs

1. DCK, DAI, LAT, $\overline{\text{EN}}$ terminals
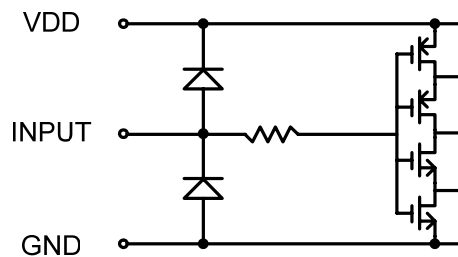
2. DAO terminals
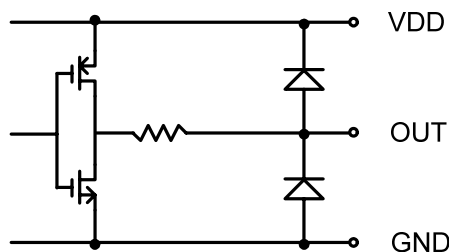
Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VCC	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VCC+0.3	V
Output Current	IOUT	100	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FDCK	25	MHz
GND Terminal Current	IGND	1600	mA
Power Dissipation (4 layer PCB)	PD	2.34 (QFN32 : Ta=25°C)	W
		2.11 (TSSOP24 exposed pad: Ta=25°C)	
		1.90 (PDIP24 : Ta=25°C)	
		1.20 (SOP24 : Ta=25°C)	
		1.05 (SSOP24 : Ta=25°C)	
Thermal Resistance	Rth(j-a)	40.6 (QFN32)	°C/W
		45 (TSSOP24 exposed pad)	
		50.0 (PDIP24)	
		79.2 (SOP24)	
		90.2 (SSOP24)	
Operating Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VCC	—	3.3	5.0	5.5	V
Output Voltage	VOUT	Driver On[1]	1.0	—	0.5VCC	V
Output Voltage	VOUT	Driver Off[2]	—	—	17	
Output Current	IO	OUTn	5	—	90	mA
	IOH	VOH = VCC – 0.2 V	—	—	+1.2	
	IOL	VOL = 0.2 V	—	—	−1.4	
Input Voltage	VIH	VCC = 3.3 V ~ 5.5V	0.8VCC	—	VCC	V
	VIL		0.0	—	0.2VCC	
Input Clock Frequency	FDCK	Single Chip Operation	—	—	25	MHz
LAT Pulse Width	tw LAT	VCC = 5.0V	15	—	—	ns
DCK Pulse Width	tw DCK		15	—	—	
Set-up Time for DAI	tsetup(D)		10	—	—	
Hold Time for DAI	thold(D)		10	—	—	
Set-up Time for LAT	tsetup(L)		10	—	—	
Hold Time for LAT	thold(L)		10	—	—	
Set-up Time for Open/Short	tsetup(OS)		25	—	—	

[1] Notice that the power dissipation is limited to its package and ambient temperature.
[2] The driver output voltage including any overshoot stress has to be compliant with the maximum voltage (17V).

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| Open/Short Detection Response | tdet | | 100 | — | — | |

Electrical Characteristics (VCC = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.8VCC	—	VCC	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.2VCC	
Output Leakage Current	IOL	VOH = 17 V	—	—	±1.0	uA
Output Voltage (S-OUT)	VOL	IOL = 1.4 mA	—	—	0.2	V
	VOH	IOH= 1.2 mA	VCC-0.2	—	—	
Output Current Skew (Channel-to-Channel)[*1]	IOL1	VOUT = 1.0 V Rrext = 2.2 KΩ	—	—	±3	%
Output Current Skew (Chip-to-Chip)[*2]	IOL2				±6	%
Output Voltage Regulation	% / VOUT	Rrext = 2.2 KΩ VOUT = 1 V ~ 3 V	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VCC	Rrext = 2.2 KΩ	—	±1	±4	
LED Open Detection Threshold	V(od)	all outputs turn on	—	0.3	—	V
LED Short Detection Threshold	V(sd)		—	0.5VCC	—	
Thermal Shutdown Threshold	T(sht)	junction temperature	—	180	—	°C
Supply Current[*3]	$I_{DD(off)}$	power on all pins are open unless VCC and GND	—	3.0	—	mA
	$I_{DD(off)}$	input signal is static Rrext = 2.9 KΩ all outputs turn off	—	4.9	—	
	$I_{DD(on)}$	input signal is static Rrext = 2.9 KΩ all outputs turn on	—	6.4	—	
	$I_{DD(off)}$	input signal is static Rrext = 560 Ω all outputs turn off	—	12.7	—	
	$I_{DD(on)}$	input signal is static Rrext = 560 Ω all outputs turn on	—	15.4	—	

[*1] Channel-to-channel skew is defined as the ratio between (any Iout – average Iout) and average Iout, where average Iout = (Imax + Imin) / 2.

[*2] Chip-to-Chip skew is defined as the range into which any output current of any IC falls.

[*3] IO excluded.

Switching Characteristics (VCC = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	EN-to-OUT15	tpLH	VIH = VCC VIL = GND Rrext = 2.2 KΩ VL = 5.0 V RL = 180 Ω CL*1 = 13 pF	—	16	—	ns
	LAT-to-OUT15			—	28.5	—	
	DCK-to-DAO			—	18	—	
Propagation Delay ('H' to 'L')	EN-to-OUT15	tpHL		—	18	—	
	LAT-to-OUT15			—	20.5	—	
	DCK-to-DAO			—	16	—	
Output Current Rise Time		tor		—	17	—	
Output Current Fall Time		tof		—	15	—	
Output Delay Time (OUT(n)-to-OUT(n+1))		tod		—	2.2	—	

Switching Characteristics (VCC = 3.3V, Ta = 25°C unless otherwise noted)

| CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	EN-to-OUT15	tpLH	VIH = VCC VIL = GND Rrext = 2.2 KΩ VL = 5.0 V RL = 180 Ω CL*1 = 13 pF	—	64	—	ns
	LAT-to-OUT15			—	57	—	
	DCK-to-DAO			—	25	—	
Propagation Delay ('H' to 'L')	EN-to-OUT15	tpHL		—	17.5	—	
	LAT-to-OUT15			—	25	—	
	DCK-to-DAO			—	20	—	
Output Current Rise Time		tor		—	50	—	
Output Current Fall Time		tof		—	15	—	
Output Delay Time (OUT(n)-to-OUT(n+1))		tod		—	2.2	—	

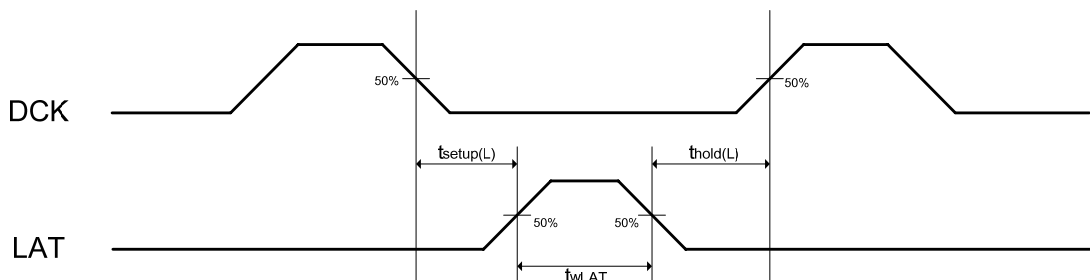*1 CL means the probe capacitance of oscilloscope.
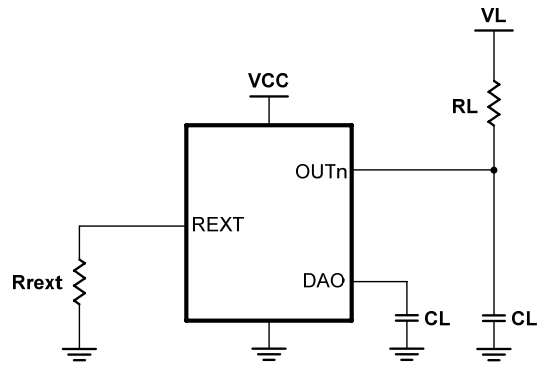
Switching Characteristics Test Circuit

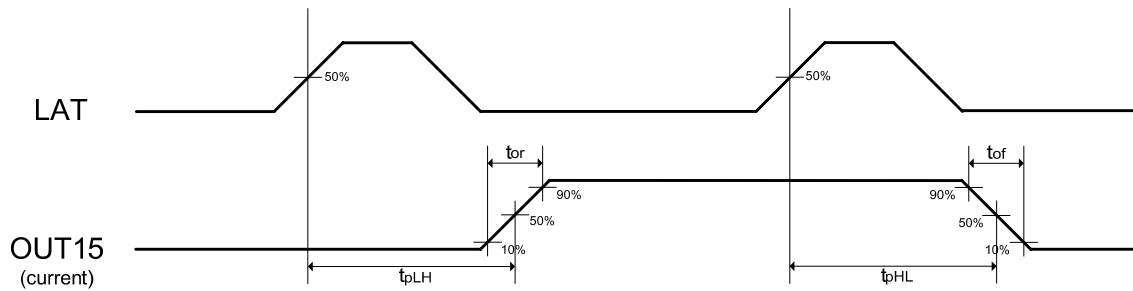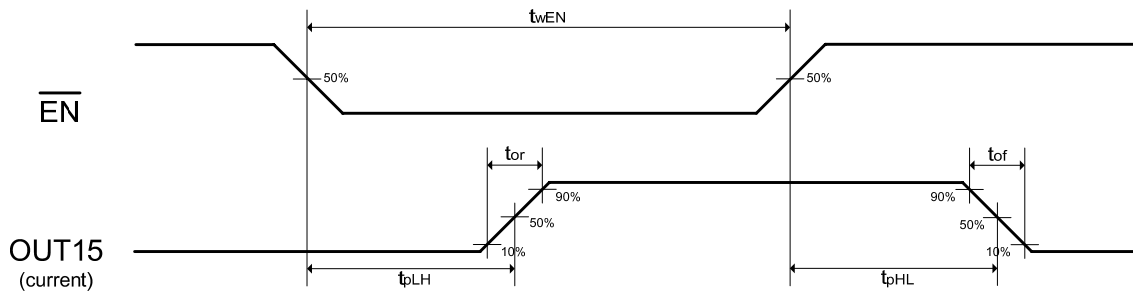## Timing Diagram

1. DCK-DAI, DAO
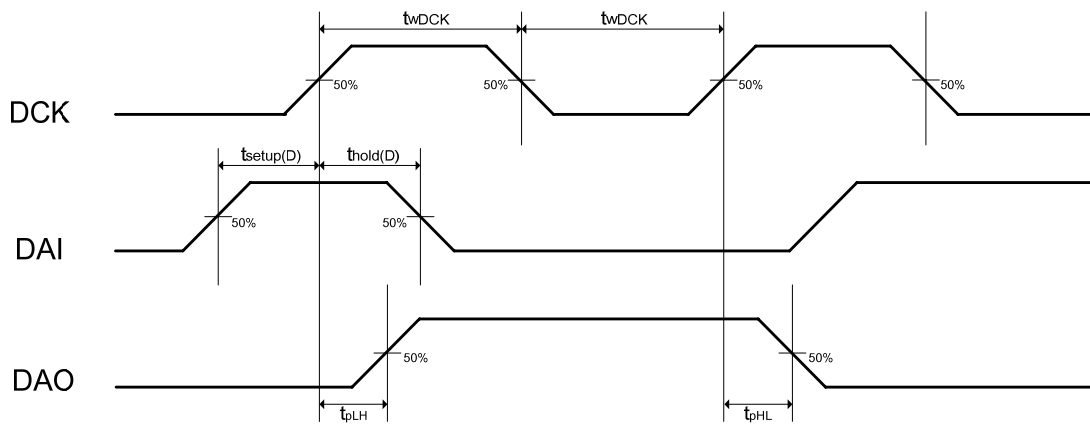
2. DCK-LAT

3. LAT-OUT15

4. $\overline{\text{EN}}$-OUT15
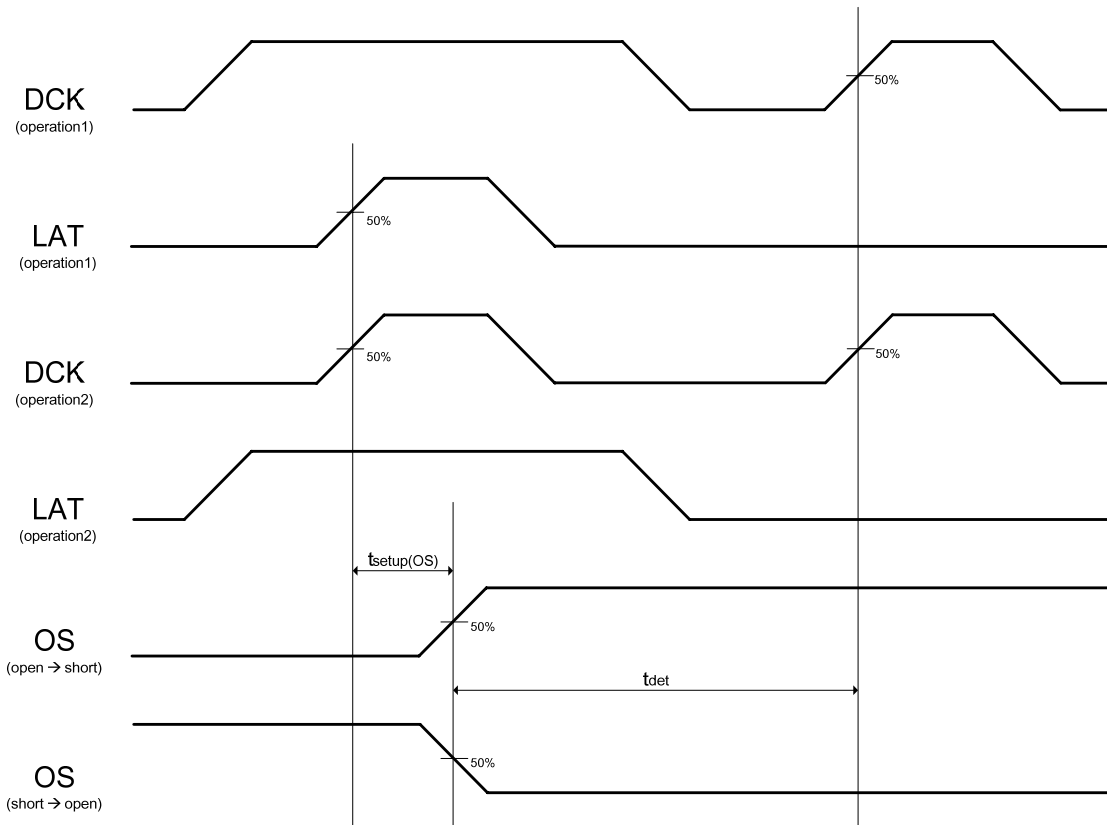

5. OUT_{n+1}-OUT_n
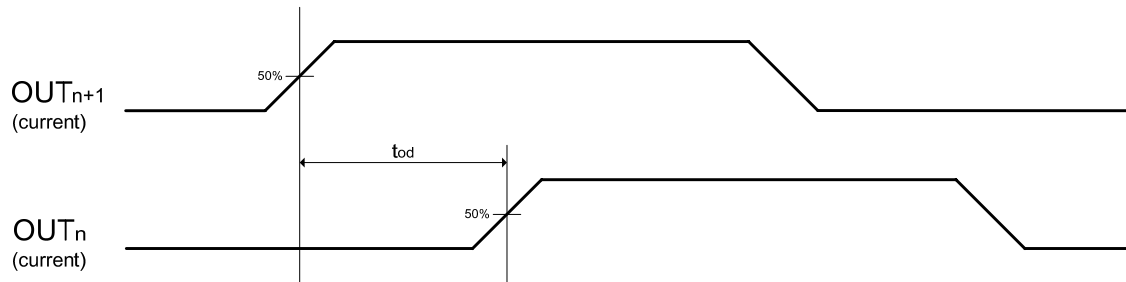
## 6. OS-LAT, DCK ($\overline{\text{EN}}$='L')
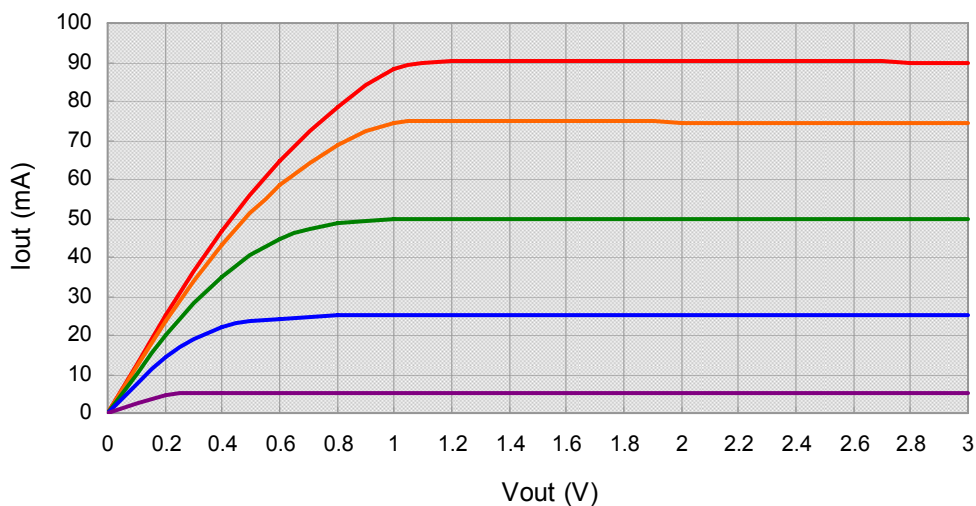
Constant-Current Output

Constant-current value of each output channel is set by an external resistor connected between the REXT pin and GND. Varying the resistor value can adjust the current scale ranging from 5mA to 90mA. The reference voltage of REXT terminal (Vrext) is approximately 1.2V. The output current value is calculated roughly by the following equation:

Iout(mA)	5	10	20	30	40	50	60	70	80	90
M	46.4	45.9	45	44.5	44.2	44.3	44.9	43.7	42.3	42.7

Output Current as a Function of Rrext Value

$$\text{Iout (mA)} \simeq \frac{\text{Vrext (V)}}{\text{Rrext (K}\Omega)} \times \mathbf{M}$$
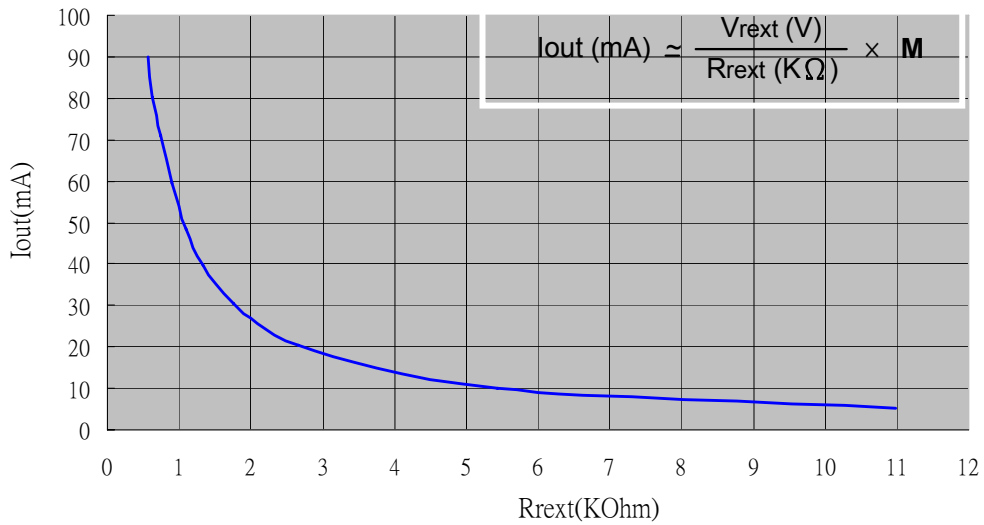
Output Current as a Function of Output Voltage

In order to obtain a good performance of constant-current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage above.

Serial Data Interface

The serial-in data (DAI) will be clocked into 16 bit shift register synchronized on the rising edge of the clock (DCK). The data '1' represents the corresponding current output 'ON', while the data '0' stands for 'OFF'. The data will be transferred into the 16 bit latch synchronized on the rising edge (edge trigger) of the strobe signal (LAT); otherwise, the data will be held. The latch pulse should be sent after the falling edge of the last clock within a frame data. The trigger timing of the serial-out data (DAO) will be shifted out on synchronization to the rising edge of the clock. All

outputs are turned off while enable terminal (EN) is kept at high level. And they are active when EN shifts to low.
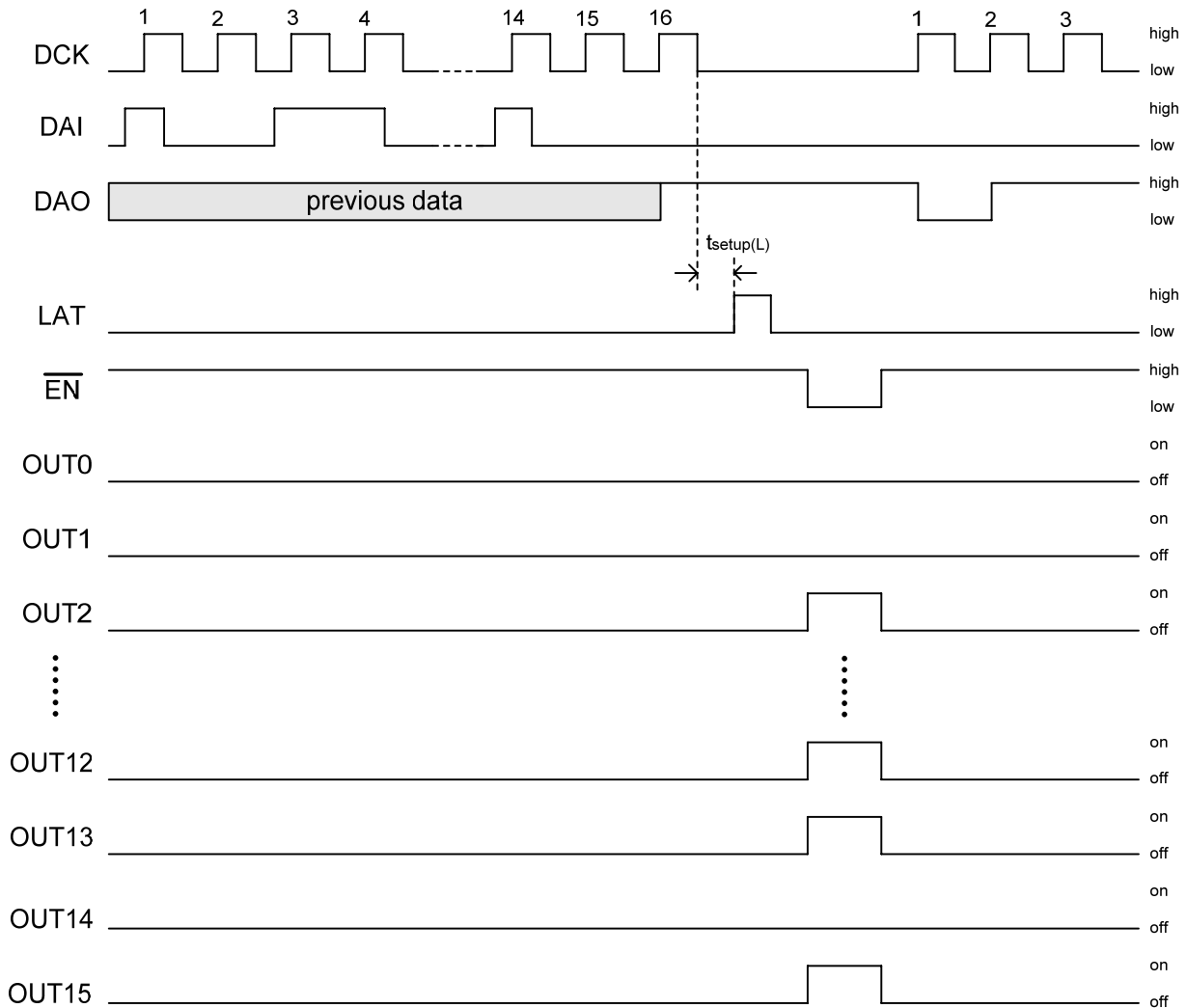
Thermal Shutdown

During operation, when the junction temperature of the IC will reach approximately above $180℃$, it will cause the driver to shutdown all the outputs. Basically, the IC will cool down and return to the safe operating temperature which is approximately below $110℃$. DM13C will restart all the outputs at the same time. Operation in the thermal situation for a long time may cause chip damage permanently.
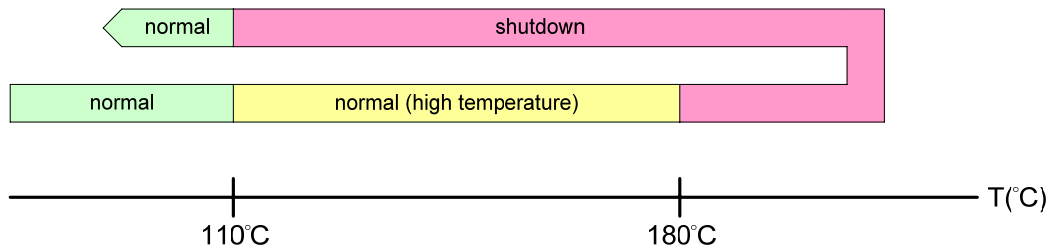
Relations between Thermal Shutdown and Junction Temperature

LED Open/Short Detection

The result of open/short detection of DM13C could be retrieved from serial-out (DAO) data. It will be identified as a LED open failure when the output is turned on but the output voltage is below 0.3V. And then it will be identified as a LED short failure when the output is turned on but the output voltage is above 1/2 VCC.

To set up with the following conditions: (1) the image data written in shift register corresponding to particular output channel is '1'; (2) the output enable terminal is activated (EN='L'); (3) the rising edge of the latch signal (LAT), DM13C will execute LED open/short detection then renews the results within the corresponding shift register.

By using the error message retrieved from serial-out data, system can recognize the status of every LED driven by each channel. For either LED open or short detection, the original image data is written to '1' but '0' is retrieved then a LED failure has occurred. If the image data is written to '0' or the output enable terminal is inactive (EN='H'), it will not execute any detection process for the corresponding channel. Therefore, system still retrieves the original image data.
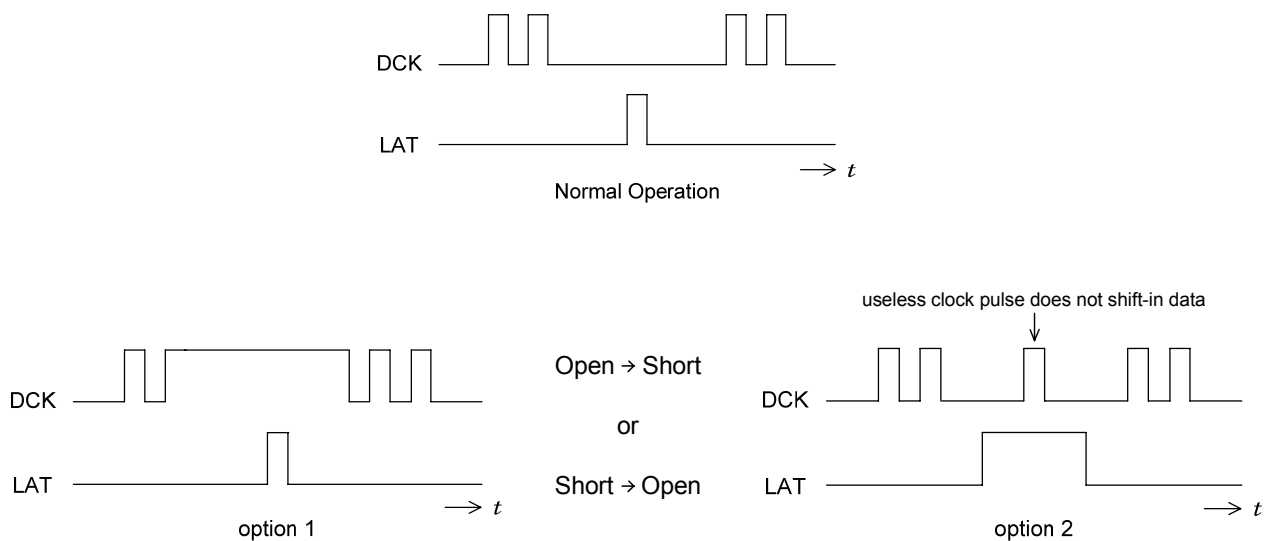
Real-time monitor

With the above operating principle, system could continuously retrieve LED status from serial-out then compare with the last frame data one by one. Once there is any discrepancy ('1'→'0'), we can locate which channel is abnormal precisely. Since the process is ongoing and without shifting between image mode and detection mode, it does not interrupt the image data flow and the output display. The 'real-time monitor' method is suitable for LED Variable Message Signs (VMS) system.
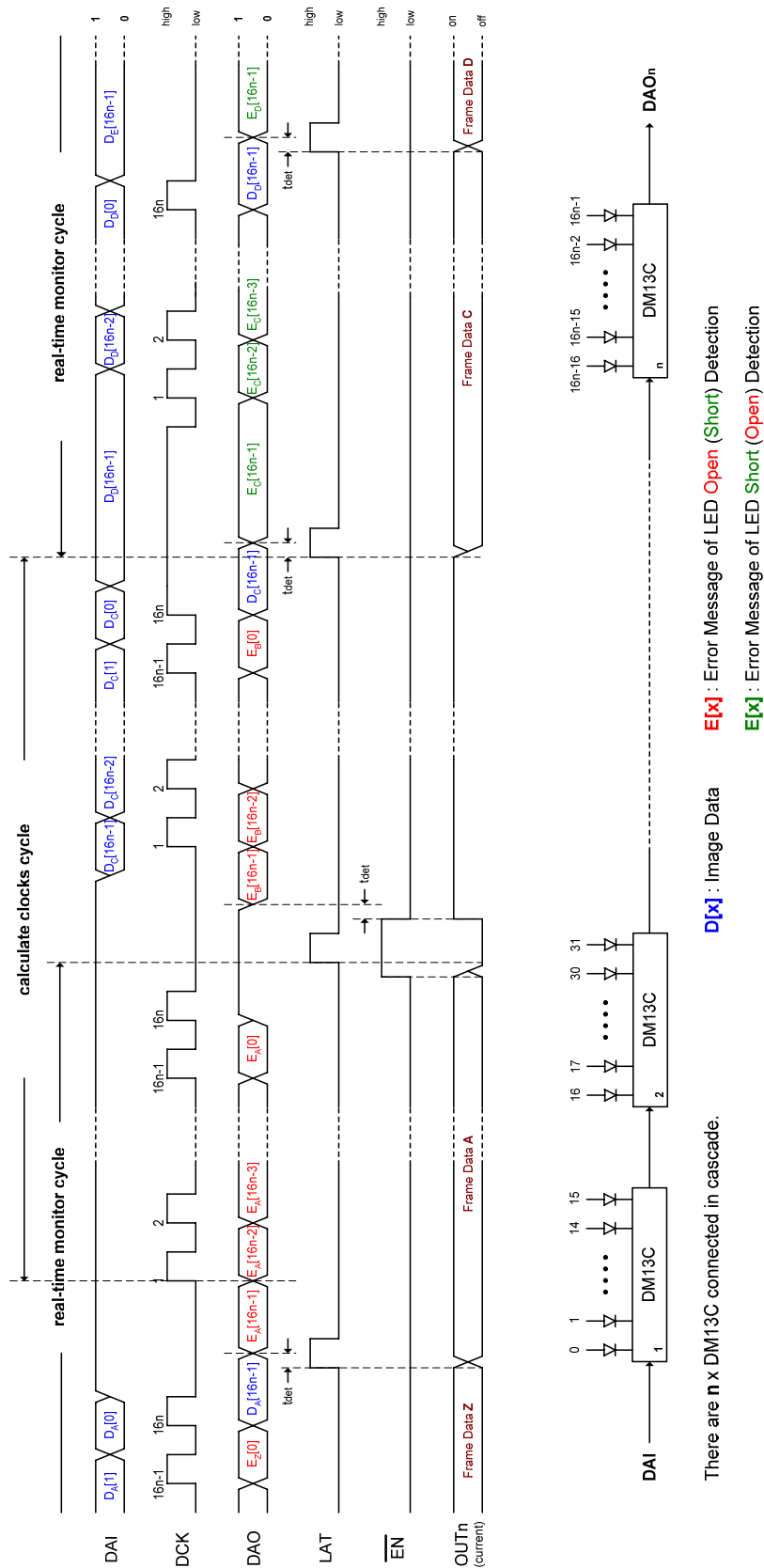
Clocks calculation

For large LED display applications, 'real-time monitor' could be a heavy loading for system because it needs to compare the retrieved information with a lot of frame data. Therefore, to write the image data of all channels to '1', all failure status will be identified when there will be any '0' retrieved. By calculating the numbers of clock pulses, the locations of abnormal channel could be pointed out easily. The "clocks calculation" method helps to minimize the loading and memory resources of system.

Selection of Open/Short Detection

The default detection type provided by DM13C is LED **open** detection after power-on. Users could switch LED open to short detection (or short to open detection) by following timing sequence. There are two alternative options could be selected. The option 1 shows triggering latch pulse when the last clock of the frame data kept at high level. The option 2 shows sending one useless clock pulse which will not shift-in data while the latch signal is kept at high level.


Normal Operation

option 1

Open → Short

or

Short → Open

useless clock pulse does not shift-in data

option 2

Timing Diagram of LED Open/Short Detection

real-time monitor cycle

calculate clocks cycle

real-time monitor cycle

DAI

DCK

DAO

LAT

EN

OUTn (current)

high / low / on / off / 1 / 0

$D_A[1]$ $D_A[0]$ ... $D_C[16n-1]$ $D_C[16n-2]$ $D_C[0]$ $D_C[1]$ ... $D_D[16n-1]$ $D_D[16n-2]$ $D_D[0]$ $D_E[16n-1]$

$E_Z[0]$ $D_A[16n-1]$ $E_A[16n-1]$ $E_A[16n-2]$ $E_A[16n-3]$ $E_A[0]$ $E_B[16n-1]$ $E_B[16n-2]$ $E_B[0]$ $D_C[16n-1]$ $E_C[16n-1]$ $E_C[16n-2]$ $E_C[16n-3]$ $D_D[0]$ $D_D[16n-1]$ $E_D[16n-1]$

Frame Data Z / Frame Data A / Frame Data C / Frame Data D

tdet

16n-1 / 16n / 2 / 1 / 16n-1 / 16n / 2 / 1 / 16n-1 / 16n / 2 / 1 / 16n-1 / 16n

There are **n** x DM13C connected in cascade.

DAI

DM13C 1 — 0 1 ... 14 15

DM13C 2 — 16 17 ... 30 31

DM13C n — 16n-16 16n-15 16n-2 16n-1

DAOn

D[x] : Image Data

E[x] : Error Message of LED Open (Short) Detection

E[x] : Error Message of LED Short (Open) Detection

Threshold of Short Detection

The default threshold voltage for LED short detection of DM13C is 1/2 VCC. One could change the default voltage by switching or setting a new voltage of V$_{LED}$ during short detection is going on. Please see the example below for reference:
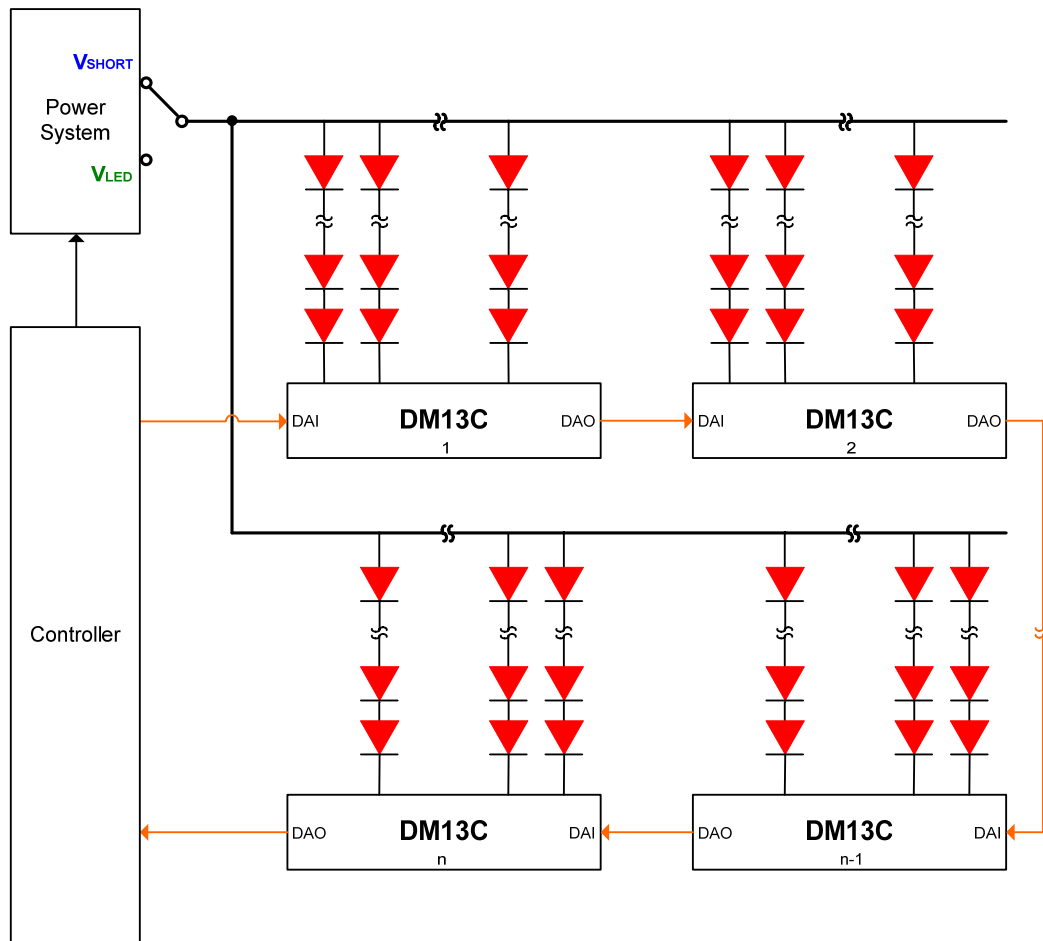
Example for shifting the threshold of LED short detection

Note that the **V$_{SHORT}$** should be satisfied with the following inequality:

$$\frac{1}{2}VCC \ < \ V_{SHORT} \ < \ \frac{1}{2}VCC + V_{F(LED\ forward\ voltage)} \times N_{(Numbers\ of\ LED\ in\ a\ string)}$$

The new threshold voltage of short detection will be equivalent to:

$$\frac{1}{2}VCC + (\ V_{LED} - V_{SHORT}\ )$$

Outputs Delay

Large in-rush currents will occur when the system activates all the outputs at once. To reduce this effect, DM13C is designed to have a constant unit of delay (around 1.5ns) between outputs. The delay for every output goes like this: there is no delay for OUT15 and OUT7, 1 unit of delay for OUT14 and OUT6, 2 units of delay for OUT13 and OUT5 and so on.

Global Brightness Control

DM13C has no built-in global brightness control feature. In order to obtain a lower resolution of global brightness control effect, two methods could be utilized. One is providing PWM signal synchronized on latch pulse to modulate the output enable terminal ($\overline{\text{EN}}$ pin). The other is to adjust the Rrext value or voltage drop across the external resistor. Please see the reference circuit below:
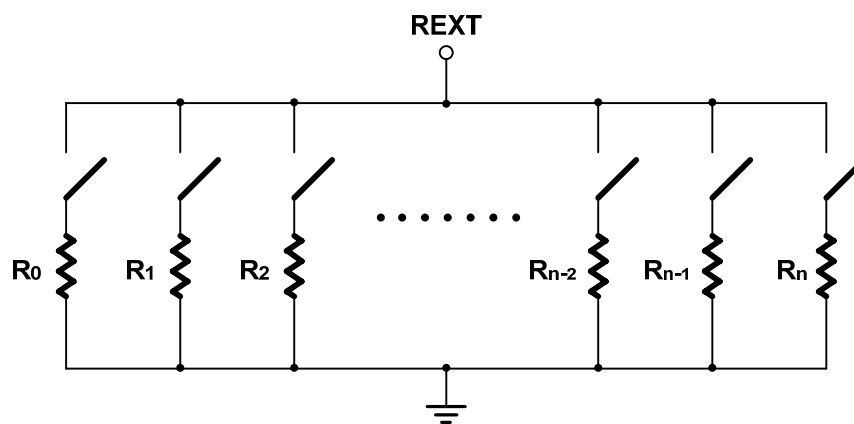
Global Brightness Control with Resistor Ladder
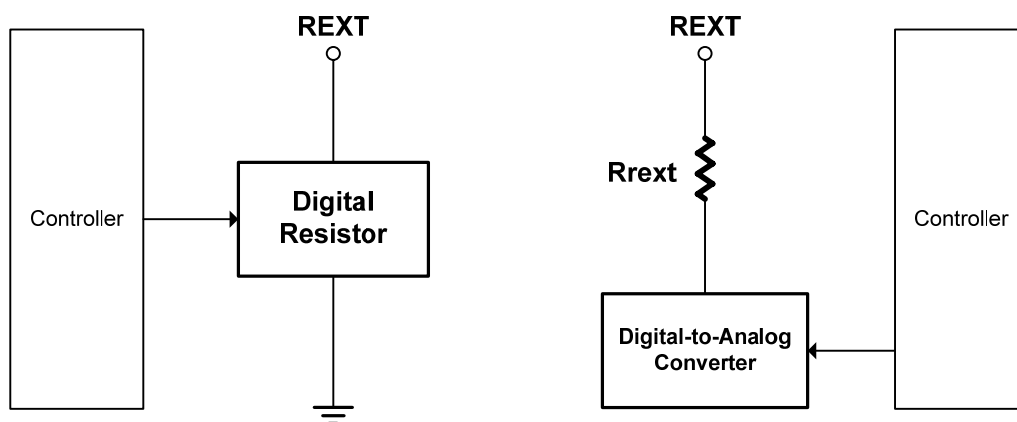

Global Brightness Control with Digital Resistor

Global Brightness Control with D/A converter

Power Dissipation

The power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{Tj(junction\ temperature)(max)(°C) - Ta(ambient\ temperature)(°C)}{Rth(junction\text{-}to\text{-}air\ thermal\ resistance)(°C/Watt)}$$
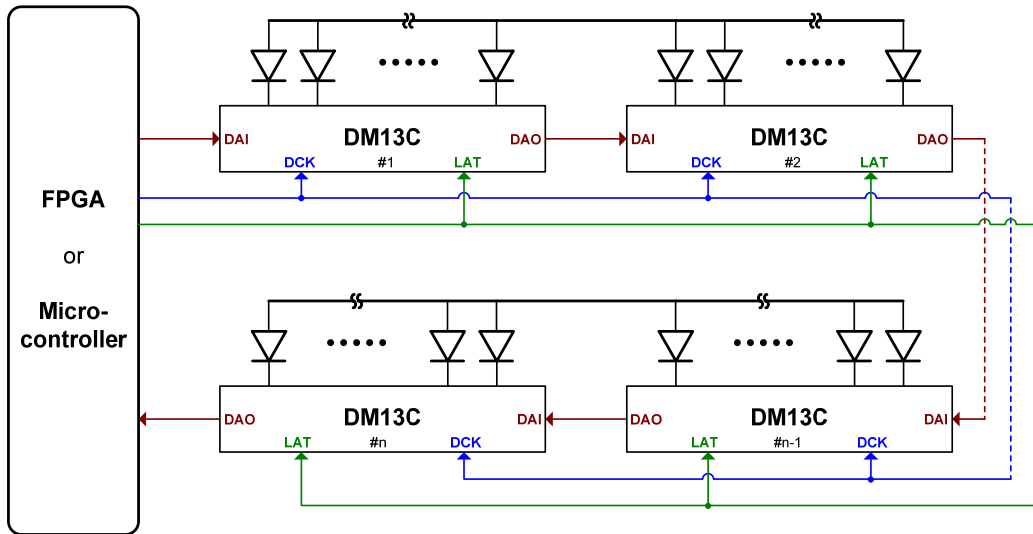
The relationship between power dissipation and operating temperature can be refer to the figure below:
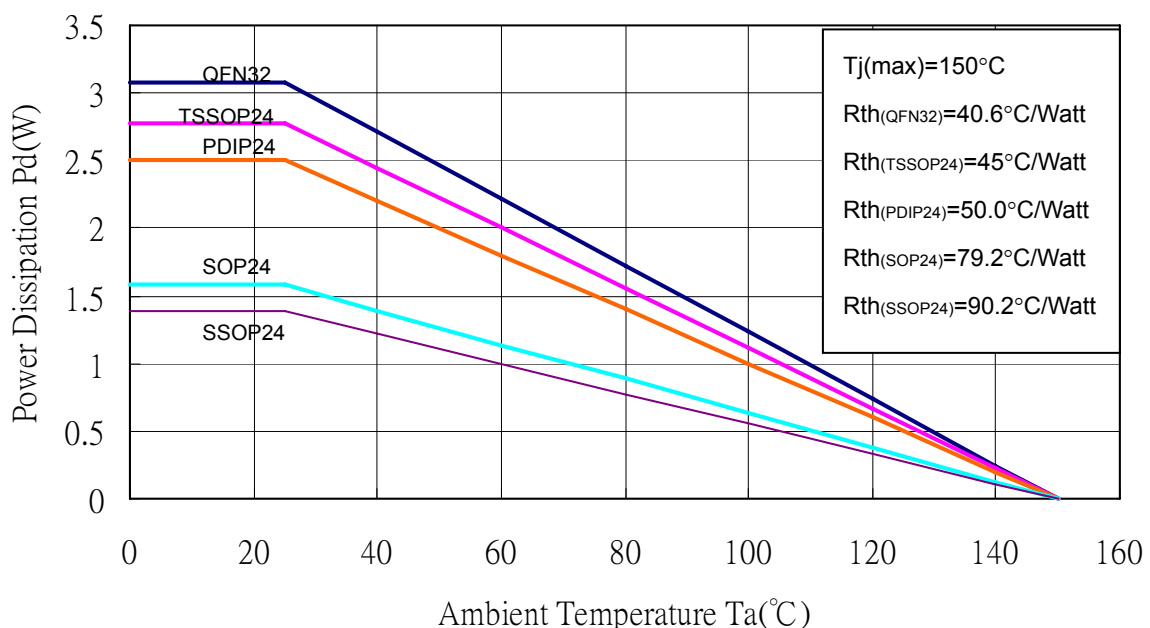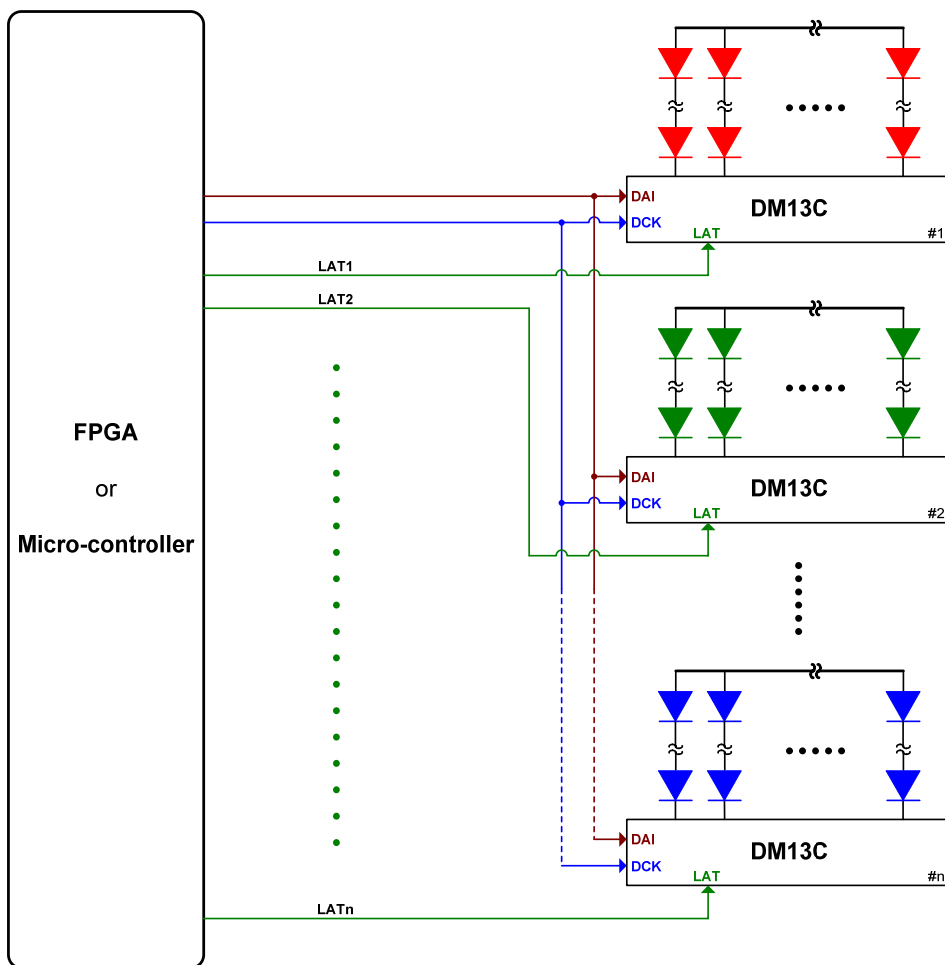

The power consumption of IC can be determined by the following equation and should be less than the maximum allowable power dissipation:

$$Pd(W) = V_{CC}(V) \times I_{DD}(A) + Vout0 \times Iout0 \times Duty0 + \cdots\cdots + Vout15 \times Iout15 \times Duty15 \leq Pd(max)(W)$$
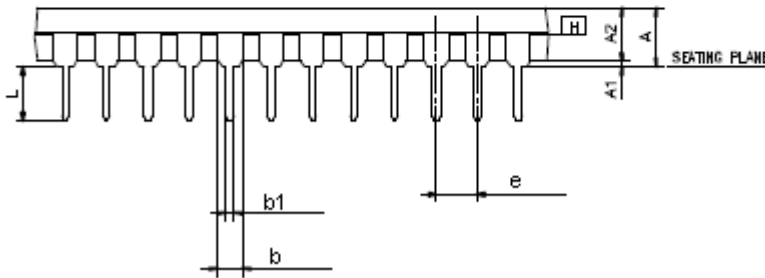

Typical Application

Serial Connection Type

Parallel Connection Type

Package Outline Dimension

DM13C-DIP(Sk)
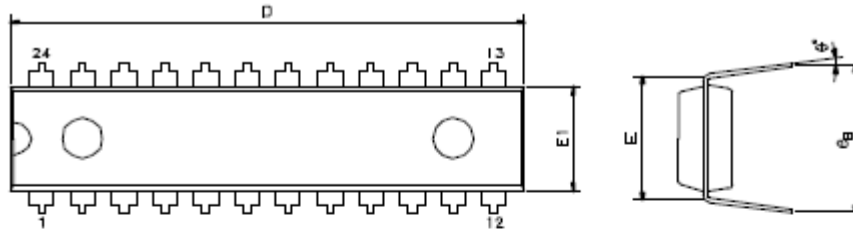
A	-	-	5.334	-	-	0.21
A1	0.381	-	-	0.015	-	-
A2	3.175	3.302	3.429	0.125	0.130	0.135
b	-	1.524	-	-	0.06	-
b1	-	0.457	-	-	0.018	-
D	31.242	31.750	32.512	1.230	1.250	1.280
E	7.620 BSC			0.3 BSC		
E1	6.426	6.553	6.680	0.253	0.258	0.263
e	-	2.540	-	-	0.100	-
eB	8.509	9.017	9.525	0.335	0.355	0.375
L	2.921	3.302	3.810	0.115	0.13	0.150
S	-	-	-	-	-	-
θ°	0	7	15	0	7	15

Package Outline Dimension

DM13C-DIP(Shr)
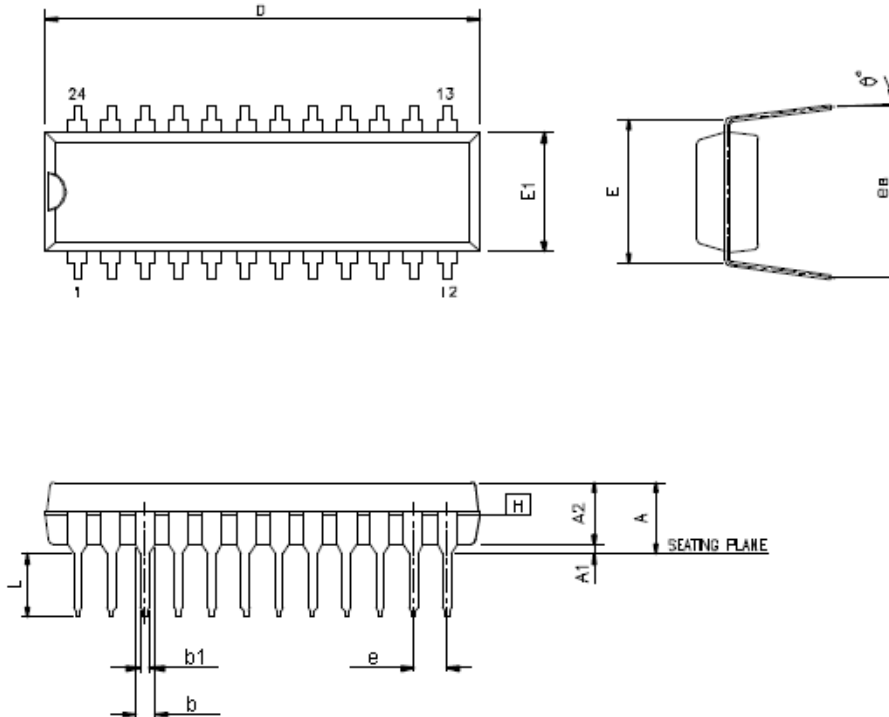
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
A	-	-	5.334	-	-	0.21
A1	0.381	-	-	0.015	-	-
A2	3.175	3.302	3.429	0.125	0.130	0.135
b	-	1.016	-	-	0.04	-
b1	-	0.457	-	-	0.457	-
D	22.352	22.860	23.368	0.880	0.900	0.920
E	7.620 BSC			0.3 BSC		
E1	6.223	6.350	6.477	0.245	0.250	0.255
e	-	1.778	-	-	0.070	-
eB	8.509	9.017	9.525	0.335	0.355	0.375
L	2.921	3.302	3.810	0.115	0.13	0.150
S	-	-	-	-	-	-
θ°	0	7	15	0	7	15

點晶科技股份有限公司
SiTI Silicon Touch Technology Inc.

Package Outline Dimension

DM13C-SSOP
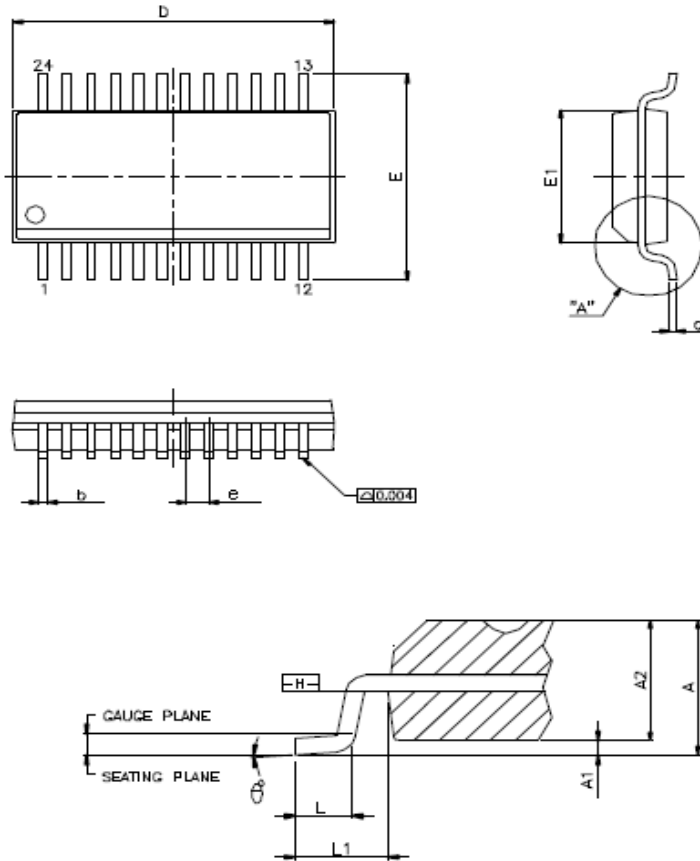
	DIMENSION IN MM			DIMENSION IN INCH		
A	1.346	1.626	1.753	0.053	0.064	0.069
A1	0.102	0.152	0.254	0.004	0.006	0.010
A2	-	-	1.499	-	-	0.059
b	0.203	-	0.305	0.008	-	0.012
C	0.178	-	0.254	0.007	-	0.010
D	8.560	8.661	8.738	0.337	0.341	0.344
E	5.791	5.994	6.198	0.228	0.236	0.244
e	0.635 BSC			0.025 BSC		
E1	3.810	3.912	3.988	0.150	0.154	0.157
L	0.406	0.635	1.270	0.016	0.025	0.050
L1	1.041 BSC			0.0409 BSC		
θ°	0	-	8	0	-	8

Package Outline Dimension

DM13C-SOP
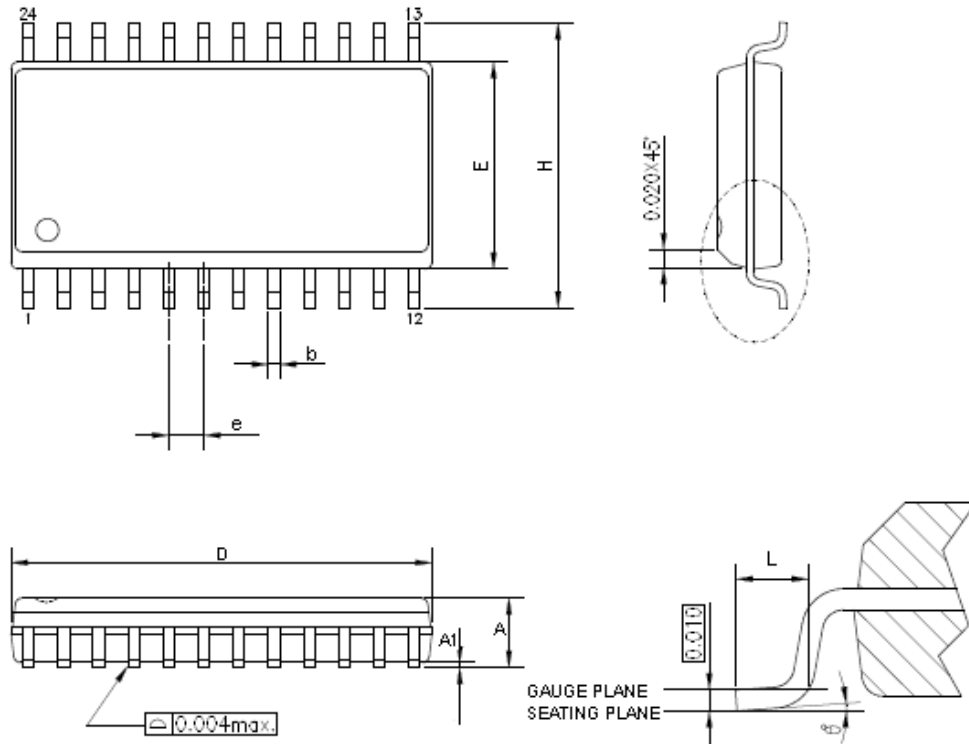
	DIMENSION IN MM			DIMENSION IN INCH		
A	-	-	2.642	-	-	2.642
A1	0.102	-	-	0.102	-	-
b	0.406 BSC			0.406 BSC		
D	15.545	15.697	15.850	15.545	15.697	15.850
E	7.417	7.518	7.595	7.417	7.518	7.595
e	1.270 BSC			1.270 BSC		
H	10.287	10.465	10.643	10.287	10.465	10.643
L	0.533	0.787	1.041	0.533	0.787	1.041
θ°	0	4	8	0	4	8

Package Outline Dimension

DM13C-SOP(1.0)
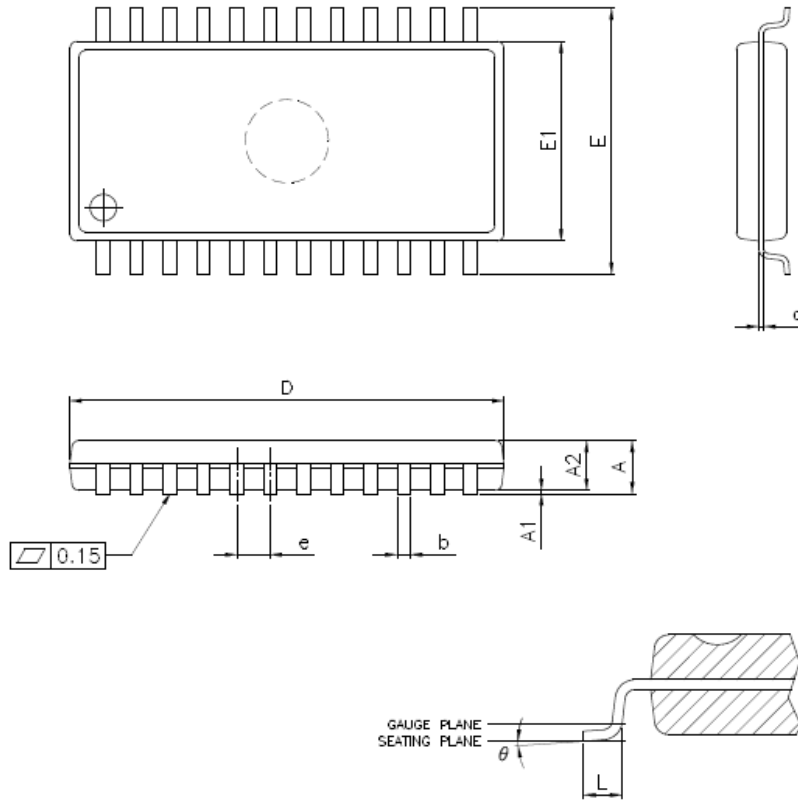
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
A	-	-	1.900	-	-	0.075
A1	0.050	0.100	0.200	0.002	0.004	0.008
A2	1.300	1.500	1.700	0.051	0.059	0.067
b	0.300	0.400	0.500	0.012	0.016	0.020
c	0.100	0.150	0.250	0.004	0.006	0.010
D	12.800	13.000	13.200	0.504	0.512	0.520
E	7.700	8.000	8.300	0.303	0.315	0.327
e	1.000 BSC			0.04 BSC		
E1	5.800	6.000	6.200	0.228	0.236	0.244
L	0.250	0.450	0.650	0.010	0.018	0.026
θ°	0	-	10	0	-	10

Package Outline Dimension

DM13C-TSSOPEX
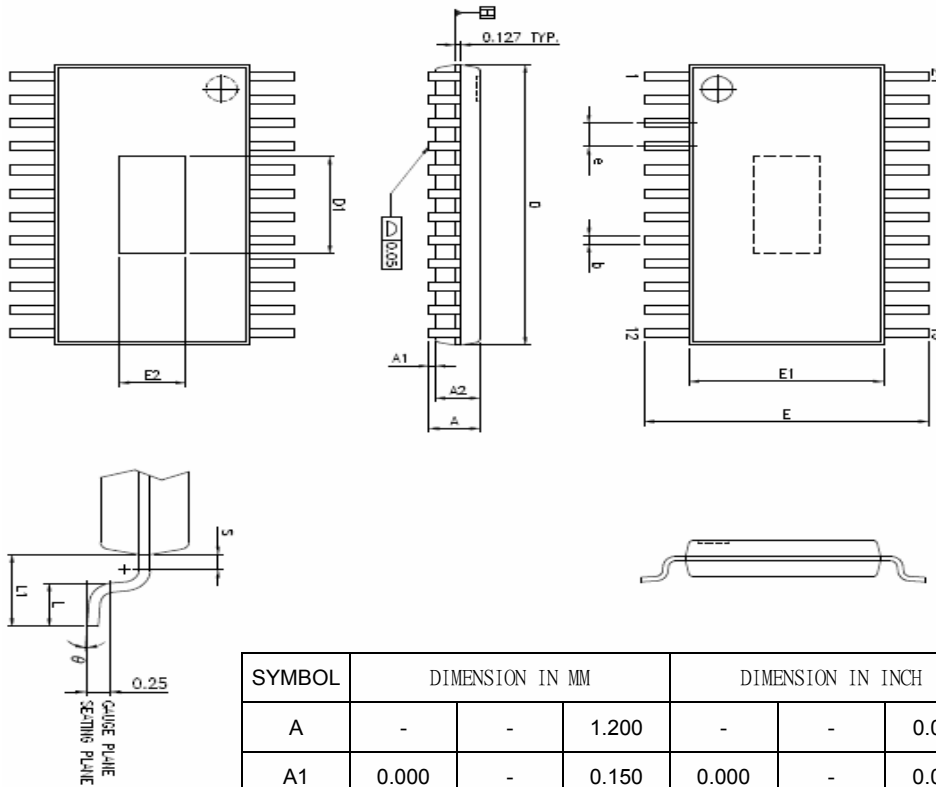
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
A	-	-	1.200	-	-	0.047
A1	0.000	-	0.150	0.000	-	0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190	-	0.300	0.007	-	0.012
D	7.700	7.800	7.900	0.303	0.307	0.311
E1	4.300	4.400	4.500	0.169	0.173	0.177
E	6.400 BSC			0.252 BSC		
e	0.650 BSC			0.0256 BSC		
L1	1.000 REF			0.04 REF		
L	0.450	0.600	0.750	0.018	0.024	0.030
S	0.200	-	-	0.008	-	-
θ°	0	-	8	0	-	8
PAD SIZE1 (74×18E)						
E2	1.500	-	1.880	0.059	-	0.074
D1	3.700	-	4.620	0.146	-	0.182
PAD SIZE2 (112×18E)						
E2	2.280	-	2.850	0.090	-	0.112
D1	3.700	-	4.620	0.146	-	0.182

Package Outline Dimension

QFN32
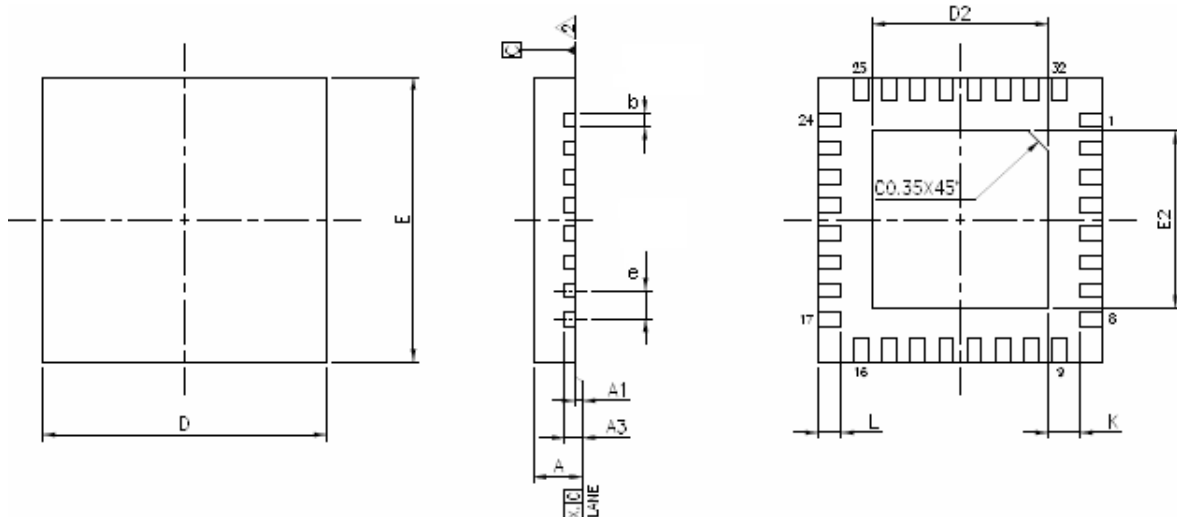
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	0.020	0.050	0.000	0.001	0.002
A3	0.203 REF			0.008 REF		
b	0.180	0.250	0.300	0.007	0.010	0.012
D	4.900	5.000	5.100	0.193	0.197	0.201
E	4.900	5.000	5.100	0.193	0.197	0.201
e	0.500 BSC			0.02 BSC		
L	0.300	0.400	0.500	0.012	0.016	0.020
k	0.200	-	-	0.008	-	-
	EXPOSED PAD			EXPOSED PAD		
D2	1.250	2.700	3.250	0.049	0.106	0.128
E2	1.250	2.700	3.250	0.049	0.106	0.128

Note: 1.DIMENSIONING AND TOLERANCING CONFORM TO ASME Y145.5M-1994.

2. REFER TO JEDEC STD. MO-220 WHHD-2 ISSUE A

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