CMOSTEK

CMT2380F32

Ultra Low Power Sub-1GHz Wireless MCU

MCU Features

- 32 MHz Cortex-M0+ 32-bit CPU platform
- 32 kB Flash with erasing protection
- 4 kB RAM with parity to enhance system stability
- 16 general purpose I/O interfaces available
- Flexible power management system
  - 0.5 uA @ 3 V(deep sleep mode): the power consumption when all clocks are off, power-on reset is active, I/O state is maintained, I/O interrupt is active and all registers, RAM, and CPU stay in data storage status
  - 0.8 uA @ 3 V (deep sleep mode): the power consumption when RTCs work
  - 150 uA/MHz @3 V @16 MHz: the power consumption when CPU and peripheral modules run with program Flash operating internally
  - 2 us: the chip's wakeup time from ultra-low power mode, the fast response enables mode switching more flexible and efficient
- RTC and crystal
  - External high speed crystal: 4 – 32 MHz
  - External low speed crystal: 32.768 kHz
  - Internal high speed clock: 4/8/16/22 and 24 MHz
  - Internal low speed clock: 32.8/38.4 kHz
- Timer and counter
  - 3 general purpose 16-bit timers/counters
  - A 16-bit timer/counter available in low power mode
  - 3 high performance 16-bit timers/counters capable for capture/compare and PWM output
  - One 20-bit programmable counter/watchdog circuit with built-in dedicated ultra-low power RC-OSC to perform WDT counting
- Communication interface
  - UART 0 and UART 1 standard communication interface
  - One ultra-low power UART(LPUART) supporting for low speed clock
  - Standard I2C and SPI communication interface
- One 12-bit 1 Msps SAR ADC
- 2 voltage comparators
- Low voltage detector (LVD), configurable 16-level comparison level, support for port voltage and supply voltage monitoring

RF Features

- Frequency range: 127 – 1020 MHz
- Modem: FSK, GFSK, MSK, GMSK and OOK
- Data rate：0.5 – 300 kbps
- Sensitivity: -121 dBm @ 434 MHz, FSK
- Receiving current: 8.5 mA @ 434 MHz, FSK
- Transmitting current: 72 mA @ 20 dBm, 434 MHz
- Configurable up to 64-byte FIFO

System Features

- Supply voltage：1.8 – 3.6 V
- Operating temperature: -40 – 85 ℃
- QFN40 5x5 packaging

Application

- Smart grid and automatic meter reading
- Home security and building automation
- Wireless sensor networks and industrial monitoring
- ISM band data communication

Description

Employed a 32-bit Cortex-M0+ CPU core and an ultra-low power RF transceiver, the CMT2380F32 is a FSK, GFSK, MSK, GMSK and OOK wireless MCU with high performance and ultra-low power applying to 127 to 1020 MHz band wireless applications. Operating with 1.8 to 3.6 V supply voltage, the CMT2380F32 consumes only 72 mA current while delivering up to 20 dBm power. As for the receiver, the

device consumes an ultra-low current of 8.5 mA with the sensitivity reaching -121 dBm.

The device employs a wide range of peripherals like support of standard UART, I2C and SPI interfaces, up to 16 general-purpose I/Os, support of internal high-speed, low-speed, low-power RC oscillators and 32.768 kHz external crystal oscillators, flexible data handling and packet handler, up to 64-byte Tx/Rx FIFO, feature-enriched RF GPIO, multiple low-power modes and fast-start mechanisms, high-precision RSSI, manual fast frequency hopping, multi-channel input 12-bit high-speed ADC, etc. Leading the industry in the aspect of the smallest package size, the CMT2380F32 is ideal for size constraints due to a small form-factor, power-efficient IoT applications.

Table 1. The CMT2380F32 Resource List

Memory		Analog Peripherals			Digital Peripherals									Others	
ROM	RAM	ADC	VCMP	LVD	RTC	WDT	Timer	CCP PWM	UART	LPUART	SPI	I2C	PCA	CRC	GPIO
32 k	4 k	12-bit x9-ch	2	✓	✓	✓	16-bit x6	16-bit x6-ch	2	1	1	1	✓	✓	16+1

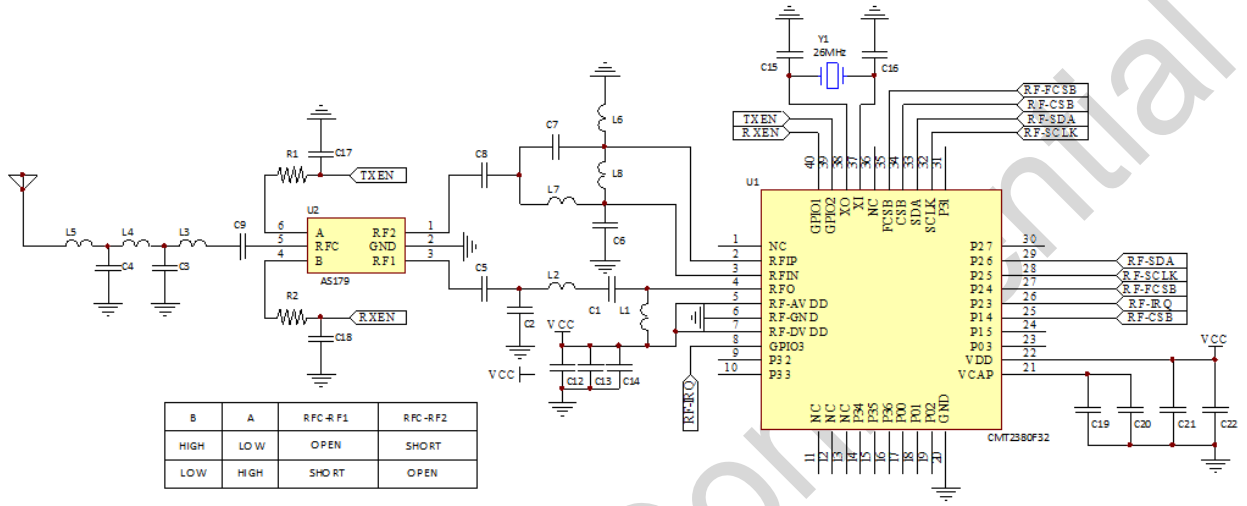

Figure 1. Typical Application Schematic for the CMT2380F32

(20dBm Output Power with Antenna Switch)

Table 2. Typical Application BOM (20 dBm Output Power with Antenna Switch)

Label	Description	Component Value		Unit	Supplier
		434 MHz	868/915 MHz		
C1	± 5%, 0402 NP0, 50 V	15	15	pF	-
C2	± 5%, 0402 NP0, 50 V	10	3.9	pF	-
C3	± 5%, 0402 NP0, 50 V	8.2	2.7	pF	-
C4	± 5%, 0402 NP0, 50 V	8.2	2.7	pF	-
C5	± 5%, 0402 NP0, 50 V	220	220	pF	-
C6	± 5%, 0402 NP0, 50 V	4.7	2	pF	-
C7	± 5%, 0402 NP0, 50 V	4.7	2	pF	-
C8	± 5%, 0402 NP0, 50 V	220	220	pF	-
C9	± 5%, 0402 NP0, 50 V	220	220	pF	-
C12	± 5%, 0402 NP0, 50 V	470		pF	-
C13	± 20%, 0402 X7R, 25 V	2.2		nF	-

Label	Description	Component Value		Unit	Supplier
		434 MHz	868/915 MHz		
C14	± 20%, 0603 X7R, 25 V	4.7		uF	-
C15	± 5%, 0402 NP0, 50 V	27		pF	-
C16	± 5%, 0402 NP0, 50 V	27		pF	-
C17	± 5%, 0402 NP0, 50 V	10		pF	-
C18	± 5%, 0402 NP0, 50 V	10		pF	-
C19	± 20%, 0402 X7R, 25 V	100		nF	-
C20	± 20%, 0603 X7R, 25 V	4.7		uF	-
C21	± 20%, 0402 X7R, 25 V	100		nF	-
C22	± 5%, 0402 NP0, 50 V	470		pF	-
L1	± 10%, 0603multilayer chip inductor	180	100	nH	Sunlord SDCL
L2	± 10%, 0603 multilayer chip inductor	27	6.8	nH	Sunlord SDCL
L3	± 10%, 0603 multilayer chip inductor	18	12	nH	Sunlord SDCL
L4	± 10%, 0603 multilayer chip inductor	33	22	nH	Sunlord SDCL
L5	± 10%, 0603 multilayer chip inductor	15	10	nH	Sunlord SDCL
L6	± 10%, 0603 multilayer chip inductor	27	12	nH	Sunlord SDCL
L7	± 10%, 0603 multilayer chip inductor	27	12	nH	Sunlord SDCL
L8	± 10%, 0603 multilayer chip inductor	68	18	nH	Sunlord SDCL
Y1	± 10 ppm, SMD32*25 mm	26		MHz	EPSON
U1	CMT2380F32, ultra-low power sub-1GHz wireless MCU	-		-	CMOSTEK
U2	AS179, PHEMT GaAs IC SPDT Switch	-		-	SKYWORKS
R1	± 5%, 0402	2.2		kΩ	-
R2	± 5%, 0402	2.2		kΩ	-

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1 Electrical Specifications

V_{DD}= 3.3 V，T_{OP}= 25 °C，F_{RF} = 433.92 MHz, sensitivity is measured by receiving a PN9 sequence and matching to 50 Ω impedance, 0.1% BER if nothing else stated. All measurement results are obtained using the evaluation board CMT2380F32-EM if nothing else stated.

1.1 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		-40		85	℃
Operating speed		CPU frequency range	256k	4M	32 M	Hz
RF supply voltage slope	V_{RF-PSR}		1			mV/us
Controller supply voltage	$V_{MCU-PSR}$		50			mV/us
Controller power-on reset effective voltage	$V_{MCU-POR}$				0.1	V

1.2 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min.	Typ.	Max.
Supply voltage	V_{DD}		-0.3	3.6	V
Interface voltage	V_{IN}		-0.3	3.6	V
Junction temperature	T_J		-40	125	℃
Storage temperature	T_{STG}		-50	150	℃
Soldering temperature	T_{SDR}	Lasts for at least 30 seconds		255	℃
ESD rating[2]		Human body model (HBM)	-2	2	kV
Latch-up current		@ 85 ℃	-100	100	mA

Notes:

[1]. Exceeding *the Absolute Maximum Ratings* may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT2380F32 is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good ESD protection.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

1.3 RF Power Consumption

Table 5. RF Power Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep current	I_{SLEEP}	Sleep mode, sleep counter off		300		nA
		Sleep mode ,sleep counter on		800		nA
Standby current	$I_{Standby}$	Crystal oscillator on		1.45		mA
RFS current	I_{RFS}	433 MHz		5.7		mA
		868 MHz		5.8		mA
		915 MHz		5.8		mA
TFS current	I_{TFS}	433 MHz		5.6		mA
		868 MHz		5.9		mA
		915 MHz		5.9		mA
FSK, RX current (high performance)	I_{Rx-HP}	433 MHz, 10 kbps,10 kHz F_{DEV}		8.5		mA
		868 MHz, 10 kbps, 10 kHz F_{DEV}		8.6		mA
		915 MHz, 10 kbps,10 kHz F_{DEV}		8.9		mA
FSK, RX current (low power mode)	I_{Rx-LP}	433 MHz, 10 kbps, 10 kHz F_{DEV}		7.2		mA
		868 MHz, 10 kbps, 10 kHz F_{DEV}		7.3		mA
		915 MHz, 10 kbps, 10 kHz F_{DEV}		7.6		mA
FSK, TX current	I_{Tx}	433 MHz, +20 dBm (Direct-tie)		72		mA
		433 MHz, +20 dBm (With RF switch)		77		mA
		433 MHz, +13 dBm (Direct-tie)		23		mA
		433 MHz, +10 dBm (Direct-tie)		18		mA
		433 MHz, -10 dBm (Direct-tie)		8		mA
		868 MHz, +20dBm (Direct-tie)		87		mA
		868 MHz, +20dBm (With RF switch)		80		mA
		868 MHz, +13 dBm (Direct-tie)		27		mA
		868 MHz, +10 dBm (Direct-tie)		19		mA
		868 MHz, -10 dBm (Direct-tie)		8		mA
		915 MHz, +20 dBm (Direct-tie)		70		mA
		915 MHz, +20 dBm (Direct-tie)		75		mA
		915 MHz, +13 dBm (Direct-tie)		28		mA
		915 MHz, +10 dBm (Direct-tie)		19		mA
		915 MHz, +10 dBm (Direct-tie)		8		mA

1.4 Receiver

Table 6. Receiver Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Rate	DR	OOK	0.5		40	kbps
		FSK and GFSK	0.5		300	kbps
Error	F_{DEV}	FSK and GFSK	2		200	kHz
Sensitivity @ 433 MHz	$S_{433\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-121		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-116		dBm
		DR = 10 kbps, F_{DEV}= 10 kHz (low power mode)		-115		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-113		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz (low power mode)		-112		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-111		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-108		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-105		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-103		dBm
Sensitivity @ 868 MHz	$S_{868\text{-}HP}$	DR = 2 kbps, F_{DEV} = 10 kHz		-119		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz (low power mode)		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz (low power mode)		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-108		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-99		dBm
Sensitivity @ 915 MHz	$S_{915\text{-}HP}$	DR = 2 kbps, F_{DEV} = 10 kHz		-117		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz(low power mode)		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz (low power mode)		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-99		dBm
Saturation	P_{LVL}				20	dBm
Image rejection ratio	IMR	F_{RF} = 433 MHz		35		dBc
		F_{RF} = 868 MHz		33		dBc
		F_{RF} = 915 MHz		33		dBc
Receive channel bandwidth	BW	Receive channel bandwidth	50		500	kHz
Co-channel rejection	CCR	DR = 10 kbps, F_{DEV} = 10 kHz Interference with the same modulation		-7		dBc

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Adjacent channel rejection	ACR-I	DR = 10 kbps, F_{DEV} = 10 kHz, BW = 100 kHz, 200 kHz channel spacing, interference with the same modulation		30		dBc
Alternate channel rejection	ACR-II	DR = 10 kbps, F_{DEV} = 10 kHz, BW=100kHz, 400 kHz channel spacing, interference with the same modulation		45		dBc
Blocking	BI	DR = 10 kbps, F_{DEV} = 10 kHz, ±1 MHz offset, continuous wave interference		70		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz, ± 2 MHz offset, continuous wave interference		72		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz, ±10 MHz offset, continuous wave interference		75		dBc
Input 3rd order intercept point	IIP3	DR = 10 kbps, F_{DEV} = 10 kHz, 1 MHz and 20 MHz offset two tone test, maximum system gain setting		-25		dBm
RSSI range	RSSI		-120		20	dBm
Sensitivity @ 433.92 MHz (typical configuration)		DR = 1.2 kbps, F_{DEV} = 5 kHz		-122.9		dBm
		DR = 1.2 kbps, F_{DEV} = 10kHz		-121.8		dBm
		DR = 1.2 kbps, F_{DEV} = 20 kHz		-119.5		dBm
		DR = 2.4 kbps, F_{DEV} = 5 kHz		-120.6		dBm
		DR = 2.4 kbps, F_{DEV} = 10 kHz		-120.3		dBm
		DR = 2.4 kbps, F_{DEV} = 20 kHz		-119.7		dBm
		DR = 9.6 kbps, F_{DEV} = 9.6 kHz		-116.0		dBm
		DR = 9.6 kbps, F_{DEV} = 19.2 kHz		-116.1		dBm
		DR = 20 kbps, F_{DEV} = 10 kHz		-114.2		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-113.0		dBm
		DR = 50 kbps, F_{DEV}= 25 kHz		-110.6		dBm
		DR = 50 kbps, F_{DEV} = 50 kHz		-109.0		dBm
		DR = 100 kbps, F_{DEV} = 50 kHz		-107.8		dBm
		DR = 200 kbps, F_{DEV}= 50 kHz		-103.5		dBm
		DR = 200 kbps, F_{DEV} = 100 kHz		-104.3		dBm
		DR = 300 kbps, F_{DEV} = 50 kHz		-98.0		dBm
		DR = 300 kbps, F_{DEV} = 150 kHz		-101.6		dBm

1.5 Transmitter

Table 7. Transmitter Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power	P_{OUT}	Specific matching network is required for different frequency bands	-20		+20	dBm
Output power step	P_{STEP}			1		dB
GFSK (Gaussian filter coefficient)	BT		0.3	0.5	1.0	-
Output power change with different temperature	$P_{OUT-TOP}$	Temperature range:-40 to + 85 °C		1		dB
Spurious emissions		P_{OUT} = +13 dBm,433MHz, F_{RF}<1 GHz			-54	dBm
		1 GHz to12.75 GHz, including harmonics			-36	dBm
Harmonic output[1] for F_{RF}= 433 MHz	$H2_{433}$	2nd harmonic,+20 dBm P_{OUT}		- 46		dBm
	$H3_{433}$	3nd harmonic,+20 dBm P_{OUT}		- 50		dBm
Harmonic output[1] for F_{RF}= 868 MHz	$H2_{868}$	2nd harmonic,+20 dBm P_{OUT}		- 43		dBm
	$H3_{868}$	3nd harmonic,+20 dBm P_{OUT}		- 52		dBm
Harmonic output[1] for F_{RF}= 915 MHz	$H2_{915}$	2nd harmonic,+20 dBm P_{OUT}		- 48		dBm
	$H3_{915}$	3nd harmonic,+20 dBm P_{OUT}		- 53		dBm
Harmonic output[1] for F_{RF}= 433 MHz	$H2_{433}$	2nd harmonic,+13 dBm P_{OUT}		- 52		dBm
	$H3_{433}$	3nd harmonic,+13 dBm P_{OUT}		- 52		dBm
Harmonic output[1] for F_{RF}= 868 MHz	$H2_{868}$	2nd harmonic,+13 dBm P_{OUT}		- 52		dBm
	$H3_{868}$	3nd harmonic,+13 dBm P_{OUT}		- 52		dBm
Harmonic output[1] for F_{RF}= 915 MHz	$H2_{915}$	2nd harmonic,+13 dBm P_{OUT}		- 52		dBm
	$H3_{915}$	3nd harmonic,+13 dBm P_{OUT}		- 52		dBm

Notes:

[1]. The harmonic level mainly depends on the matching network. Above parameters are measured based on the CMT2380F32-EM, users may get different results on their applications.

1.6 RF Operating Mode Switching Time

Table 8. RF Operating Mode Switching Time

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
RF operating mode switching time	T_{SLP-RX}[1]	From sleep to RX		1		ms
	T_{SLP-TX}[1]	From sleep to TX		1		ms
	T_{STB-RX}	From standby to RX		350		us
	T_{STB-TX}	From standby to TX		350		us
	T_{RFS-RX}	From RFS to RX		20		us
	T_{TFS-RX}	From TFS to TX		20		us
	T_{TX-RX}	From TX to RX (Needs $2T_{symbol}$ to ramp down)		$2T_{symbol}$ +350		us
	T_{RX-TX}	From RX to TX		350		us

Notes:

[1]. T_{SLP-RX} and T_{SLP-TX} are dominated by the crystal oscillator startup time, and the start-up time is to a large degree crystal dependent.

1.7 RF Frequency Synthesizer

Table 9. RF Frequency Synthesizer

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}		760		1020	MHz
			380		510	MHz
			190		340	MHz
			127		170	MHz
Frequency resolution	F_{RES}			25		Hz
Frequency tuning time	t_{TUNE}			150		us
Phase noise @ 433 MHz	PN_{433}	10 kHz deviation		-94		dBc/Hz
		100 kHz deviation		-99		dBc/Hz
		500 kHz deviation		-118		dBc/Hz
		1MHz deviation		-127		dBc/Hz
		10 MHz deviation		-134		dBc/Hz
Phase noise @ 868 MHz	PN_{868}	10 kHz deviation		-92		dBc/Hz
		100 kHz deviation		-95		dBc/Hz
		500 kHz deviation		-114		dBc/Hz
		1MHz deviation		-121		dBc/Hz
		10 MHz deviation		-130		dBc/Hz
Phase noise @ 915 MHz	PN_{915}	10 kHz deviation		-89		dBc/Hz
		100 kHz deviation		-92		dBc/Hz
		500 kHz deviation		-111		dBc/Hz
		1MHz deviation		-121		dBc/Hz
		10 MHz deviation		-130		dBc/Hz

1.8 Requirement on Crystals for RF Section

Table 10. Requirement on Crystals for RF Section

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Crystal frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
ESR	Rm			60		Ω
Crystal startup time[3]	t_{XTAL}			400		us

Notes:

[1]. An external 26 MHz reference clock can be used to drive the XI pin directly through a coupling capacitor if such a clock is available. The peak-to-peak level of the external reference clock is required between 0.3 and 0.7 V.

[2]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF tolerance between the receiver and its paired transmitter.

[3]. This parameter is to a large degree crystal dependent.

1.9 Controller Output Features

Table 11. Controller Output Features

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output high level	V_{OH}	Sourcing 4 mA current, V_{DD} = 3.3V	V_{DD} - 0.25			V
		Sourcing 6 mA current, V_{DD}= 3.3V	V_{DD} - 0.60			V
Output low level	V_{OL}	Sinking 4 mA current, V_{DD} = 3.3V			V_{DD} + 0.25	V
		Sinking 6 mA current, V_{DD}= 3.3V			V_{DD} + 0.60	V
Output high level (enhanced mode)	V_{OHD}	Sourcing 8 mA current, V_{DD} = 3.3V	V_{DD} - 0.25			V
		Sourcing 12 mA current, V_{DD} = 3.3V	V_{DD} - 0.60			V
Output low level (enhanced mode)	V_{OLD}	Sinking 8 mA current, V_{DD} = 3.3V			V_{DD} + 0.25	V
		Sinking 12 mA current, V_{DD} = 3.3V			V_{DD} + 0.60	V

Notes:

1. The maximum total current of I_{OH} and I_{OL} (sum of all pins) shall not exceed 40 mA to meet the specified maximum voltage drop.
2. The maximum total current of I_{OH} and I_{OL} (sum of all pins, enhanced mode) shall not exceed 100 mA to meet the specified maximum voltage drop.

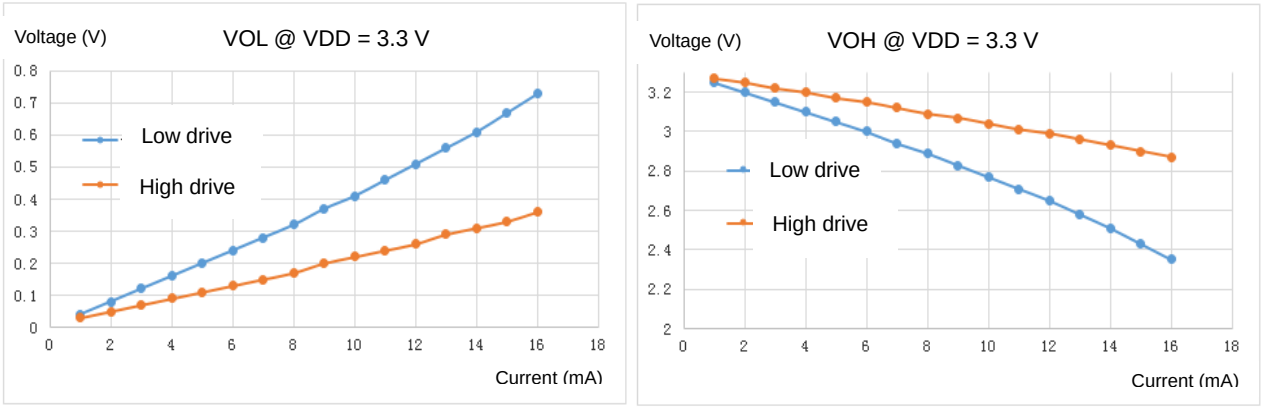


Figure 2. Controller I/O Driving Ability

1.10 Controller Input Features（P0, P1, P2 and P3 Reset)

Table 12. Controller Input Features（P0, P1, P2 and P3 Reset)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output high level	V_{IH}	V_{DD} = 1.8 V	1	1.1	1.2	V
		V_{DD} = 3.3 V	1.8	2	2.2	V
Output low level	V_{IL}	V_{DD} = 1.8 V	0.6	0.7	0.8	V
		V_{DD} = 3.3 V	1.1	1.3	1.5	V
Input hysteresis range (V_{IH}-V_{IL})	V_{HYS}	V_{DD} = 1.8 V	0.4	0.4	0.4	V
		V_{DD} = 3.3 V	0.7	0.7	0.7	V
Pull-up resistor	R_{PUP}	Pull-up enabled		80		kΩ
Input capacitance		Sinking 12 mA current，V_{DD} = 3.3 V		5		pF

1.11 Port External Input Sampling Requirements (Timer Gate/Timer Clock)

Table 13. Port External Input Sampling Requirements (Timer Gate/Timer Clock)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt input pulse width	T_{INT}	V_{DD} = 1.8 V	30[1]			ns
		V_{DD} = 3.3 V	30[1]			ns
Timer 4/5/6 capture pulse width (F_{SYS}=4MHz)	T_{CAP}	V_{DD} = 1.8 V	0.5			us
		V_{DD} = 3.3 V	0.5			us
Timer 0/1/2/4/5/6 external clock input (F_{SYS}=4MHz)	T_{CLK}	V_{DD} = 1.8 V			PCLK/2	MHz
		V_{DD} = 3.3 V			PCLK/2	MHz
PCA external input clock	T_{PCA}	V_{DD} = 1.8 V			PCLK/8	MHz
		V_{DD} = 3.3 V			PCLK/8	MHz

Notes:

[1]. It's the minimum external interrupt input pulse width used in the practical test for triggering the interrupt. It can support triggering the interrupt with even shorter pulse width based on the chip capability.

1.12 Port Leakage Features (P0, P1, P2 and P3)

Table 14. Port Leakage Features (P0, P1, P2, and P3)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Leakage current	$I_{lkg(Px,y)}$	V_{DD}: 1.8 to 3.6V			± 50	nA
Notes: [1]. Unless otherwise specified, the leakage current is measured with GND or VDD applied to the corresponding pin. [2]. The pin to be tested must be set to input mode.						

1.13 Controller Power Consumption Features

Table 15. Controller Power Consumption Features

Parameter	Symbol	Condition	Note	Typ.	Max.	Unit
Operating current when program running in SRAM	I_{DD-RAM}	V_{CORE} = 1.55 V, V_{DD} = 3.3 V. All peripheral clock sources are off. Run While(1) in SRAM with RCH as clock source.	4 MHz	220		uA
			8 MHz	400		uA
			16 MHz	740		uA
			24 MHz	1080		uA
			32 MHz	1400		uA
Core mark operating current	$I_{DD-Mark}$	V_{CORE} = 1.55 V, V_{DD} = 3.3 V. All peripheral clock sources are off. Run Core Mark in Flash with RCH as clock source	4 MHz	670		uA
			8 MHz	1300		uA
			16 MHz	2380		uA
			24 MHz	3410		uA
			32 MHz Flash Wait=1	3530		uA
Operating current	I_{RUN}	V_{CORE} = 1.55 V, V_{DD} = 3.3 V. All peripheral clock sources are on. Run While(1) in Flash with RCH as clock source.	4 MHz	700	880	uA
			8 MHz	1350	1600	uA
			16 MHz	2500	3000	uA
			24 MHz	3600	4300	uA
		V_{CORE} = 1.55 V, V_{DD} = 3.3 V. All peripheral clock sources are off. Run While(1) in Flash with RCH as clock source.	4 MHz	550	750	uA
			8 MHz	1050	1300	uA
			16 MHz	1900	2400	uA
			24 MHz	2700	3300	uA
			32 MHz Flash Wait=1	2850	3000	uA
Sleep current	I_{SLP}	V_{CORE} = 1.55 V， V_{DD} = 1.8~3.6 V.	4 MHz	260	280	uA

Parameter	Symbol	Condition	Note	Typ.	Max.	Unit
		All peripheral clock sources are on with RCH as clock source.	8 MHz	500	520	uA
			16 MHz	950	970	uA
			24 MHz	1400	1420	uA
		V_{CORE} = 1.55 V, V_{DD} = 1.8 ~ 3.6 V. All peripheral clock sources are off. RCH clock source is used.	4 MHz	110	125	uA
			8 MHz	190	210	uA
			16 MHz	330	360	uA
			24 MHz	470	500	uA
			32 MHz	580	610	uA
LP operating current	I_{LP-RUN}	V_{CORE} = 1.55 V, V_{DD} = 1.8 ~ 3.6 V. All peripheral clock sources are on. Run While(1) in Flash with XTAL (32768Hz, Driver = 1) as clock source.	TA = -40 ~ 25 ℃	7	9	uA
			TA = 50 ℃	7.3	9.2	uA
			TA = 85 ℃	8.9	11.3	uA
	I_{LP-RUN}	V_{CORE} = 1.55V, V_{DD} = 1.8 ~ 3.6 V. All peripheral clock sources are off. Run While(1) in Flash with XTAL (32768 Hz, Driver = 1) as clock source.	TA = - 40 ~ 25 ℃	6	8	uA
			TA = 50 ℃	6.1	8.2	uA
			TA = 85 ℃	7.7	10.1	uA
LP sleep current	I_{LP-SLP}	V_{CORE} = 1.55 V, V_{DD} = 1.8 ~ 3.6 V. All peripheral clock sources are on. Run While(1) in Flash with XTAL (32768 Hz, Driver = 1) as clock source.	TA = - 40 ~ 25 ℃	3.3	3.5	uA
			TA = 50 ℃	3.6	3.8	uA
			TA = 85 ℃	5.4	5.8	uA
	I_{LP-SLP}	V_{CORE} = 1.55 V, V_{DD} = 1.8 ~ 3.6 V. All peripheral clock sources are off (except LPTimer and RTC). Run While(1) in Flash with XTAL (32768Hz, Driver = 1) as clock source.	TA = - 40 ~ 25 ℃	2.2	2.4	uA
			TA = 50 ℃	2.5	2.6	uA
			TA = 85 ℃	4.2	4.6	uA
Deep sleep current	$I_{DEEP-SLP}$	V_{CORE} = 1.55 V, V_{DD} = 1.8 ~ 3.6 V. All peripheral clock sources are off, except LPTimer, WDT and RTC.	TA = - 40 ~ 25 ℃	1.5	1.65	uA
			TA = 50 ℃	1.85	2.2	uA
			TA = 85 ℃	3.5	4.2	uA
		V_{CORE} = 1.55 V, V_{DD} = 1.8 ~ 3.6 V. All peripheral clock sources are off, except WDT.	TA = - 40 ~ 25 ℃	1.2	1.3	uA
			TA = 50 ℃	1.5	1.8	uA
			TA = 85 ℃	3.1	3.7	uA
		V_{CORE} = 1.55 V, V_{DD} = 1.8 ~ 3.6 V. All peripheral clock sources are off, except LPTimer.	TA = - 40 ~ 25 ℃	0.9	1	uA
			TA = 50 ℃	1.1	1.3	uA
			TA = 85 ℃	2.6	3	uA

Parameter	Symbol	Condition	Note	Typ.	Max.	Unit
		V_{CORE} = 1.55 V, V_{DD} = 1.8~3.6V. All peripheral clock sources are off, except RTC.	TA = - 40 ~ 25 ℃	1.0	1.1	uA
			TA = 50 ℃	1.2	1.5	uA
			TA = 85 ℃	2.6	3.4	uA
		V_{CORE} = 1.55 V,V_{DD} = 1.8 ~ 3.6 V. All peripheral clock sources are off.	TA = - 40 ~ 25 ℃	0.42	0.6	uA
			TA = 50 ℃	0.75	0.95	uA
			TA = 85 ℃	2.2	2.7	uA

1.14 POR/BOR Features

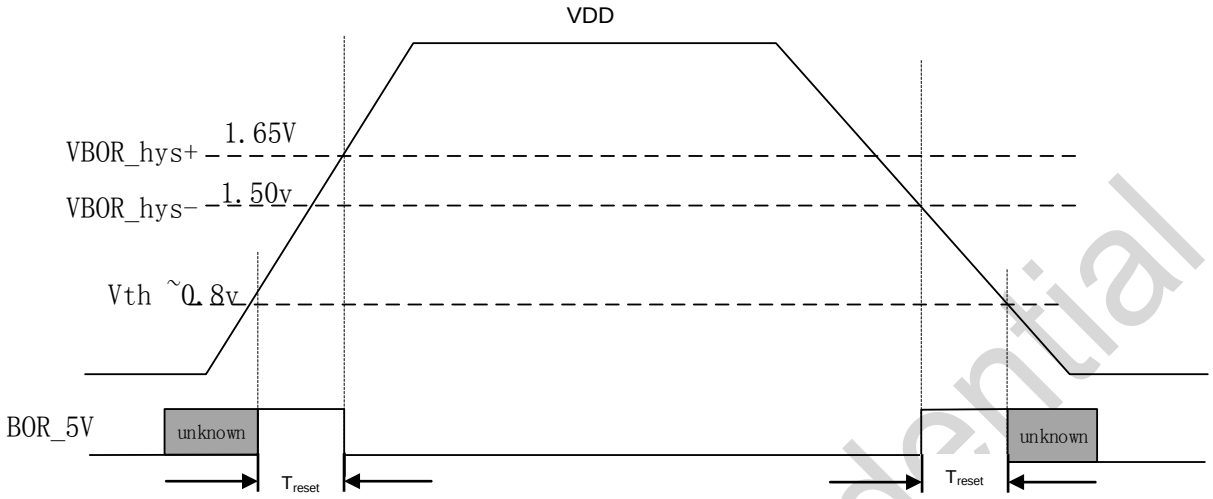


Figure 3. POR/BOR Features

Notes:

1. POR/BOR detects the VDD voltage.
2. It detects the threshold only instead of VDD power-up and power-down slew rate.
3. The detection threshold is the same no matter the VDD is powering on or off. A reset pulse is triggered when VDD is lower than the threshold.
4. In case a reset pulse is generated, the pulse duration will not be less than T_{reset} to guarantee a complete system reset.

Table 16. POR/BOR Features

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
POR release voltage (power-up process)BOR detection voltage (power-down process)	V_{POR}		1.45	1.50	1.65	V

1.15 Controller External XTH Oscillator

Table 17. Controller External XTH Oscillator

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency	F_{FCLK}		4		32	MHz
Equivalent series resistance	ESR_{FCLK}	32 MHz crystal		30	60	Ω
		4 MHz crystal		400	1500	Ω
Load capacitance	C_{FCLK}	The two pins of the crystal oscillator are connected separately.	12		24	pF
Duty cycle	DC_{FCLK}		40	50	60	%
Current consumption[1]	I_{DD}	32 MHz crystal, C_{FCLK}= 12 pF, ESR_{FCLK} = 30 Ω		600		uA
Startup time	T_{Fstart}	4 MHz~32 MHz	200		400	us

Notes:

[1]. It is the current consumption when configure XTH_CR_Driver = 0b1110.

1.16 Controller External 32.768 kHz Oscillator

Table 18. Controller External 32.768 kHz Oscillator

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency	F_{SCLK}			32.768		kHz
Equivalent series resistance	ESR_{SCLK}			65	85	kΩ
Load capacitance	C_{SCLK}	The two pins of the crystal oscillator are connected separately.	0	12		pF
Clock duty cycle	DC_{FCLK}		40	50	60	%
Current consumption[1]	I_{DD}	C_{SCLK} =12pF,ESR_{SCLK} = 65kΩ		0.6	1	uA
Startup time	T_{start}	C_{SCLK} =12pF,ESR_{SCLK} = 65 kΩ,40%~60% duty cycle		500		ms

Notes:

[1]. The operating current is measured under the condition at XTL_CR_Driver = 0b0011 and ESR=65kΩ.

1.17 Controller Internal RCH Oscillator

Table 19. Controller Internal RCH Oscillator

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal high speed oscillating frequency	F_{MCLK}		4	4.0 8.0 16.0 22.12 24.0	32	MHz
Startup time (not including software calibration)	T_{Mstart}	F_{MCLK} = 4 MHz		6.0		us
		F_{MCLK} = 8 MHz		4.0		us
		F_{MCLK} = 16 MHz		3.0		us
		F_{MCLK} = 24 MHz		2.5		us
Current consumption	I_{MCLK}	F_{MCLK} = 4 MHz		80		uA
		F_{MCLK} = 8 MHz		100		uA
		F_{MCLK} = 16 MHz		120		uA
		F_{MCLK} = 24 MHz		140		uA
Clock duty cycle	DC_{MCLK}		45	50	55	%
Frequency tolerance	DEV_{MCLK}	V_{DD} = 1.8 ~ 3.6 V, TA = -40 ~ +85 ℃	-2.5		+2.5	%
		V_{DD} = 1.8 V ~ 3.6 V, TA = - 20 ~ + 50 ℃	-2.0		+ 2.0	%

1.18 Controller Internal RCL Oscillator

Table 20. Controller Internal RCL Oscillator

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal high speed oscillating frequency	F_{ACLK}			38.4		kHz
				32.768		
Startup time	T_{ACLK}			100		us
Current consumption	I_{ACLK}			0.25		uA
Clock duty cycle	DC_{ACLK}		25	50	75	%
Frequency tolerance	DEV_{ACLK}	V_{DD} = 1.8 ~ 3.6V, TA = - 40 ~ + 85 ℃	-2.0		+2.0	%
		V_{DD} = 1.8 ~ 3.6V, TA = - 20 ~ + 50 ℃	-1.5		+1.5	%

1.19 Controller Flash Features

Table 21. Controller Flash Features

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sector endurance	EC_{Flash}		20			kcycles
Byte Program Time	T_{Prog}		6		7.5	us
Sector erase time	T_{Erase}		4		5	ms
Chip erase time			30		40	ms
Data retention	RET_{Flash}	TA = +25 °C	20			Year
		TA = +85 °C	10			Year

1.20 Controller Low Power Mode Recover Time

Table 22. Controller Low Power Mode Recover Time

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Return to active mode from deep sleep mode	T_{Wakeup}	Regulated 1.5 V, TA = + 25°C, 4 MHz		4.0		us
		Regulated 1.5 V, TA = + 25°C, 8 MHz		3.1		us
		Regulated 1.5 V, TA = + 25°C, 16 MHz		2.8		us
		Regulated 1.5 V, TA = + 25°C, 24 MHz		2.7		us

1.21 Controller ADC Features

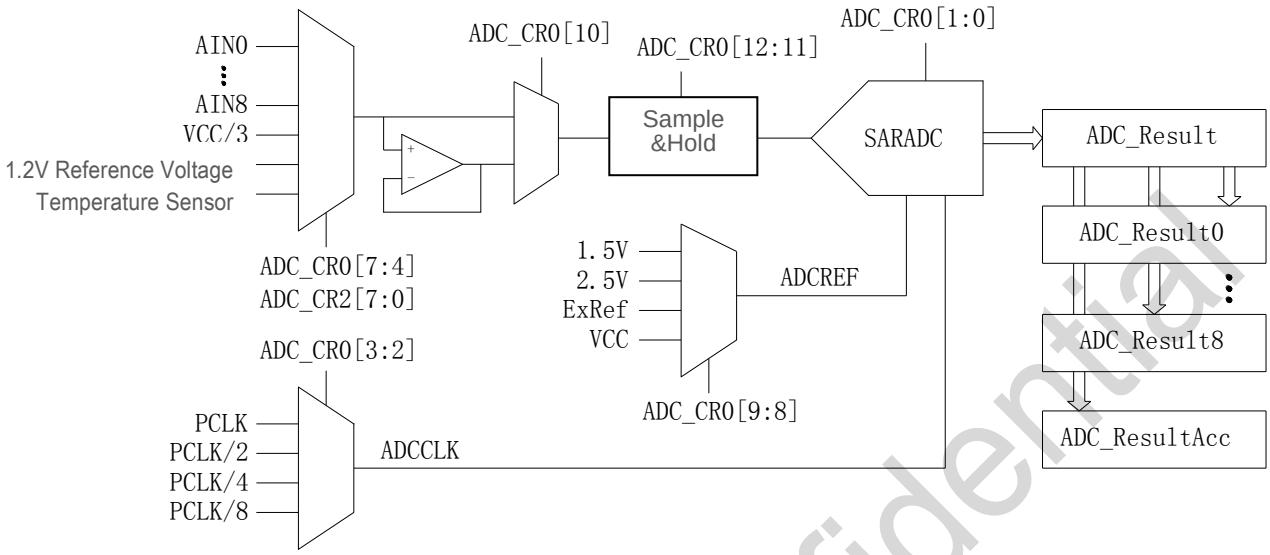


Figure 4. Controller ADC Features

Table 23. Controller ADC Features

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage range	V_{ADCin}	Single-ended	0		$V_{ADC\_REF\_IN}$	V
External input reference voltage	$V_{ADC\_REF\_IN}$		0		3.6	V
Internal 2.5V reference voltage	V_{REF_25}	TA = 25°C,V_{DD} = 3.3 V	2.475	2.5	2.525	V
Internal 1.5 V reference voltage	V_{REF_15}	TA = 25°C,V_{DD} = 3.3 V	1.485	1.5	1.515	V
Operating current (including reference source and buffer)	I_{ADC1}	200 ksps		2		mA
Operating current (not including reference source and buffer)	I_{ADC2}	1000 ksps		0.5		mA
Input capacitance	C_{ADC_IN}			16	19.2	pF
ADC clock	F_{ADC_CLK}				24	MHz
Startup time (ADC core and reference source)	T_{ADC_START}			30		us
Conversion time	T_{ADC_CONV}		20	24	28	Cycles
Valid bit	ENOB	1 Msps @ V_{DD} ≥ 2.7 V 500 ksps @ V_{DD} ≥ 2.4 V 200 ksps @ V_{DD} ≥ 1.8 V REF = EXREF(External Reference)		10.3		bit
		1 Msps @ V_{DD} ≥ 2.7 V 500 ksps @ V_{DD} ≥ 2.4 V		10.3		bit

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
		200 ksps @ V_{DD} ≥ 1.8 V REF = V_{DD}				
		200ksps @ VDD ≥ 1.8 V REF = Internal 1.5V		9.4		Bit
		200ksps @ V_{DD} ≥ 2.8 V REF = Internal 2.5 V		9.4		Bit
Signal to noise ratio	SNR	1 Msps @ V_{DD} ≥ 2.7 V 500 ksps @ V_{DD} ≥ 2.4 V 200 ksps @ V_{DD} ≥ 1.8 V REF = EXREF(External Reference)		68.2		dB
		1 Msps @ V_{DD} ≥ 2.7 V 500 ksps @ V_{DD} ≥ 2.4 V 200 ksps @ V_{DD} ≥ 1.8 V REF = V_{DD}		68.2		dB
		200 ksps @ V_{DD} ≥ 1.8 V REF = Internal 1.5V		60		dB
		200 ksps @ V_{DD} ≥ 2.8 V REF = Internal 2.5V		60		dB
Differential nonlinearity	DNL		-1		+1	LSB
Integral nonlinearity	INL		-3		+3	LSB
Drift error	E_{offset}			0		LSB
Gain error	E_{gain}			0		LSB
Missing code	MC		11.999	12		bit

1.22 Analog Voltage Comparator

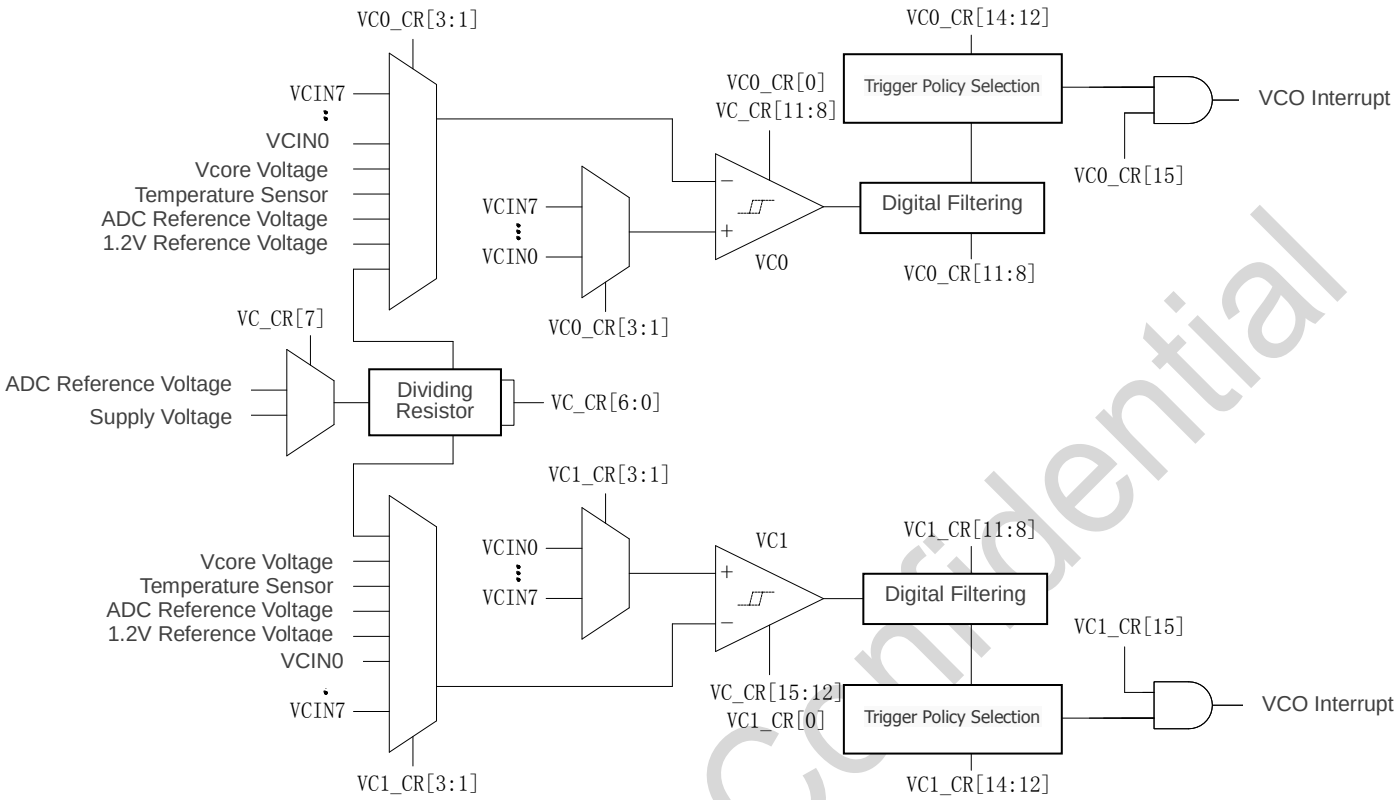


Figure 5. Analog Voltage Comparator

Table 24. Analog Voltage Comparator

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}	Single-ended	0		3.6	V
Common-mode input range	V_{IN_COM}		0		V_{DD} - 0.2	V
Input offset	V_{Offset}	TA = 25°C, V_{DD} = 3.3V	-10		+10	mV
Internal 1.2 V reference voltage	V_{1P2_AT}			1.2		V
Comparator current	I_{COMP}	VCx_BIAS_SEL = 00 VCx_BIAS_SEL = 01 VCx_BIAS_SEL = 10 VCx_BIAS_SEL = 11		0.16 1.28 10 20		uA
Comparator response time	$T_{RESPONSE}$	VCx_BIAS_SEL = 00 VCx_BIAS_SEL = 01 VCx_BIAS_SEL = 10 VCx_BIAS_SEL = 11		20 5 1 0.2		us
Comparator startup time (data signal does not change when it is enabled)	T_{Setup}	VCx_BIAS_SEL = 00 VCx_BIAS_SEL = 01 VCx_BIAS_SEL = 10 VCx_BIAS_SEL = 11		20 5 1 0.2		us

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
From main band gap being enabled to V1P2_AT being stable	$T_{Warmup1}$			20		us
From 2.5V being enabled & BGR being enabled to V2P5 being stable	$T_{Warmup2}$			15		us
V2P5 reference source current	I_{V2P5}			4		uA
Digital filtering time	T_{Filter}	VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111		25 50 100 400 1,600 6,000 25,000 100,000		us

1.23 Low Battery Detection Features

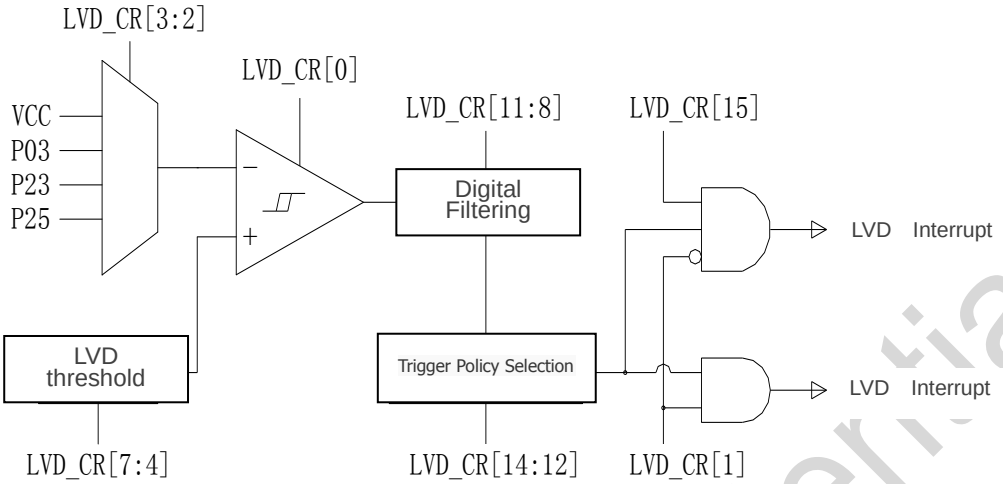
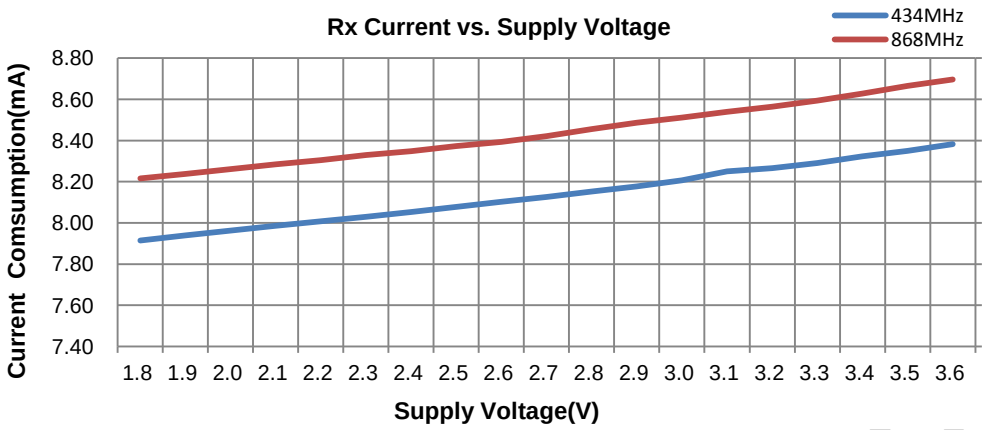


Figure 6. Low Battery Detection Features

Table 25. Low Battery Detection Features

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External input voltage range	V_{EX}	Single-ended	0		V_{DD}	V
V_{DD} or V_{EX} detection threshold	V_{LEVEL}	LVD_CR_VTDS = 0000		1.86		V
		LVD_CR_VTDS = 0001		1.96		
		LVD_CR_VTDS = 0010		2.07		
		LVD_CR_VTDS = 0011		2.17		
		LVD_CR_VTDS = 0100		2.27		
		LVD_CR_VTDS = 0101		2.38		
		LVD_CR_VTDS = 0110		2.48		
		LVD_CR_VTDS = 0111		2.58		
		LVD_CR_VTDS = 1000		2.69		
		LVD_CR_VTDS = 1001		2.79		
		LVD_CR_VTDS = 1010		2.89		
		LVD_CR_VTDS = 1011		3.00		
		LVD_CR_VTDS = 1100		3.10		
		LVD_CR_VTDS = 1101		3.20		
		LVD_CR_VTDS = 1110		3.31		
		LVD_CR_VTDS = 1111		3.41		
Low battery detection operating current	I_{LVD}			0.12		uA
Low battery detection response time (when V_{DD} or V_{EX} falls below or rises above the thresholds)	$T_{Response}$			80		us
Startup time (when it is enabled, V_{DD} or V_{EX} does not change)	T_{Setup}			5		us
Hysteresis voltage	V_{Hyste}			20		mV
Digital filtering time	T_{Filter}	LVD_debounce = 000		30		us
		LVD _debounce = 001		40		
		LVD _debounce = 010		50		
		LVD _debounce = 011		130		
		LVD _debounce = 100		480		
		LVD _debounce = 101		1,800		
		LVD _debounce = 110		7,300		
		LVD _debounce = 111		29,000		

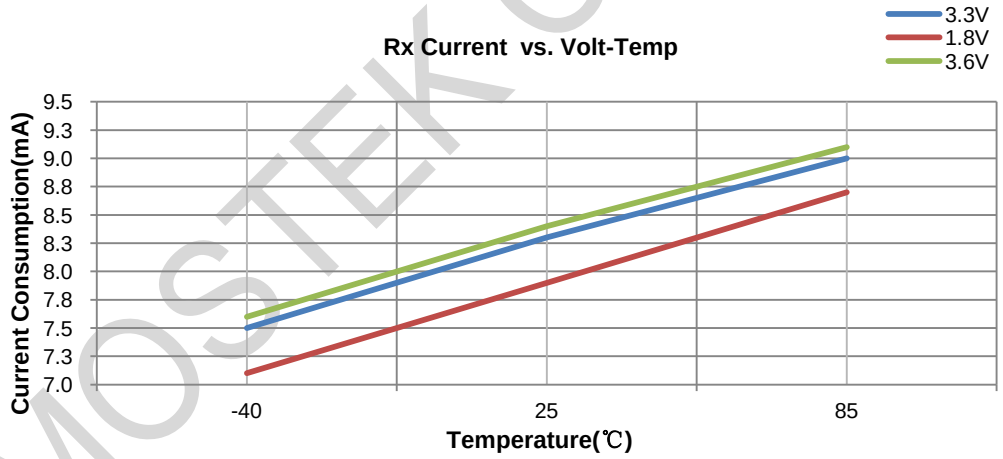
1.24 Receive Current and Supply Voltage Correlation



Test Conditions：Freq = 434 MHz & 868 MHz, F_{DEV} = 10 kHz, BR = 10 kbps

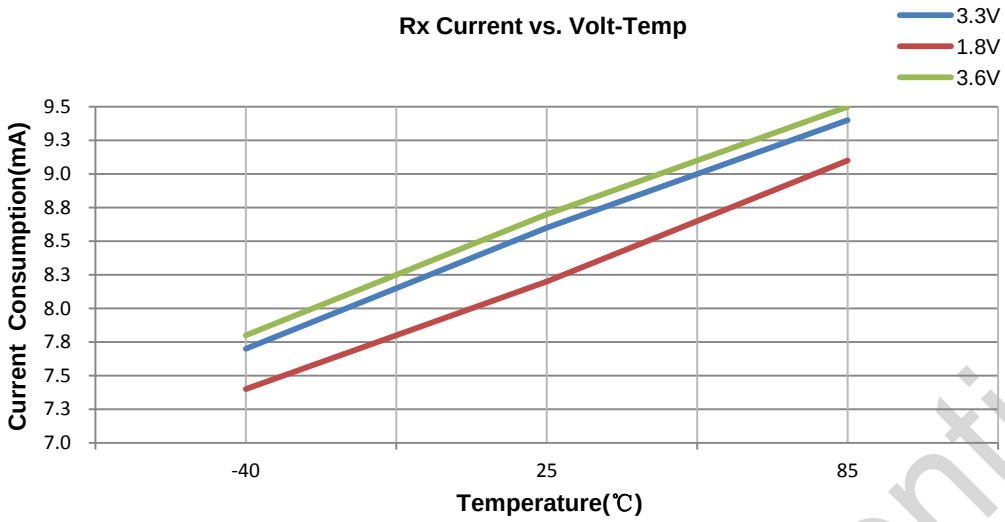
Figure 7. Rx Current vs. Supply Voltage

1.25 Correlation Among Receive Current, Supply Voltage and Temperature



Test Conditions：Freq = 434 MHz, F_{DEV} = 10 KHz, BR = 10 kbps

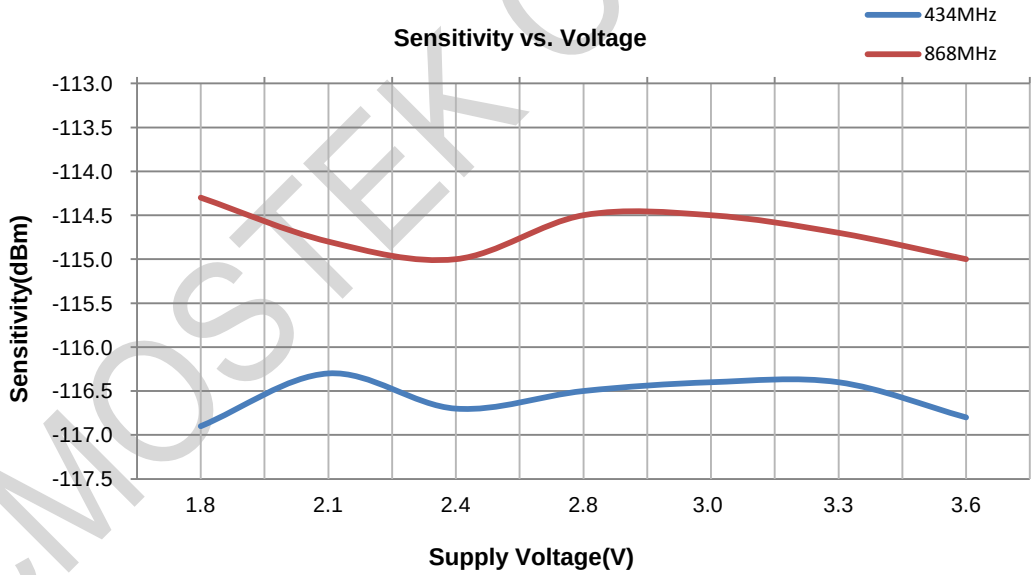
Figure 8. Rx Current vs. Volt-Temp



Test Conditions: Freq = 868 MHz, F_{DEV}= 10 kHz, BR = 10 kbps

Figure 9. Rx Current vs. Volt-Temp

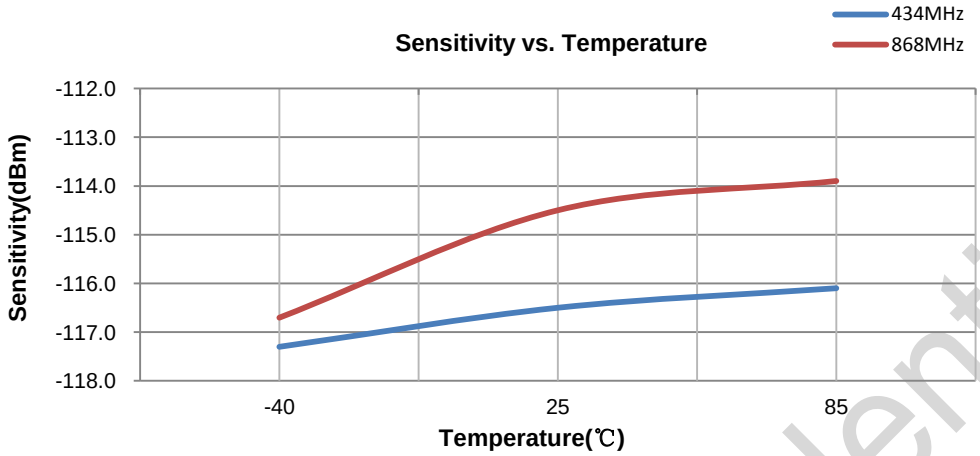
1.26 Receive Sensitivity and Supply Voltage Correlation



Test Conditions: FSK modulation, F_{DEV} = 10 kHz, BR = 10 kbps

Figure 10. Sensitivity vs. Voltage

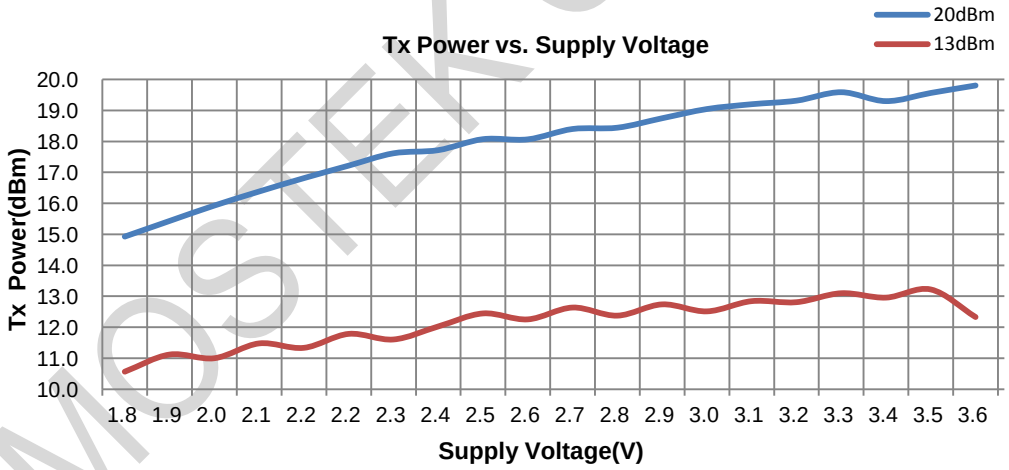
1.27 Receive Sensitivity and Temperature Correlation



Test Conditions：FSK modulation, F_{DEV} = 10 kHz, BR = 10 kbps

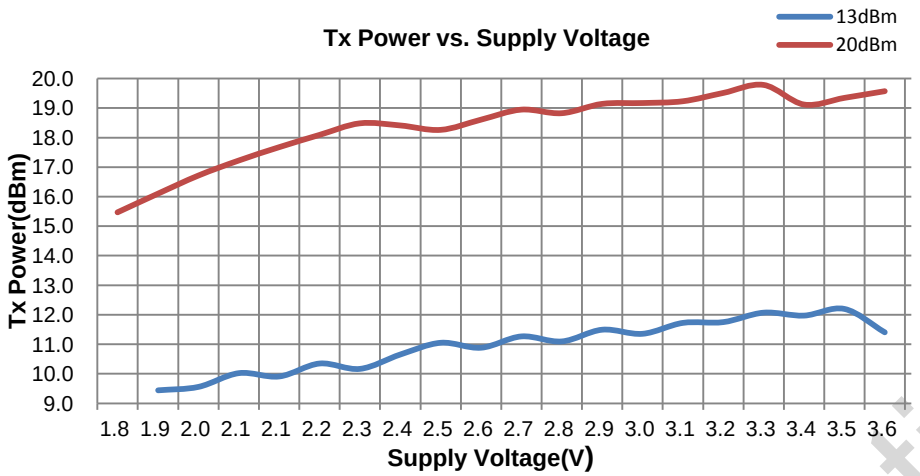
Figure 11. Sensitivity vs. Temperature

1.28 Transmit Power and Supply Voltage Correlation



Test Conditions：Freq = 434 MHz, 20 dBm & 13 dBm matching network respectively

Figure 12. Tx Power vs. Supply Voltage



Test Conditions：： Freq = 868MHz, 20dBm&13dBmmatching network respectively

Figure 13. Tx Power vs. Supply Voltage

1.29 Phase Noise

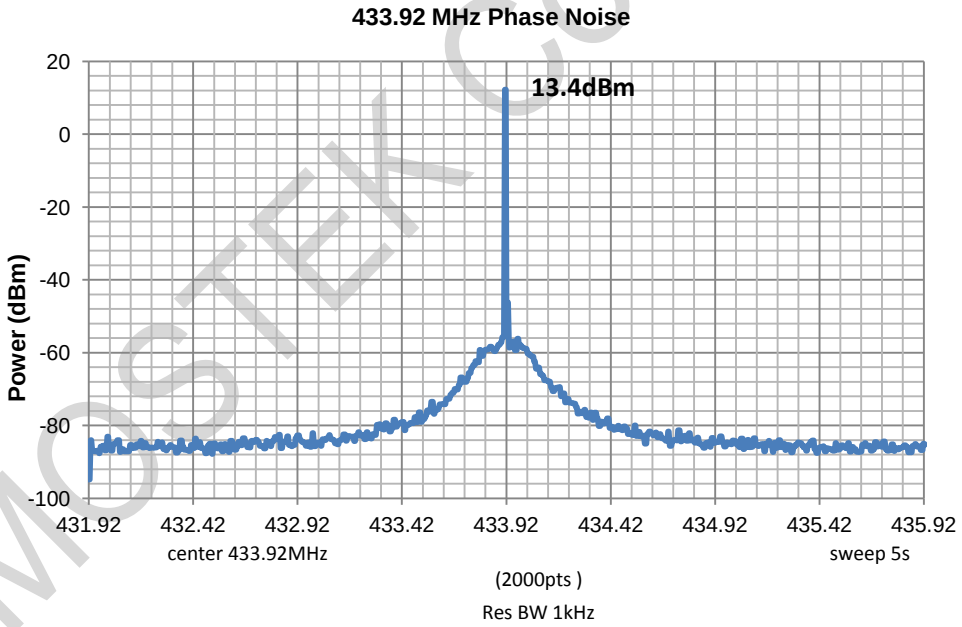


Figure 14. 433.92MHz Phase Noise

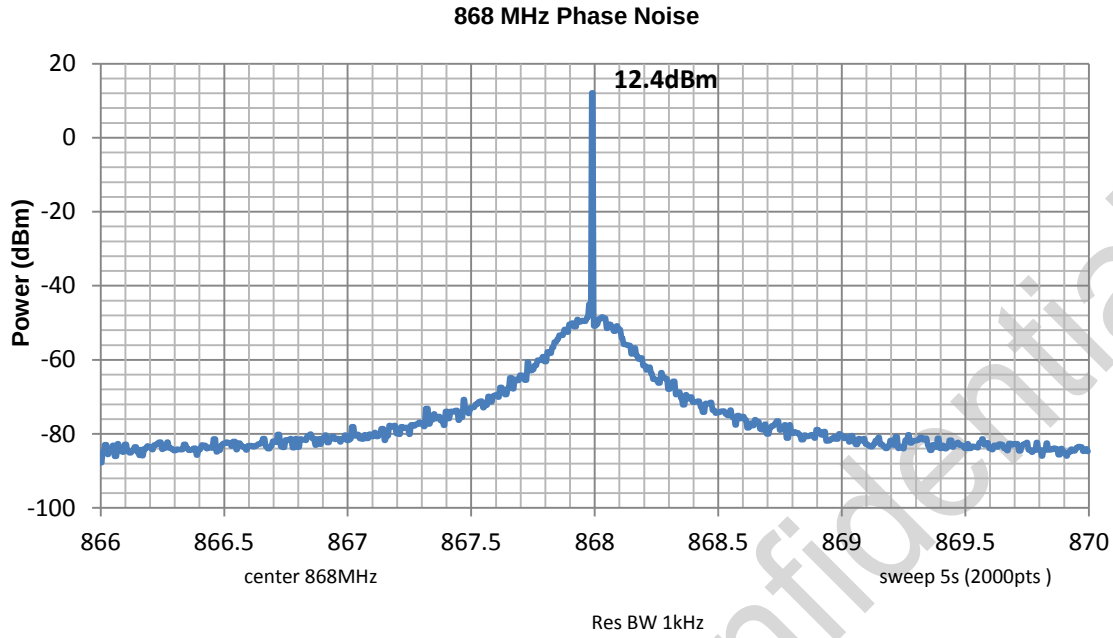


Figure 15. 868 MHz Phase Noise

2 Pin Description

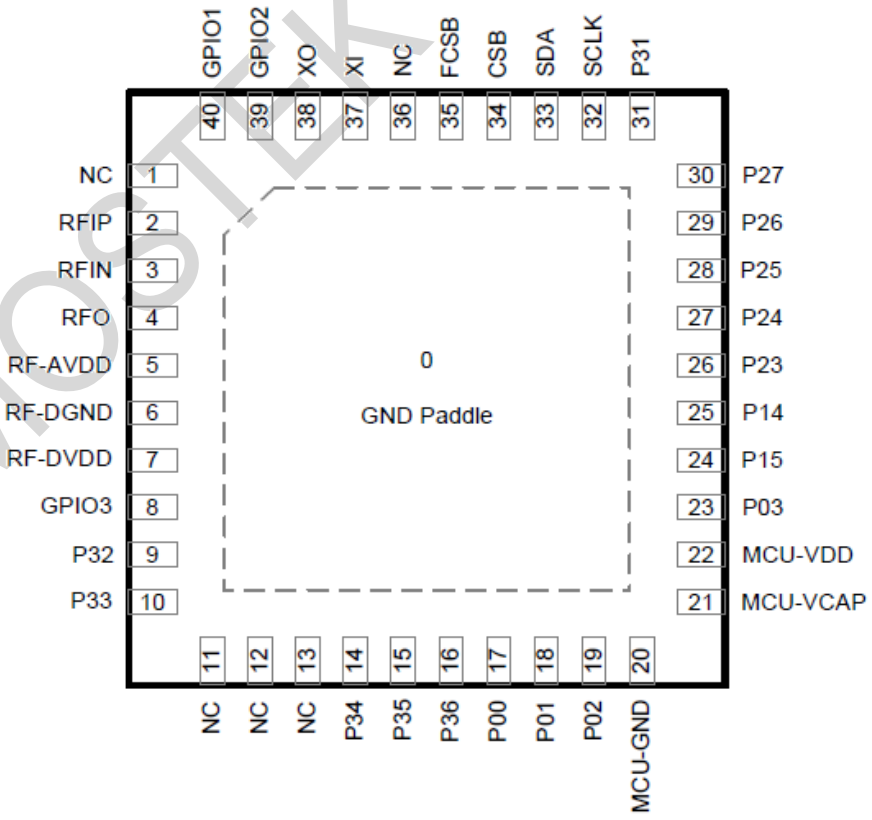


Figure 16. The CMT2380F32 Pin Arrangement Diagram

Table 26. The CMT2380F32 Pin Description

Pin #	Pin Name	I/O	Description
0	GND	I	Chip substrate, must connect to ground
1	NC	-	No connection
2 - 3	RFIP/RFIN	I	Differential RF signal input port
4	FRO	O	PA output
5	RF-AVDD	I	RF circuit VDD, requires to connect to a 1.8-3.6 V power supply
6	RF-DGND	I	GND, must connect to ground
7	RF-DVDD	I	Digital VDD, requires to connect to a 1.8-3.6 V power supply
8[1]	GPIO3	IO	Can be configured as: CLKO, DOUT/DIN, INT2 and DCLK (TX/RX)
9	P32	IO	General purpose digital input/output pin
	TIM3_TOGN	O	LPtimer inverted reversal output
	PCA_CH2	IO	PCA capture input/compare output 2
	TIM6_CHB	IO	Timer6 capture input/compare output B
	VC1OUT	O	VC1 output
	UART1_TXD	O	UART1 TXD
	PCA_CH4	IO	PCA capture input/compare output 4
	RTC_1HX	O	RTC1HZ output
	AIN2/VC2	I	Analog input
10	P33	IO	General purpose digital input/output pin
	UART2_RXD	I	UART2 RXD
	PCA_CH1	IO	PCA capture input / compare output 1
	TIM5_CHB	IO	Timer5 capture input / compare output B
	PCA_ECI	I	PCA external clock
	UART1_RXD	I	UART1 RXD
	XTL_OUT	O	32K Oscillating output
	TIM1_TOGN	O	Timer1 inverted reversal output
	AIN3/VC3	I	Analog input
11	NC	-	Not connect
12	NC	-	Not connect
13	NC	-	Not connect
14	P34	IO	General purpose digital input/output pin
	PCA_CH0	IO	PCA capture input / compare output 0
	UART2_TXD	O	UART2 TXD
	TIM5_CHA	IO	Timer5 capture input / compare output A
	TIM0_EXT	I	Timer0 external clock input
	TIM4_CHA	IO	Timer4 capture input / compare output A
	RTC_1HZ	O	RTC1HZ output
	TIM1_TOG	O	Timer1 inverted output
	AIN4/VC4	I	Analog input

Pin #	Pin Name	I/O	Description
15	P35	IO	General purpose digital input/output pin
	UART1_TXD	O	UART1 TXD
	TIM6_CHB	IO	Timer6 capture input / compare output B
	UART0_TXD	O	UART0 TXD
	TIM0_GATE	I	Timer0 gating
	TIM4_CHB	IO	Timer4 capture input / compare output B
	SPI_MISO	I	SPI Module master input slave output data signal
	I2C_SDA	IO	I2Cdata
	AIN5/VC5	I	Analog input
16	P36	IO	General purpose digital input/output pin
	UART1_RXD		UART1 RXD
	TIM6_CHA		Timer6 capture input / compare output A
	UART0_RXD		UART0 RXD
	PCA_CH4		PCA capture input / compare output 4
	TIM5_CHA		Timer5 capture input / compare output A
	SPI_MOSI		SPI module master output slave input data signal
	I2C_SCL	I	I2C Clock
	AIN6/VC6/AVREF	O	Analog input
17	P00	I	Digital input
	ResetB	I	Reset input port, active low, chip reset
18	P01	IO	General purpose digital input/output pin
	UART0_RXD	I	UART0 RXD
	I2C_SDA	IO	I2C data
	UART1_TXD	O	UART1 TXD
	TIM0_TOG	O	Timer0 inverted output
	TIM5_CHB	IO	Timer5 capture input / compare output B
	SPI_SCK	O	SPI clock
	TIM2_EXT	O	Timer2 external clock
	AIN7/VC7	I	Analog input
	XTHI	I	External XTH crystal oscillator clock input
19	P02	IO	General purpose digital input/output pin
	UART0_TXD	O	UART0 TXD
	I2C_SCL	O	I2C clock
	UART1_RXD	I	UART1 RXD
	TIM0_TOGN	O	Timer0 inverted reversal output
	TIM6_CHA	IO	Timer6 capture input / compare outputA
	SPI_CS	O	SPI CS
	TIM2_GATE	I	Timer2 gating
	AIN8	I	Analog Input
	XTHO	O	External XTH crystal oscillator clock output

Pin #	Pin Name	I/O	Description
20	MCU-GND	I	Digital Ground
21	MCU-VCAP	O	LDO core power supply output (internal circuit only, connect 4.7uF capacitor)
22	MCU-VDD	I	Digital Power Supply
23	P03	IO	General purpose digital input/output pin
	PCA_CH3	O	PCA capture input / compare output 3
	SPI_CS	O	SPI CS
	TIM6_CHB	IO	Timer6 capture input / compare output B
	LPTIM_EXT	I	LPTimer external clock input
	RTC_1HZ	O	RTC 1Hz output
	PCA_ECI	I	PCA external clock input
	VC0_OUT	O	VC0 output
	LVDIN1	I	Analog input
24	P15	IO	General purpose digital input/output pin
	I2C_SDA	IO	I2C data
	TIM2_TOG	O	Timer2 inverted output
	TIM4_CHB	IO	Timer4 capture input / compare output B
	LPTIM_GATE	I	LPTimer gating
	SPI_SCK	O	SPI clock
	UART0_RXD	I	UART0 RXD
	LVD_OUT	O	LVD output
	XTLO	O	External XTL crystal oscillator clock input
25	P14	IO	General purpose digital input/output pin
	I2C_SCL	O	I2C clock
	TIM2_TOGN	O	Timer2 inverted reversal output
	ECI	I	PCA external clock input
	ADC_RDY	O	ADC ready
	SPI_CS	O	SPI CS
	UART0_TXD	O	UART0 TXD
	XTLI	I	External XTL crystal oscillator clock input
26	P23	IO	General purpose digital input/output pin
	TIM6_CHA	IO	Timer6 capture input / compare output A
	TIM4_CHB	IO	Timer4 capture input / compare output B
	TIM4_CHA	IO	Timer4 capture input / compare output A
	PCA_CH0	IO	PCA capture input / compare output0
	SPI_MISO	IO	SPI Module master input slave output data signal
	UART1_TXD	O	UART1 TXD
	IR_OUT	O	38k carrier output
	LVDIN2/VC0	I	Analog input
27	P24	IO	General purpose digital input/output pin
	TIM4_CHB	IO	Timer4 capture input / compare output B

Pin #	Pin Name	I/O	Description
	TIM5_CHB	IO	Timer5 capture input / compare output B
	HCLK_OUT	O	HCLK output
	PCA_CH1	IO	PCA capture input / compare output 1
	SPI_MOSI	O	SPI module master output slave input data signal
	UART1_RXD	I	UART1 RXD
	VC1_OUT	O	VC1 output
	AIN0	I	Analog input
28	P25	IO	General purpose digital input/output pin
	SPI_SCK	O	SPI Clock
	PCA_CH0	IO	PCA capture input / compare output 0
	TIM5_CHA	IO	Timer5 capture input / compare output A
	LVD_OUT	O	LVD output
	UART2_RXD	I	UART2 RXD
	I2C_SDA	IO	I2C data
	TIM1_GATE	I	Timer1 gating
	LVDIN3/VC1	I	Analog input
29	P26	IO	P26 general purpose digital input/output pin
	SPI_MOSI	O	SPI Module master output slave input data signal
	TIM4_CHA	IO	Timer4 capture input / compare output A
	TIM5_CHB	IO	Timer5 capture input / compare output B
	PCA_CH2	IO	PCA capture input / compare output 2
	UART2_TXD	O	UART2 TXD
	I2C_SCL	O	I2C Clock
	TIM1_EXT	I	Timer1 external clock input
	AIN1	I	Analog input
30	P27	IO	General purpose digital input/output pin
	SPI_MISO	IO	SPI Module master input slave output data signal
	TIM5_CHA	IO	Timer5 capture input / compare output A
	TIM6_CHA	IO	Timer6 capture input / compare output A
	PCA_CH3	IO	PCA capture input / compare output 3
	UART0_RXD	I	UART0 RXD
	RCH_OUT	O	24 M oscillating output
	XTH_OUT	O	32 M oscillating output
	SWDIO	IO	Debugging interface, SWDIO
31	P31	IO	General purpose digital input/output pin
	TIM3_TOG	O	Timer 3 Inverted output
	PCA_ECI	I	PCA external clock
	PCLK_OUT	O	PCLK output
	VC0OUT	O	VC0 output
	UART0_TXD	O	UART0 TXD

Pin #	Pin Name	I/O	Description
	RCL_OUT	O	RCL oscillating output
	HCLK_OUT	O	HCLK output
	SWCLK	I	Debugging interface, SWCLK
32	SCLK	I	RF SPI clock
33	SDA	IO	RF SPI data input/output, connect to 10 kΩ pull-up resistor externally
34	CSB	I	RF SPI chip selection for register access
35	FCSB	I	RF SPI chip selection for FIFO access
36	NC	-	Not connect
37	XI	I	26 MHz crystal circuit input
38	XO	O	26 MHz crystal circuit output
39	GPIO2	IO	Can configure as: INT1,INT2,DOUT/DIN,DCLK (TX/RX),RF_SWT
40	GPIO1	IO	Can configure as: DOUT/DIN,INT1,INT2,DCLK (TX/RX),RF_SWT

Notes:

[1]. INT1 and INT2 refer to RF interrupts. DOUT refers to the demodulated data output. DIN refers to the modulation data input. DCLK refers to the modulation or demodulation data rate synchronous clock, which is switched automatically according to operation mode switch between TX and RX.

3 Chip Structure

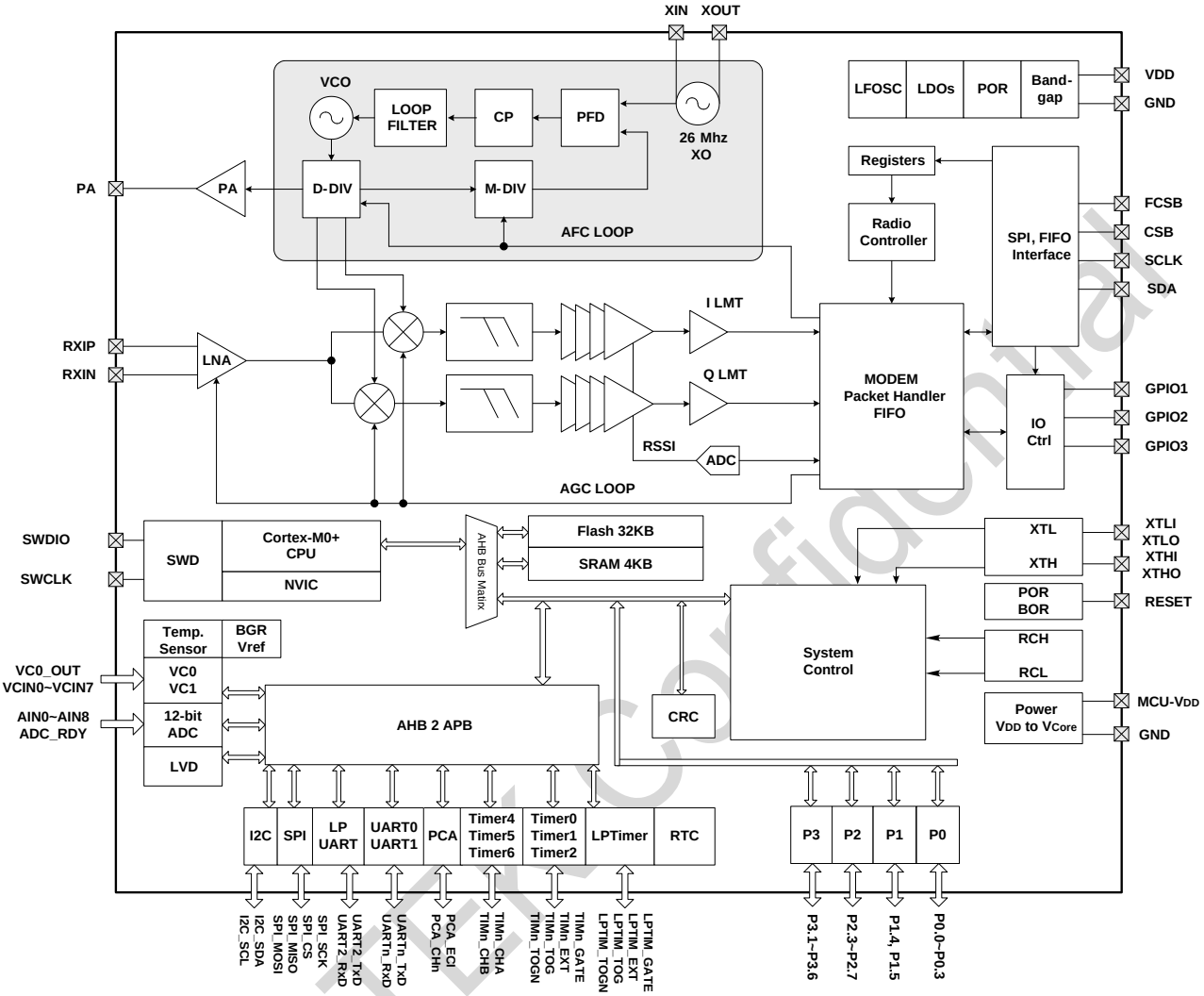


Figure 17. Functional System Block Diagram

The CMT2380F32 is a microcontroller integrated with high-performance sub-GHz wireless transceiver. The internal system block diagram of the CMT2380F32 is shown in Figure 17.

- **Low-power and High-performance Sub-GHz Transceiver**

With supports of 127 to 1020MHzfrequency range, modulation modes like OOK, (G)FSK, (G)MSK, etc., the sub-GHz wireless transceiver is remarkable for low-power and high performance features adapting to various wireless transceiver applications. The product is part of the CMOSTEK NextGenRF™ product family which covers a complete product line consisting of transmitters, receivers, transceiver, etc.

- **High Performance Cortex-M0+ Microprocessor**

Embedded with high-performance Cortex-M0+ core microprocessor, the CMT2380F32 suits for portable measurement systems requiring ultra-low power consumption. Powered by built-in 12-bit high-precision and high-speed SAR ADC (sampling rate up to 1Msps), comparator, rich peripherals like multi-channel UART, SPI andI2C, the CMT2380F32 is remarkable for such features as high integration, strong anti-interference and high reliability. See below table for its rich peripherals.

Table 27. The CMT2380F32 Peripheral Resource List

Name	Peripheral Resource
ROM	32 kbytes Flash
RAM	4 kbytes
Debug function	Serial bus debug interface
Unique identification code	Support
Multi-function serial interface	UART0/1 LPUART SPI I2C
ADC	12-bit1 Msps SAR
Analog voltage comparator	VC0/1
Real time clock	1
IO port	16+1
Port interrupt	16
Buzzer	4-ch
Flash security protection	Available
RAM parity	Available
Internal high speed oscillator	IRC 4 / 8 / 16 / 22.12 / 24 MHz
Internal low speed oscillator	IRC 38.4 / 32.768 kHz
External high speed crystal oscillator	4 / 8 / 16 / 32 MHz
Internal low speed crystal oscillator	32.768 kHz

4 Sub-GHz Transceiver

4.1 Transmitter

The CMT2380F32 transmitter is based on direct RF synthesizer. Its carrier frequency is generated by a low noise fractional frequency synthesizer. The modulated data is transmitted by an efficient single-ended power amplifier (PA). The output power can be read and written by registers, which is configurable ranging from -20dBm to +20dBm with 1dB step.

When the PA switches quickly, its changed input impedance instantaneously interferes with the output frequency of the VCO. This effect becomes a VCO pull that produces spectral spurs and glitches near the target carrier. By ramping the PA output power, it can minimize the instantaneous glitch of the PA. The CMT2380F32 has a built-in ramping mechanism. When the PA ramp is enabled, the PA output power can be ramped to the required value by the configured speed in order to reduce the undesired spectral spectrum. In FSK mode, the transmitter supporting signal is transmitted after Gaussian filtering, meaning GFSK, to make the transmitting spectrum more concentrated.

Users can design a PA matching network based on specific application requirements to optimize the transmission efficiency at the required output power. Typical application schematics and required BOMs are detailed above. For more application schematic details and layout guidelines, please refer to*AN141 CMT2300A Schematic and PCB Layout Guide*.

The transmitter can work in pass-through mode and packet mode respectively. In pass-through mode, data is sent to the chip directly through the DIN pin of the chip and transmitted directly. In packet mode, data is preloaded into the FIFO of the chip in STBY status and transmitted then along with other packet elements.

4.2 Receiver

An ultra-low power, high performance low IF OOK, FSK receiver is built in the CMT2380F32. It follows processing steps as: 1) The RF signal sensed by the antenna is amplified by the low noise amplifier. 2) The signal is down-converted to the intermediate frequency by the quadrature mixer and then filtered by the image rejection filter. 3) The signal is further amplified by the limiting amplifier. 4) The signal is sent to the digital domain for digital demodulation processing.

Each analog module is calibrated to an internal reference voltage during power-on reset (POR). This allows the chip to perform better at different temperatures and voltages. Baseband filtering and demodulation is done by a digital demodulator. When the chip is working in an environment with strong out-of-band interference, the automatic gain control loop adjusts the gain of the system through the wideband power detector and attenuation network next to the LNA to achieve optimal system linearity, selectivity, sensitivity, etc.

Following the low-power design techniques of CMOSTEK, an ultra-low power is consumed even when the receiver keeps operating for long period. Its periodic operating mode and air wakeup feature further reduce the average power consumption of the system, serving well in applications where power consumption is critical.

Similar to the transmitter, the CMT2380F32 receiver can operate in pass-through mode and packet mode respectively. In the pass-through mode, the data output by the demodulator can be directly output through the DOUT pin of the chip. DOUT can be configured from GPIO1/2/3. In the packet mode, data processing follows steps as: 1)The data output of the demodulator is firstly sent to the packet processor for decoding. 2)The data is filled into the FIFO. 3)The controller portion of the CMT2380F32 reads the FIFO through the SPI interface.

4.3 Transceiver Power-on Reset (POR)

The power-on reset circuit assists in power supply change detection and generates a corresponding reset signal to reset the entire RF system (the RF portion of the CMT2380F32). The CMT2380F32 controller can reinitialize the RF system after POR. The two cases for POR reset generation are as follows:

1. A rapid power supply mutation triggers POR reset under the condition that RF-VDD (RF system power supply, the

same below) drops 0.9V±20% (0.72V – 1.08V) within less than 2 us. Note that it monitors RF-VDD decrease instead of its absolute value as shown inthe below figure.

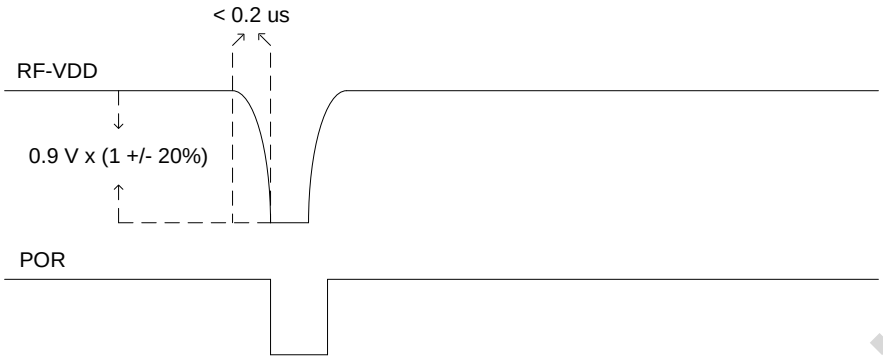


Figure 18. Rapid RF-VDD Drop Triggers POR Reset

2. A slow supply power drop triggers POR reset under the condition that RF-VDD drops to 1.45V±20% (1.16 – 1.74V) within less than 2 us. Note that it monitors the absolute value of RF-VDD instead of RF-VDD decrease as shown in the below figure.

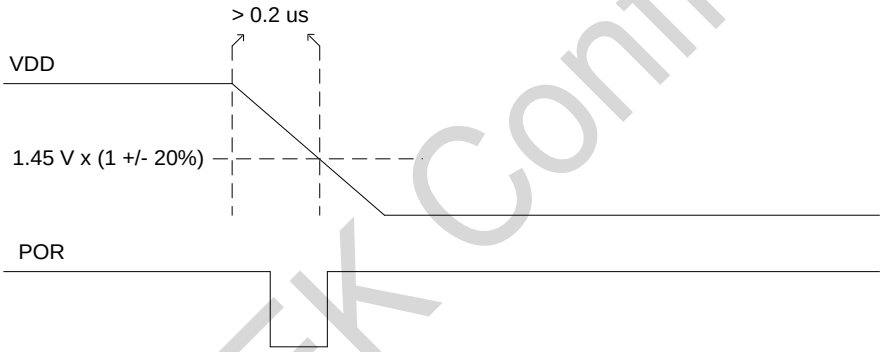


Figure 19. Slow RF-VDD Drop Triggers POR Reset

4.4 Transceiver Crystal Oscillator

The crystal oscillator provides both a reference clock for the phase-locked loop and a system clock for the digital part. The load capacitance depends on the crystal specified CL parameters. The total load capacitance between XI and XO should be equal to CL ensuring the crystal oscillates accurately at 26 MHz.

$$\mathbf{C_L = \frac{1}{1/C15 + 1/C16} + C_{par} + 2.5pF}$$

C15 and C16 are the load capacitances reside at both ends of the crystal. Cpar is the parasitic capacitance resides on the PCB. Each pin of the crystal has a 5pF parasitic capacitance inside, as an equivalence of 2.5pF altogether. The equivalent series resistance of the crystal should meet the specified specifications to ensure reliable crystal start-up. Alternatively the traditional crystal can be replaced with an external source connected to the XI pin. This clock signal is recommended to have a peak-to-peak level between 300 mV and 700 mV and be coupled to the XI pin with a coupling capacitor.

4.5 Transceiver Built-in Low Frequency Oscillator (LPOSC)

The CMT2380F32 RF system integrates a sleep timer driven by a 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer periodically wakes up the chip from sleep mode. Sleep time can be configured from 0.03125 ms to 41,922,560 ms when the chip is in periodical operating mode. Due to the low power oscillator frequency will change with the temperature and voltage drift, it will be automatically calibrated during power on and will be periodically calibrated since then. These calibrations will keep the oscillator's frequency tolerance within ± 1%.

4.6 Transceiver Built-in Low Battery Detection

The chip is employed with low battery detection function which is performed each time when the frequency is tuned. Frequency tuning occurs when the chip transitions from the SLEEP/STBY state to the RFS/TFS/TX/RX state. The detection result can be read by the LBD_VALUE register.

4.7 Receiver Signal Strength Indication (RSSI)

The RSSI is used to evaluate the strength of the signal within the tuned channel. The cascaded I/Q logarithmic amplifier amplifies the signal before it is sent to the demodulator. The receive signal indicators inside the logarithmic amplifiers ofI channel and Q channel produce DC voltage that is proportional to the input signal strength. The RSSI output is the sum of the two signal values, which extend a dynamic range of 80 dB based on the sensitivity. After the signal strength is sampled by the ADC, a smoother RSSI value is obtained through a SAR filter and a smoothing filter. The order of the smoothing filter can be set via RSSI_AVG_MODE<2:0>. After filtering, the code value is converted into a dBm value. Users can obtain either the RSSI code value (RSSI_CODE<7:0>) ordBm value (RSSI_DBM<7:0>) by reading the register. With configuring the value of RSSI_DET_SEL<1:0>, users can choose to either output the RSSI value in real time or store RSSI value at each stage during packet receiving.

The CMT2380F32 supports users to set RSSI_TRIG_TH<7:0> threshold. After a comparison between the threshold value and detected RSSI value, the comparison outputs logic *1* if the RSSI detection value is more than the threshold value, otherwise it outputs logic *0*. The comparison output can be output to the RSSI VLD interrupt or it can support the operation of the internal super-low power (SLP) mode.

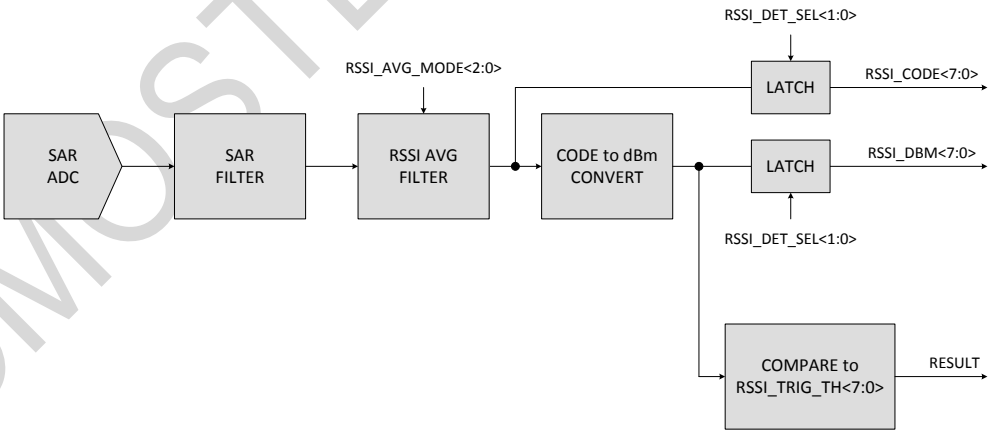


Figure 20. RSSI Measuring and Comparing Circuit Structure

The CMT2380F32 offers RSSI to meet the qualitative analysis requirements of users generally. However more accurate RSSI measurement results are needed in case of quantitative analysis, therefore users need to perform production calibration based on actual solutions. Please refer to *AN144- CMT2300A RSSI User Guide* for details.

4.8 Phase Jump Detector (PJD)

PJD refers to the phase jump detector. During the chip performing FSK demodulation, it can be used to identify useful signals from noise via observing the hopping characteristics of received signals.

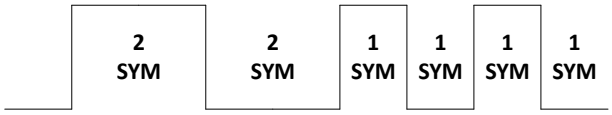


Figure 21.Receive Signal Jump Diagram

PJD identifies an input signal transition from *0* to *1* or from *1* to *0* as a phase jump. Users simply configure PJD_WIN_SEL<1:0> to indicate PJD how many signal transitions need to be detected before output the judgment result. As shown in above diagram, 6 phase jumps occurred among the total of 8 symbols received, meaning the jump number is not equal to the number of symbols. The jump count is equivalent to the number of symbols only if preamble is received. In general, the more signal transition detected, the more reliable the judgment is. The less, the faster the detection completes. If the receiving time window is small, the number of detections needs to be reduced to meet the window setting requirements. In general, 4 signal transitions detection can ensure reliable detection, that is, neither misjudging noise as a useful signal nor the detection failure of a useful signal will happen.

Monitoring signal transitions is essentially monitoring whether the signal meets the expected data rate, meanwhile, the PJD also automatically monitors whether the error of the signal meets the agreed value of the valid signal and determines if the SNR exceeds 7 dB. It outputs *1* if it determines a reliable signal is received based on the combined data rate, error and SNR monitoring results, otherwise it outputs *0* if it determines the signal is noise or interference signal. This result can be output to the RSSI VLD interrupt or to the implementation instance of the internal assisting super-low power (SLP) receive mode. In the direct mode, the FSK demodulation output can also be muted through setting the DOUT_MUTE register bit to *1*based on phase jump detect result.

PJD is similar to traditional carrier sense(CS) technique, more reliable though. A combine of RSSI monitoring and PJD technique ensures accurate channel state identification.

4.9 Receiver Clock Data Recovery (CDR)

CDR system is largely to recover the clock signal synchronized with the data rate while receiving data, either for decoding inside the chip or outputting to the GPIO for users to sample data. Error existing between the recovered clock frequency and the actual transmitted data rate will cause data acquisition errors, error codes and decoding errors during data reception. Therefore, CDR takes a simple but critical role.

The CMT2380F32 receiver supports three CDR systems according to different application requirements:

- **COUNTING system**

  This system is designed for the case where the data rate is relatively accurate. If the data rate is 100% aligned, users can even receive unlimited lengths of *0* without error.

- **TRACING system**

  This system is designed for dealing with large data rate errors. It has a tracking function that automatically detects the data rate transmitted by TX and adjusts the RX local data rate promptly to minimize the error between them. This system leads the industry by supporting up to 15.6% error.

- **MANCHESTER system**

  This system comes from COUNTING system by inheriting its basic features except a difference on specific design for

Manchester codec, which performs special treatment in case of a sudden change in the TX data rate to identify the signal part with sudden changes.

4.10 Fast Manual Frequency Hopping

Manual frequency hopping refers to switching an original basic frequency point obtained by RRPDK configuration, e.g. 433.92MHz,to another frequency point by simply setting 1 or 2 registers on MCU during the application, which simplify user's operation much for switching frequency points frequently in multi-channel applications.

$$\mathbf{FREQ} = \mathbf{Basic\ Frequency\ Point} + \mathbf{2.5\ kHz} \times \mathbf{FH\_OFFSET} < 7:0 > \times \mathbf{FH\_CHANNEL} < 7:0 >$$

General processing steps follow: 1) Set FH_OFFSET<7:0> during the initialization configuration of power-up. 2) Switch channels constantly as desired in the application by changing FH_CHANNEL<7:0>.

When fast manual frequency hopping in the receiving mode is performed, it needs to have special process on AFC parameters. Please refer to *AN197-CMT2300A-CMT2119B-CMT2219B Fast Manual Frequency Hopping* and *CMT2300*as well as *CMT2219B Frequency Hopping Calculation Table* for more details.

4.11 Transceiver Control Interface and Operating Mode

4.11.1 Transceiver SPI Interface Timing

The RF system of CMT2380F32 communicates with the controller section via a 4-wire SPI port (FCSB, CSB, SDA and SCLK). The low active CSB is the chip selection signal used to access the registers. The low active FCSB is the chip selection signal used to access the FIFO. The above two cannot be set to low both at the same time. SCLK is a serial clock with speed up to 5MHz.Data is sent on the falling edge of SCLK and collected on the rising edge for the chip itself or an external MCU. SDA is a bidirectional pin for inputting and outputting data. Both the address and data parts are transmitted from the MSB.

The CSB is pulled low when registers are accessed. An R/W bit followed by a 7-bit register address is sent. After the controller pulls CSB low, it must wait for at least half a SCLK cycle before it can start transmitting R/W bits. After the controller sends the falling edge of the last SCLK, it must wait for at least half of the SCLK cycle before pulling CSB high.

It should be noted that, as for read register operations, both the controller and the transceiver may generate a switch IO (SDA) port event among address 0 and data 7. At this point, SDA will switch the IO port from input to output, and the controller will switch the corresponding IO port from output to input. In the below figure, please notice the position of the dotted line in the middle, at this time, it is strongly recommended the controller switches the IO port to input before it sends the falling edge of SCLK. The transceiver will switch the IO to output after it receives the falling edge, which avoids situations where the both set SDA to output resulting in electrical conflicts.

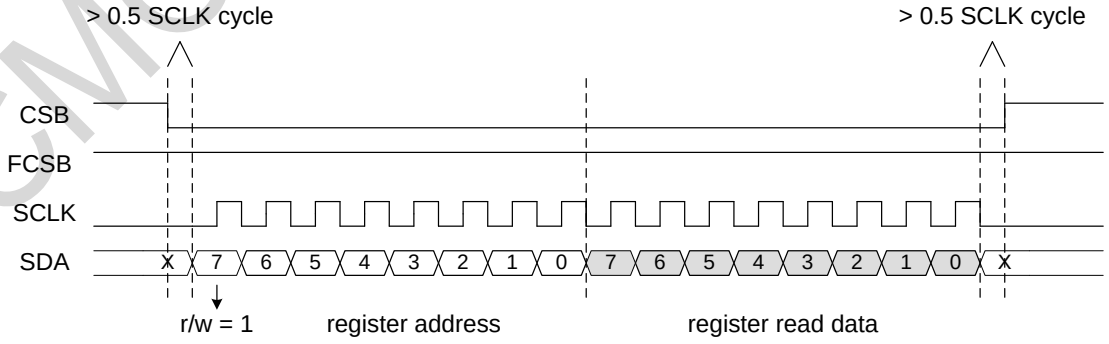


Figure 22. Transceiver SPI Read Register Timing

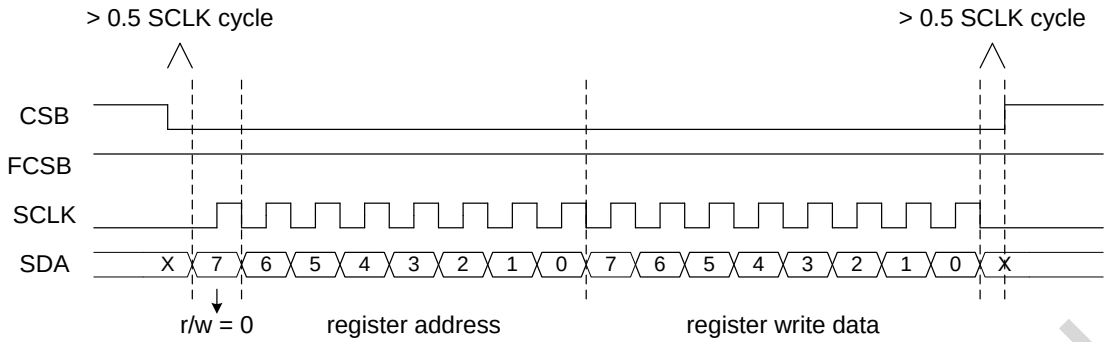


Figure 23. Transceiver SPI Write Register Timing

4.11.2 Transceiver FIFO Interface Timing

By default, the transceiver provides two independent 32-byte FIFOs for RX and TX. The RX FIFO is used to store received data in RX mode, and the TX FIFO is to store data to be transmitted in TX mode. Users can set FIFO_MARGE_EN to *1* as well, thus the two FIFOs are combined into a 64-byte FIFO, available both in TX and RX. By configuring FIFO_RX_TX_SEL, it indicates whether TX or RX currently is used. In no-combine case, when 32-byte RX FIFO is filled in, to save system operation time, users can fill in the 32-byte TX FIFO simultaneously for the next transmission.

The FIFO can be accessed via the SPI interface. Users can clear the FIFO by setting the FIFO_CLR_TX/FIFO_CLR_RX bit and transmit repeated data filled previously by setting FIFO_RESTORE, which avoids data refilling.

When accessing the FIFO, users start from configuring a number of registers involving FIFO read/write mode and some operating modes settings, as well as some other working modes. Please see *AN143-CMT2300A FIFO and Packet Format Usage Guide* for more details. As shown in below timing diagram for reading and writing, it should be noted that the FCSB control and CSB control for register access are slightly different. At the beginning of the access, the FCSB pulls down one clock cycle before sending the rising edge of SCLK. After sending the falling edge of the last SCLK, it pulls up FCSB at least 2us later. The FCSB must keep pulled up for at least 4us between two consecutive read and write operations. When writing to the FIFO, the first bit of the data must be ready a half of clock cycle before the first rising edge of SCLK is sent.

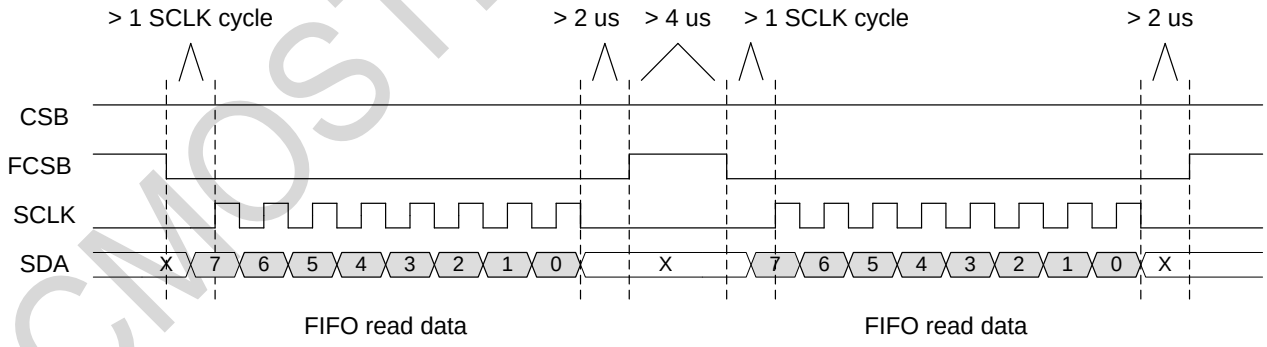


Figure 24. SPI Read FIFO Timing

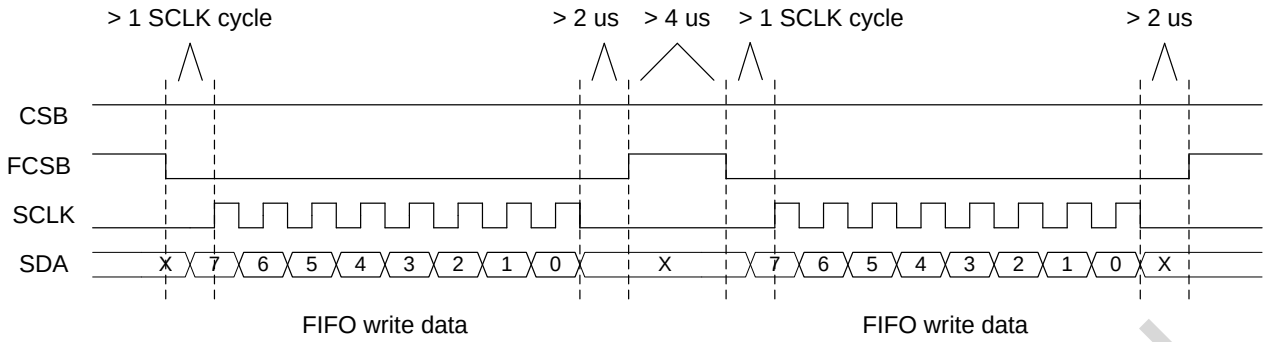


Figure 25. SPI Write FIFO Timing

The transceiver provides enriched FIFO-related interrupt sources helping for efficient operation of the chip. The Rx and Tx-related FIFO interrupt timing is shown in the figure below.

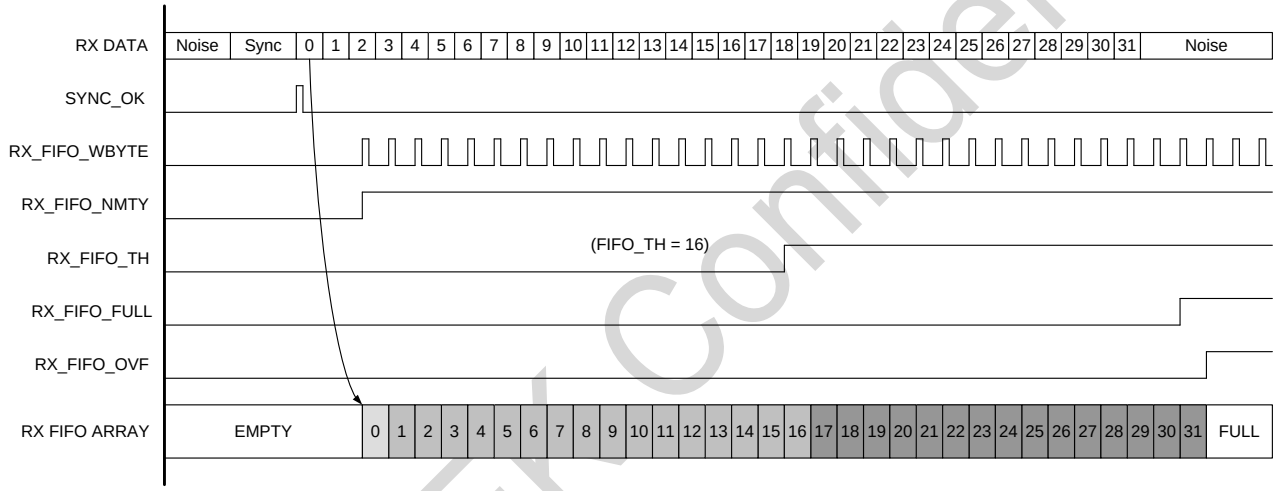


Figure 26 Transceiver RX FIFO Interrupt Timing Schematic

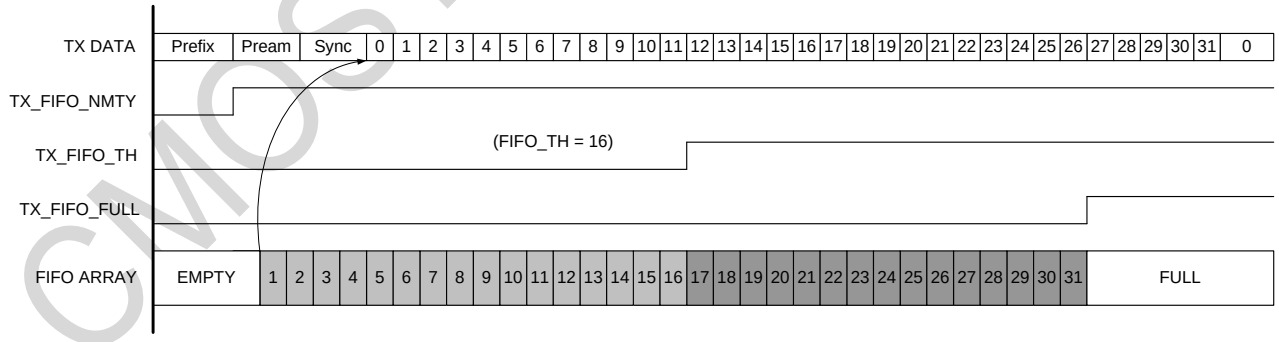


Figure 27. Transceiver TX FIFO Interrupt Timing Schematic

4.11.3 Transceiver Operating Status, Timing, and Power Consumption

- **Startup Timing**

After the transceiver is powered up on RF-VDD, generally it takes about 1 ms for POR release. The crystal starts after POR release. The startup time defaults to N ms depending on characteristics of the crystal itself. After startup, it needs to wait for a

period of time for crystal stabilization then to start working. The default stabilization time is set as 2.48ms by default. The time can be written later by writing XTAL_STB_TIME <2:0>. The chip stays in the IDLE state until the crystal is stable. After the crystal is stabilized, the chip will leave IDLE and begin calibration for each module. After calibration, the chip will stay at SLEEP, waiting for the user to do initialization configuration. The chip returns to IDLE and resume the power-on process any time when reset is performed.

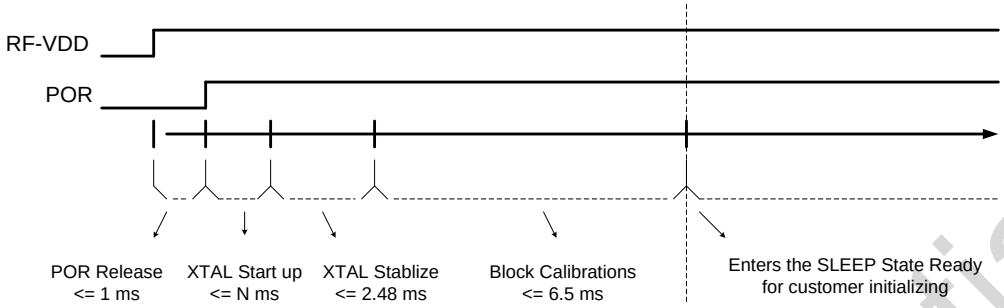


Figure 28. Startup Timing Diagram

The chip enters SLEEP mode after calibration completion. By now, the controller can switch the chip to different operating states by setting the register CHIP_MODE_SWT<7:0>.

- **Transceiver Operating Status**

The transceiver has a total of 7 working status: IDLE, SLEEP, STBY, RFS, RX, TFS and TX, as listed in the below table.

Table 28. Transceiver Status and Module Startup Table

Status	Binary Code	Switch Command	Startup Module	Optional Startup Module
IDLE	0000	soft_rst	SPI, POR	NA
SLEEP	0001	go_sleep	SPI, POR, FIFO	LFOSC, sleep timer
STBY	0010	go_stby	SPI, POR, XTAL, FIFO	CLKO
RFS	0011	go_rfs	SPI, POR, XTAL, PLL, FIFO	CLKO
TFS	0100	go_tfs	SPI, POR, XTAL, PLL, FIFO	CLKO
RX	0101	go_rx	SPI, POR, XTAL, PLL, LNA+MIXER+IF, FIFO	CLKO, RX timer
TX	0110	go_tx	SPI, POR, XTAL, PLL, PA, FIFO	CLKO

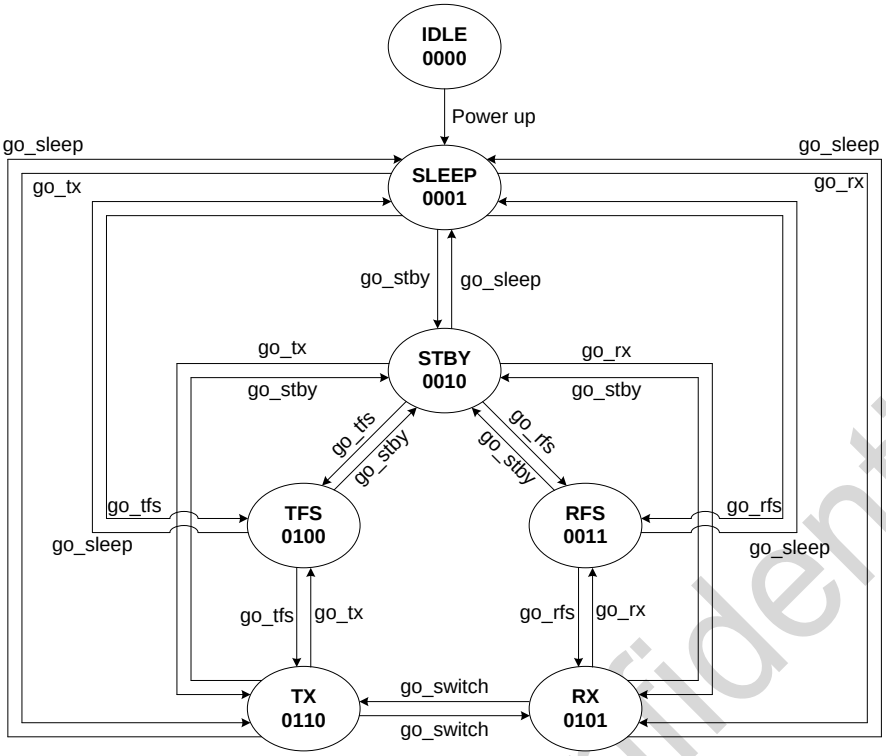


Figure 29. Status Switch Diagram

- **SLEEP Status**

The power consumption of the chip keeps the lowest in SLEEP mode with almost all modules disabled. The SPI is enabled, the registers in the configuration area and control area 1 can be accessed, and the contents previously filled in the FIFO is retained but the FIFO cannot be operated. If the periodical wake-up function is enabled, the LFOSC and sleep counters will start to work. The time period required for switching from IDLE to SLEEP is the power up processing time specified in above. Switching from the rest of the status to SLEEP is done immediately.

- **STBY Status**

In STBY, the crystal is enabled and the LDO of the digital circuit is enabled as well. The current is slightly increased. The FIFO can be operated. Users can choose whether to output CLKO (system clock) to the GPIOn pin. As the crystal is enabled, the time required switching from STBY to transmit or receive is less than that in SLEEP status (switching from SLEEP to STBY requires more time to wait for the crystal startup and stabilizing for a while). Switching from other status to STBY will complete immediately.

- **RFS Status**

RFS is transitional status before switching to RX. Except the receiver's RF module, all others are enabled and the current will be larger than that in STBY. As the PLL is already locked to the RX frequency point in RFS status, it cannot be switched to TX. Switching from STBY to RFS requires approximately 350us for PLL calibration and settling. Switching from SLEEP to RFS requires more time to wait for the crystal startup and stabilizing for a while. Switching from other status to RFS is done immediately.

- **TFS Status**

TFS is transitional status before switching to TX. Except the transmitter's RF module, all other modules are enabled and the current will be larger than STBY. As the PLL is already locked to the frequency of the TX in TFS status, it cannot be switched to

RX. Switching from STBY to TFS requires approximately 350us for PLL calibration and settling. Switching from SLEEP to TFS requires more time to wait for the crystal startup and stabilizing for a while. Switching from other states to TFS is done immediately.

- **RX Status**

All RX related modules on the receiver will be turned on. Switching from RFS to RX takes only 20us. Switching from STBY to RX requires a 350us for PLL calibration and settling. Switching from SLEEP to RX requires more time to wait for the crystal startup and stabilizing for a while. In TX, users can switch to RX in a prompt way by sending the go_switch command. No matter whether the frequency points set by TX and RX are the same, it needs to wait for 350us for PLL recalibration and settling to accomplish switch.

- **TX Status**

All transmitter related modules will be turned on at TX. Switching from TFS to TX takes only 20us. Switching from STBY to TX requires 350us for PLL calibration and settling. Switching from SLEEP to TX requires more time to wait for the crystal startup and stabilizing for a while. In RX, users can switch to TX in a prompt way by sending the go_switch command. No matter whether the frequency points set by TX and RX are the same, it needs to wait for 350us for PLL recalibration and settling to complete switch.

4.11.4 Transceiver GPIO Function and Interrupt Mapping

The three GPIOs employed in the transceiver are GPIO1, GPIO2, and GPIO3. Each GPIO can be configured with different input or output functions. The transceiver is employed with two interrupt ports, which can be configured to different GPIOs for mapping output.

Table 29. Transceiver GOIP Function

Pin#	Name	I/O	Function
48	GPIO1	IO	Can configure as: DOUT/DIN,INT1,INT2,DCLK (TX/RX),RF_SWT
47	GPIO2	IO	Can configure as:INT1,INT2,DOUT/DIN,DCLK (TX/RX),RF_SWT
9	GPIO3	IO	Can configure as: CLKO,DOUT/DIN,INT2,DCLK (TX/RX)

The interrupt mapping table is given below. Mapping for INT1 and INT2 is the same. Take INT1 as an example as follows.

Table 30. Transceiver Interrupt Mapping

Name	INT1_SEL	Description	Clear Method
RX_ACTIVE	00000	Indicates that the interrupt is ready to enter RX or has entered RX, which is *1* in the PLL calibration and RX status, otherwise *0*.	Auto
TX_ACTIVE	00001	Indicates that the interrupt is ready to enter TX or has entered TX, which is *1* in the PLL calibration and RX status, otherwise *0*.	Auto
RSSI_VLD	00010	An interrupt Indicating whether the RSSI is valid	Auto
PREAM_OK	00011	An interrupt Indicating whether Preamble is received successfully.	by MCU
SYNC_OK	00100	An interrupt Indicating whether Sync Word is received successfully.	by MCU
NODE_OK	00101	An interrupt Indicating whether Node ID is received successfully.	by MCU
CRC_OK	00110	An interrupt Indicating whether receive and pass CRC check successfully	by MCU
PKT_OK	00111	An interrupt indicating receive a packet completely	by MCU
SL_TMO	01000	An interrupt indicating SLEEP counter time out	by MCU
RX_TMO	01001	An interrupt indicating RX counter time out	by MCU

Name	INT1_SEL	Description	Clear Method
TX_DONE	01010	An interrupt indicating TX completion	by MCU
RX_FIFO_NMTY	01011	An interrupt indicating RX counter is not empty	Auto
RX_FIFO_TH	01100	An interrupt indicating unread contents in RX FIFO exceed FIFO TH	Auto
RX_FIFO_FULL	01101	An interrupt indicating RX FIFO is full	Auto
RX_FIFO_WBYTE	01110	An interrupt indicating a BYTE is written in RX FIFO, which is a pulse	Auto
RX_FIFO_OVF	01111	An interrupt indicating RX FIFO overflow	Auto
TX_FIFO_NMTY	10000	An interrupt indicating TX FIFO is not empty	Auto
TX_FIFO_TH	10001	An interrupt indicating unread contents in TX FIFO exceed FIFO TH	Auto
TX_FIFO_FULL	10010	An interrupt indicating TX FIFO is full	Auto
STATE_IS_STBY	10011	An interrupt indicating current status is STBY	Auto
STATE_IS_FS	10100	An interrupt indicating current status is RFS or TFS	Auto
STATE_IS_RX	10101	An interrupt indicating current status is RX	Auto
STATE_IS_TX	10110	An interrupt indicating current status TX	Auto
LBD	10111	An interrupt indicating that low battery detection is active (VDD is lower than the set TH)	Auto
TRX_ACTIVE	11000	An interrupt indicating begin to enter RX or TX, already in RX or TX, which is *1* in PLL calibration, RX status or TX state, otherwise *0*.	Auto
PKT_DONE	11001	Indicating that the current data packet has been received with 4 cases as below: 1. Receive the entire packet completely 2. Manchester decoding error, decoding circuit automatically restarts 3. NODE ID receives error, the decoding circuit automatically restarts 4. The signal conflict is found, the decoding circuit does not restart automatically, waiting for the MCU to process	by MCU

The interrupt is valid for value *1* by default. However value *0* becomes valid for all interrupts by setting the INT_POLAR register bit to *1*. Still take INT1 as an example as shown in the below figure with the control and selection diagram of all interrupt sources shown. INT1 and INT2 are the same in control and mapping.

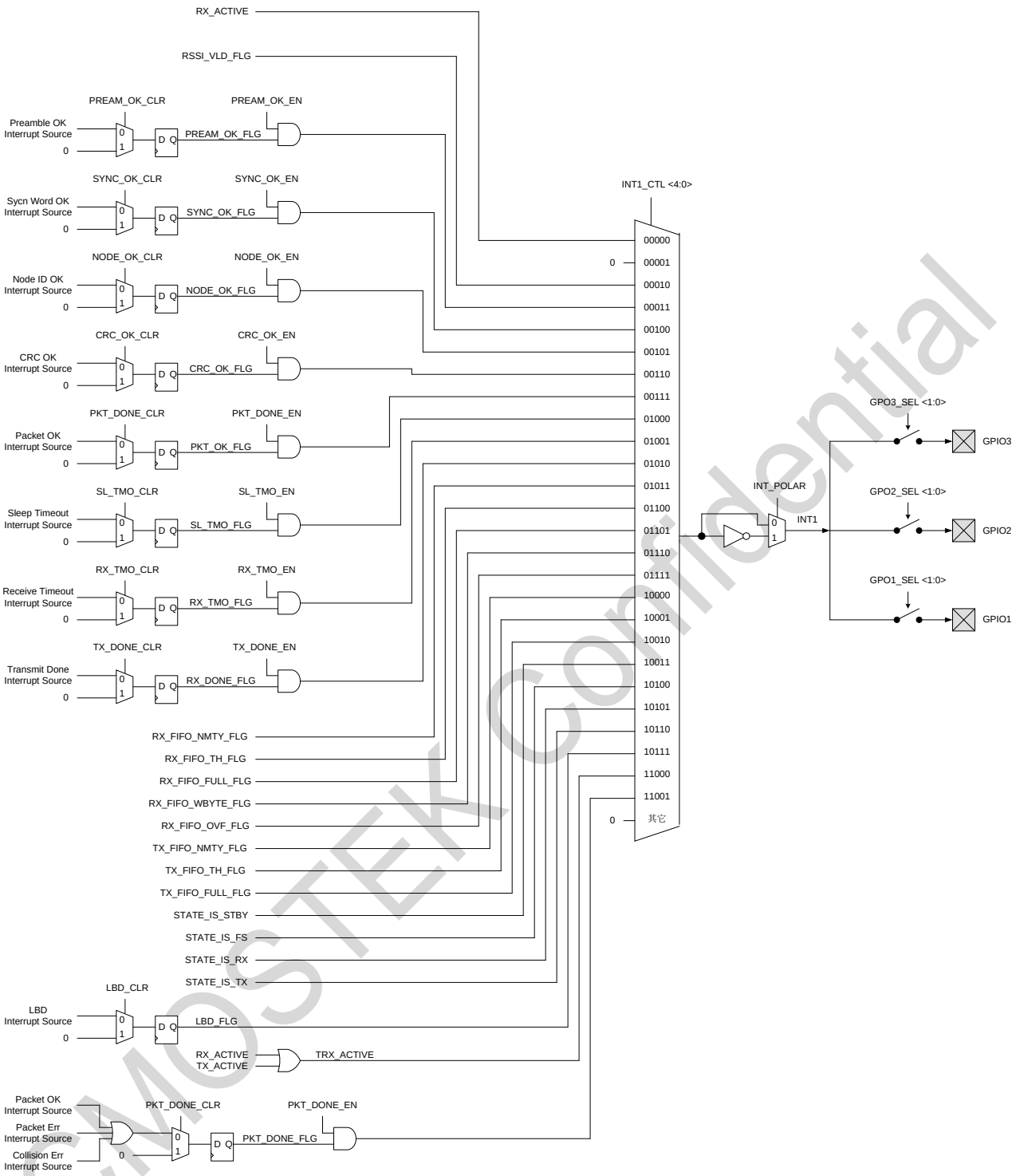


Figure 30. The CMT2300A INT1 Interrupt Map

5 Controller function Introduction

5.1 Cortex M0+ Core Function Description

The ARM® Cortex®-M0+ processor is based on the Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, it is powered with a number of new designs, improved debugging and tracking capabilities, reducing the number of instruction cycles (IPC), improved two-stage pipeline for Flash access, etc. The Cortex-M0+

processor fully supports the integrated Keil & IAR debugger.

The Cortex-M0+ includes a hardware debug circuit that supports the 2-pin SWD debug interface.

Table 31. ARM Cortex-M0+ Features

CPU instruction set	Thumb/Thumb-2
Assembly line	2-stage pipeline
Performance efficiency	2.46CoreMark/ MHz
Performance efficiency	0.95 DMIPS/MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single cycle 32-bit multipliers
Debugging	Serial-wire debug port with 4 hard break points and 2 watch points

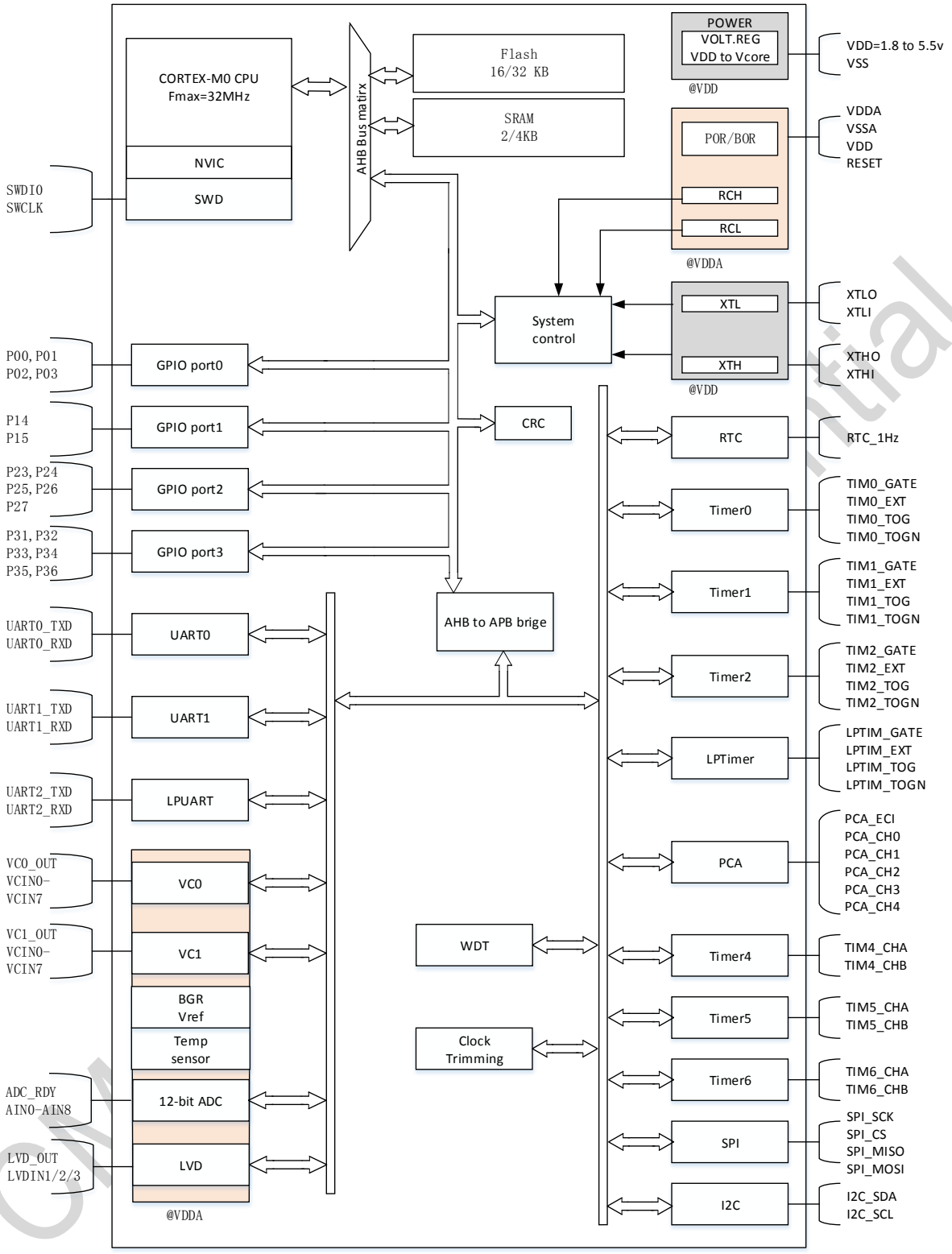


Figure 31. Controller Functional Block Diagram

5.2 Memory

5.2.1 On-chip Program Memory Flash

It's powered by fully built-in 32kbytesflash controller remarkable for no external high voltage input required, programming with high voltage generated by fully built-in circuits and support of ISP, IAP, ICP functions.

5.2.2 On-chip Data Memory Flash

4 kbytes RAM data is retained in various ultra-low power modes desired by customer. With hardware parity bit, if the data is accidentally destroyed, the hardware circuit will generate an interrupt immediately when the data is read, which helps ensure system reliability.

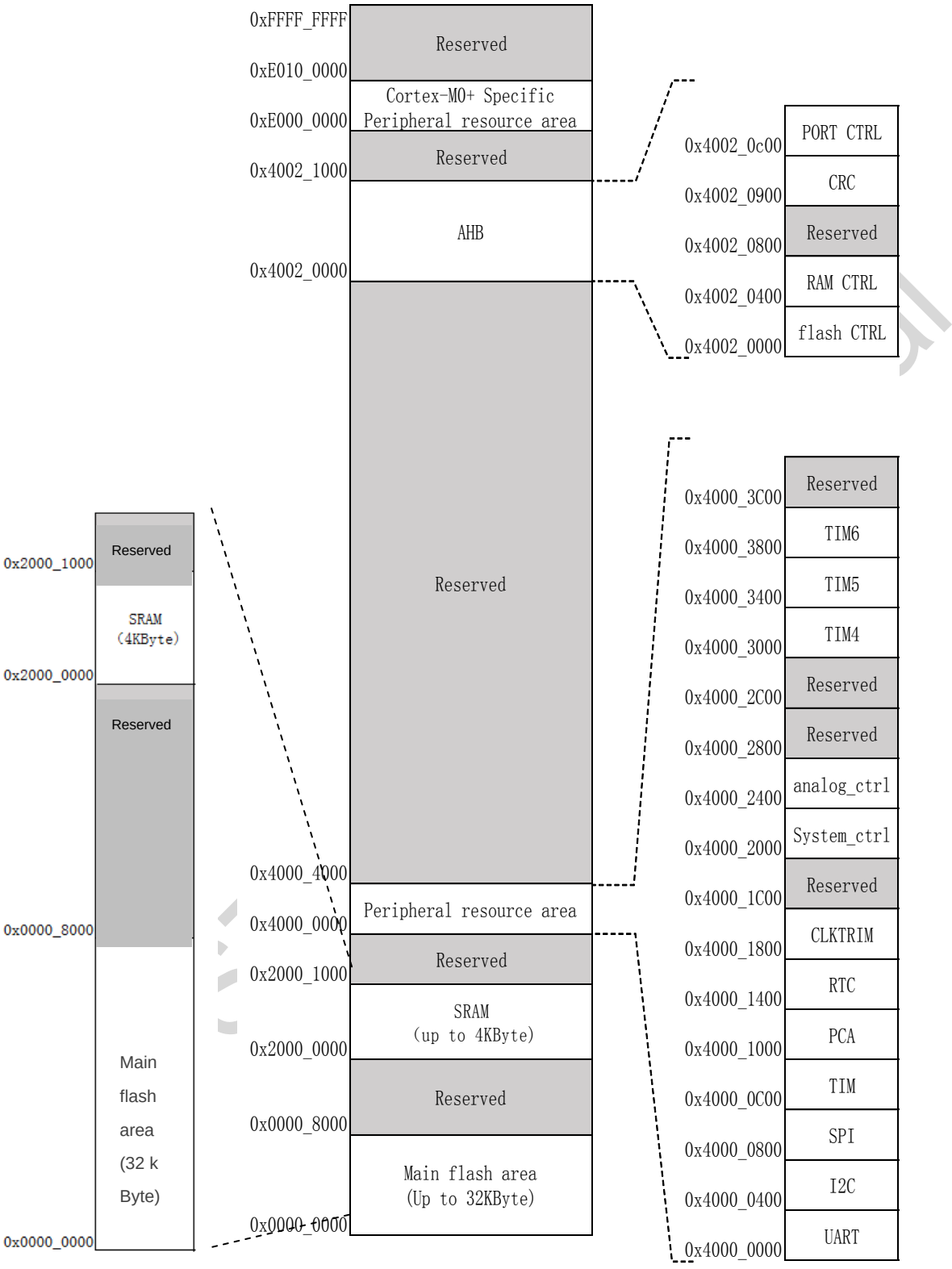


Figure 32. Memory Section Mapping

5.3 System Clock

- 1 high-precision internal clock RCH with a configurable frequency of 4~24MHz. The wake-up time from low-power mode to operating mode is 3 us at 16MHz configuration. Frequency tolerance over full temperature and voltage range is less than ±2.5%. No external expensive high-frequency crystal is required.
- 1 external crystal oscillator XTH with a frequency range of 4~32MHz.
- 1 external crystal oscillator XTL with a frequency of 32.768 kHz.
- 1 internal clock RCL with frequencies of 32.768/38.4 kHz.

5.4 Operating Mode

- **Active mode**

  Both CPU and the peripheral function modules are running.

- **Sleep mode**

  CPU stops running and the peripheral function modules are running.

- **Deep sleep mode**

  CPU stops running, the high-speed clock stops running, and the low-power function module is running.

5.5 RTC Hardware Real Time Clock RTC

RTC (real time counter) is a register supporting BCD data, which uses a 32,768 Hz crystal oscillator as its clock to implement the perpetual calendar function. It supports interrupt period setting as year/month/day/hour/minute/second, 24/12 hour mode, automatic leap year calibration by hardware, precision compensation and the highest precision reaching 0.96ppm. The internal temperature sensor or external temperature sensor can be used for accuracy compensation. It supports adjusting the year/month/day/hour/minute/second by +1/-1 operation via software with a minimum adjustable precision of 1 second.

When the MCU is reset caused by external factors, the RTC calendar recorder which indicates the time and date, does not clear the reserved value, which makes it the best choice for measuring instrumentation with the requirement of permanent high-precision and real-time clock.

5.6 General Purpose IO Port

Up to 16 GPIO ports are available with some of them multiplexed with analog ports. Each port is controlled by an independent control register bit. It supports both edge-triggered interrupts and level-triggered interrupts, which wake up the MCU to operating mode from various ultra-low power modes. It supports both Push-Pull CMOS output and Open-Drain output. Built-in pull-up resistor, pull-down resistor and the function of Schmitt trigger input filtering are available. The output drive capability is configurable with up to 12mA of current drive capability. 16 general purpose IOs support external asynchronous interrupts.

5.7 Interrupt Controller

The Cortex-M0+ processor provides a built-in Nested Vectored Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs. It supports4 interrupt priorities to handle complex logic and enables real-time control and interrupt handling.

The 32 interrupt entry vector addresses are listed in the below table.

Table 32. Interrupt Vector Address Table

Interrupt Vector Number	Interrupt Source
0	GPIO_P0
1	GPIO_P1
2	GPIO_P2
3	GPIO_P3
4	-
5	-
6	UART0
7	UART1
8	UART2
9	-
10	SPI
11	-
12	I^2C
13	-
14	Timer 0
15	Timer 1
16	Timer 2
17	LPTimer
18	Timer 4
19	Timer 5
20	Timer 6
21	PCA
22	WDT
23	RTC
24	ADC
25	-
26	VC0
27	VC1
28	LVD
29	-
30	RAM Flash fault
31	Clock trim

5.8 Reset Controller

This product has 7 reset signal sources. Each reset signal allows CPU resume to run, with most of the registers being reset and the program counter PC being reset and pointing to 00000000.

Table 33. Reset Source Table

No.	Reset Source
0	Power-on and power-off reset POR BOR
1	External Reset Pin reset
2	WDT reset
3	PCA reset
4	Cortex-M0+ LOCKUP hardware reset
5	Cortex-M0+ SYSRESETREQ software reset
6	LVD reset

5.9 Timer/Counter

Table 34. Timer Functionalities Table

Function Category	Timer	Bit Width	Pre-divided Frequency	Counting Direction	PWM	Capture	Complementary Output
Base timer	Timer 0	16/32	1/2/4/8/16 32/64/256	Up-count	NA	NA	NA
	Timer 1	16/32	1/2/4/8/16/ 32/64/256	Up-count	NA	NA	NA
	Timer 2	16/32	1/2/4/8/16/ 32/64/256	Up-count	NA	NA	NA
LPTimer	LPTimer	16	NA	Up-count	NA	NA	NA
PCA	PCA	16	2/4/8/16/32	Up-count	5	5	NA
Advanced timer	Timer 4	16	1/2/4/8/16/ 64/256/1024	Up-count / down-count/ up-down-count	2	2	1
	Timer 5	16	1/2/4/8/16/ 64/256/1024	Up-count/ down-count/ up-down-count	2	2	1
	Timer 6	16	1/2/4/8/16/ 64/256/1024	Up-count/ down-count/ up-down-count	2	2	1

The Base Timer contains three timers, Timer 0/1/2, with the same functionality. Timer 0/1/2 is a synchronous timer/counter that can either be used as a 16-bit timer/counter with auto-reload function or as a 32-bit timer/counter with no auto-reload function. Timer 0/1/2 can count external pulses or perform system timing.

The LPTimer is an asynchronous 16-bit timer/counter that can still perform clock/count by internal low speed RC or external low speed crystal oscillator even the system clock is turned off. It provides the function to wake up the system in low power mode by interrupt as well.

The PCA (programmable counter array) supports up to 5 16-bit capture/compare modules. The timer/counter can be used as the capture/compare function for general-purpose clock counter/event counter. Each module of the PCA can be independently programmed to provide input capture, output compare or pulse width modulation. In addition, module 4 supports an additional watchdog timer mode.

The Advanced Timer consists of three timers, Timer 4/5/6, with the same functionalities, which are high-performance counters used to count different clock waveforms. Each timer can generate a pair of PWMs that complement each other or 2 separate PWM outputs that captures external inputs for pulse width or period measuring.

The basic functions and features of the advanced timer are shown in the below table.

Table 35. Advanced Timer Function Table

Waveform mode	Sawtooth wave, triangle wave
Basic function	Incrementing and decrementing counting directions
	Software synchronization
	Hardware synchronization
	Cache function
	Orthogonal coding count
	General purpose PWM output
	Protection mechanism
	AOS associated action
Interrupt type	Count comparison match interrupt
	Count cycle match interrupt
	Dead time error interrupt
	Short circuit monitoring interrupt

5.10 Watchdog WDT

WDT (watch dog timer) is a configurable 20-bit timer that provides a reset in case of an MCU exception. A built-in 10k low-speed clock input is used as the counter clock. Users can choose to pause or keep it run in debug mode. WDT can be reset by writing a specific sequence.

5.11 Universal Purpose Asynchronous Receiver UART0, UART1 and LPUART

- 2 universal asynchronous receiver/transmitters
- One low power universal asynchronous receiver/transmitter available in low-power mode

5.12 Synchronous Serial Interface SPI

One serial peripheral interface, supporting master-slave mode.

5.13 I2C Bus

One I2C (inter-integrated circuit), supporting master-slave mode. With serial synchronous clock, data can be transmitted between devices at different rates. The serial 8-bit bidirectional data transmission can reach a maximum speed of 1Mbps.

5.14 Buzzer

3 base timers along with 1 LPTimer co-function to output buzzer providing programmable drive frequency for the buzzer. The buzzer port provides 16mA sink current, complementary output without additional transistors required.

5.15 Clock Calibration Circuit

The built-in clock calibration circuit can be used to calibrate the internal RC clock with an external precision crystal oscillator. The internal RC clock can also be used to verify whether the external crystal clock is working properly.

5.16 Unique ID number

Each chip has a unique 16-byte device identification number consisting of wafer lot information, chip coordinate information, etc. The ID address is 0X0010_0E70-0X0010_0E7F.

5.17 CRC16 Hardware Cyclic Redundancy Check Code

It conforms to the polynomial given in ISO/IEC13239 :F(x) = X16 + X12 + X5 + 1.

5.18 12-bit SARADC

The 12-bit successive approximation analog-to-digital converter, which is monotonous without loss of code, has a sampling rate of 1 Msps when operating with a 24M ADC clock. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from an external input or supply voltage. The 12 input channels includes 9 external pin inputs, 1 internal temperature sensor voltage, one 1/3 supply voltage and 1 built-in BGR 1.2V voltage. A configurable input signal amplifier is built in to detect weak signals.

5.19 Voltage Comparator (VC)

It's Chip pin voltage monitoring/comparison circuit. It provides 8 configurable positive/negative external input channels, 5 internal input channels including 1 internal temperature sensor voltage, 1 built-in BGR 2.5V reference voltage, 1 built-in BGR 1.2 V voltage and one 64-step resistor Partial pressure. The VC output can be used by Timer0/1/2, LPTimer, Advanced Timer, PCA capture with programmable count array, gating, and external count clocks. An asynchronous interrupt can be generated based on the rising/falling edge to wake up the MCU from low power mode. It supports configurable software anti-shake function as well.

5.20 LVD Low Voltage Detector (LVD)

It detects the chip supply voltage or chip pin voltage with sixteen levels of voltage monitoring values (1.8 ~ 3.3 V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. It provides hardware hysteresis circuit and

configurable software anti-shake function.

5.21 Embedded Debug System

The embedded debugging solution provides a full-featured real-time debugger co-working with sophisticated debugging software such as Keil and IAR. It supports for 4 hard breakpoints and multiple soft breakpoints.

5.22 High Security

It's powered with encrypted embedded debugging solution providing full-featured real-time debugger.
Please refer to AN220 *CMT2380F32 User's Manual (Microcontroller Section)* for detailed instructions on using the CMT2380F32 microcontroller.

6 Order Information

Table 36. The CMT2380F32 Order Information

Model	Description	Packaging	Packaging Option	Operating Condition	Minimum Order Quantity
CMT2380F32-EQR[1]	The CMT2380F32 ultra-low power sub-1GHz wireless MCU	QFN40(5x5)	Tape and tray	1.8 to 3.6 V, - 40 to 85 °C	3,000

Notes:

[1]. E refers to extended Industrial product rating, which supports temperature range from -40 to +85 °C. Q refers to the package type QFN40.

R refers to tape and tray type, and the minimum order quantity (MOQ) is 3,000 pieces.

Please visit www.cmostek.com for more product/product line information.

Please contact sales@cmostek.comor your local sales representative for sales or pricing requirements.

7 Packaging Information

The packaging information of the CMT2380F32 is shown in the below figure.

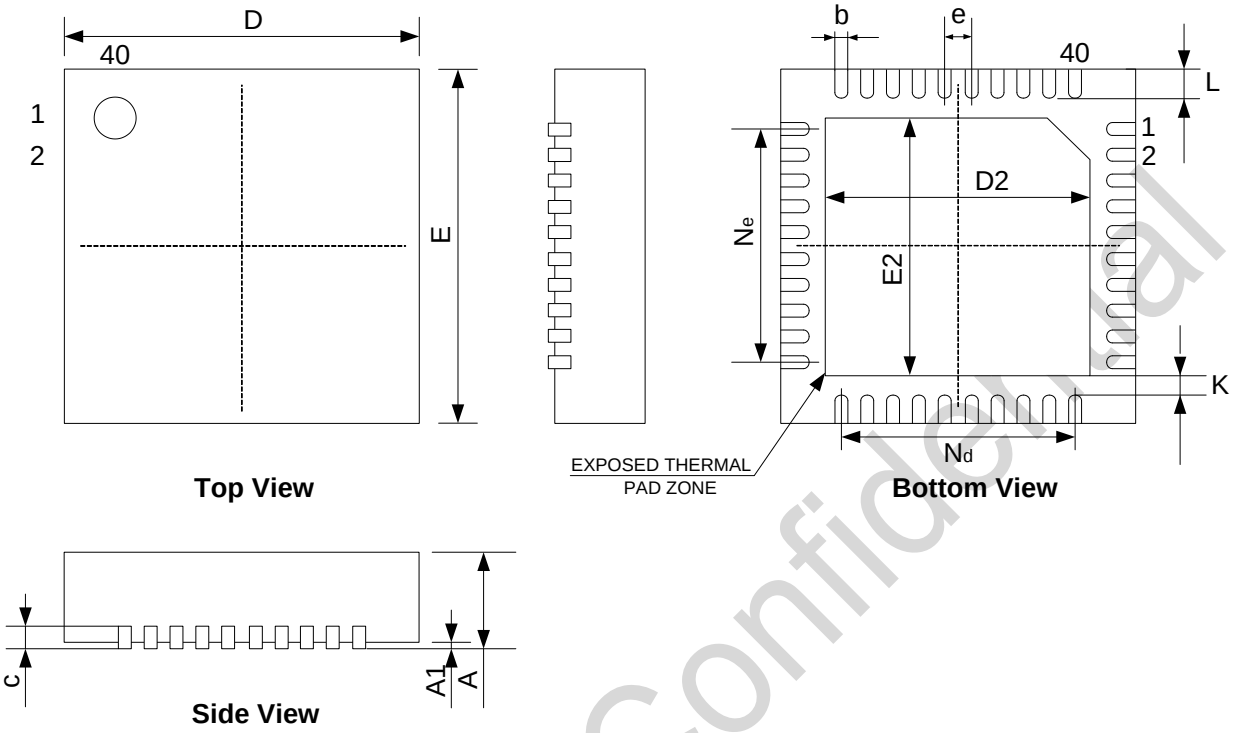


Figure 33. QFN405x5 Packaging

Table 37. QFN405x5 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
C	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.40 BSC		
Ne	3.60 BSC		
Nd	3.60 BSC		
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.35	0.40	0.45
L1	0.10REF		
K	0.20	-	-
h	0.30	0.35	0.40

8 Top Marking

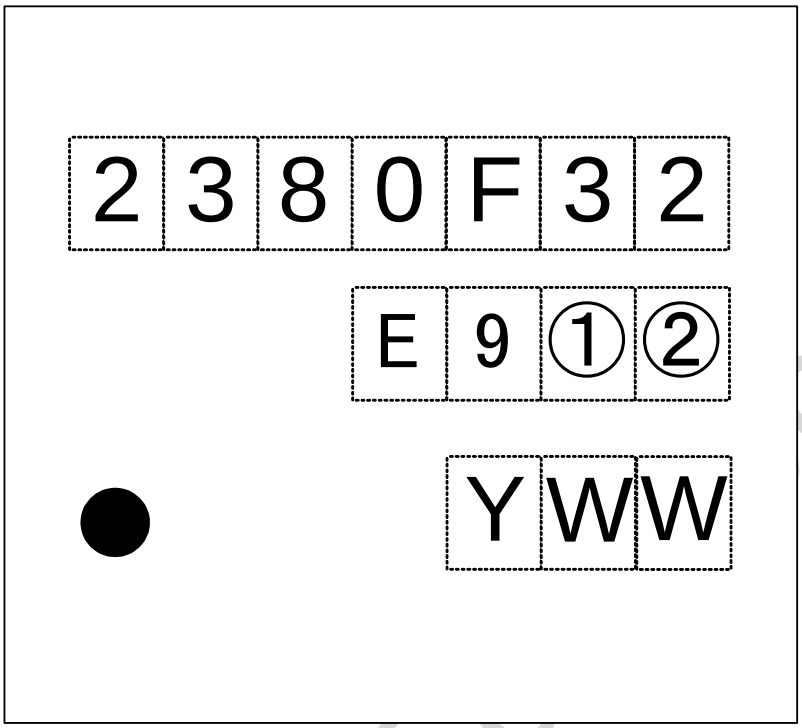


Figure 34. The CMT2380F32 Top Marking

Table 38. The CMT2380F32 Top Marking Information

Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 0.3 mm
Font Size	0.5 mm, align right
Line 1 Marking	2380F32 referring to model CMT2380F32
Line 2 Marking	E9①② is internal tracing code
Line 3 Marking	The date code is assigned by the package factory. Y is the last digit of the year. WW is the working week.

9 Reference Documents

Table 39. Reference Documents

Doc No.	Name	Description
AN141	CMT2300A Schematic and PCB Layout Guide	CMT2380F32 RF matching design guidelines
AN142	CMT2300A Quick Start Guide	CMT2380F32 RF quick start
AN143	CMT2300A FIFO and Packet Format Usage Guide	CMT2380F32 RF transceiver message usage guide
AN144	CMT2300A RSSI User Guide	CMT2380F32 RF RSSI user guide
AN146	CMT2300A Low Power Mode User Guide	CMT2380F32 RF Low power design guidelines
AN147	CMT2300A Features Usage Guide	CMT2380F32 RF features description
AN149	CMT2300A RF Parameter Configuration Guide	CMT2380F32 RF Frequency matching parameters
AN150	CMT2300A Low Voltage Transmit Power Compensation	CMT2380F32 RF Low-voltage transmit power compensation instructions
AN197	CMT2300A-CMT2119B-CMT2219B Fast Manual Frequency Hopping	CMT2380F32 fast manual frequency hopping instructions
AN198	CMT2300A-CMT2119B-CMT2219B Status Switching Precautions	CMT2380F32 RF status switching considerations
AN199	CMT2300A-CMT2119B-CMT2219B RF Frequency Calculation Guide	CMT2380F32 RF frequency calculation instructions
AN220	CMT2380F32 User Manual (Microcontroller Section)	CMT2380F32 controller detailed instructions

10 Revise History

Table 40. Revise History Records

Version No.	Chapter	Description	Date
0.8	All	Initial version	2018-04-22
0.9	7	Packaging diagram update	2018-05-09

11 Contacts

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