

NuMicro™ Family

Nano100 Series Product Brief

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Table of Contents

	<i>LIST OF FIGURES</i>	4
	<i>LIST OF TABLES</i>	5
1	GENERAL DESCRIPTION	6
2	FEATURES	8
2.1	Nano100 Features – Base Line	8
2.2	Nano110 Features – LCD Line	14
2.3	Nano120 Features – USB Connectivity Line	20
2.4	Nano130 Features – Advanced Line.....	26
3	PARTS INFORMATION LIST AND PIN CONFIGURATION	32
3.1	NuMicro™ Nano100 Series Selection Code.....	32
3.2	NuMicro™ Nano100 Products Selection Guide.....	33
3.2.1	NuMicro™ Nano100 Base Line Selection Guide.....	33
3.2.2	NuMicro™ Nano110 LCD Line Selection Guide.....	33
3.2.3	NuMicro™ Nano120 USB Connectivity Line Selection Guide.....	33
3.2.4	NuMicro™ Nano130 Advanced Line Selection Guide.....	33
3.3	Pin Configuration.....	34
3.3.1	NuMicro™ Nano100 Pin Diagrams	34
3.3.2	NuMicro™ Nano110 Pin Diagrams	37
3.3.3	NuMicro™ Nano120 Pin Diagrams	39
3.3.4	NuMicro™ Nano130 Pin Diagrams	42
4	BLOCK DIAGRAM	44
4.1	Nano100 Block Diagram	44
4.2	Nano110 Block Diagram	45
4.3	Nano120 Block Diagram	46
4.4	Nano130 Block Diagram	47
5	APPLICATION CIRCUIT	48
5.1	LCD Charge Pump.....	48
5.1.1	C-type 1/3 Bias.....	48
5.1.2	C-type 1/2 Bias.....	48
5.2	ADC Application Circuit.....	49
5.2.1	Voltage Reference Source	49
5.3	DAC Application Circuit.....	51
5.3.1	Voltage Reference Source	51
5.4	Whole Chip Application Circuit.....	53
6	POWER COMSUMPTION	54
7	ELECTRICAL CHARACTERISTIC	55
7.1	Absolute Maximum Ratings	55
7.2	Nano100/Nano110/Nano120/Nano130 DC Electrical Characteristics.....	56
7.3	AC Electrical Characteristics.....	61
7.3.1	External Input Clock	61



7.3.2	External 4~24 MHz XTAL Oscillator	61
7.3.3	External 32.768 kHz Crystal	62
7.3.4	Internal 12 MHz Oscillator	62
7.3.5	Internal 10 kHz Oscillator	62
7.4	Analog Characteristics	63
7.4.1	12-bit ADC	63
7.4.2	Brown-out Detector.....	63
7.4.3	Power-on Reset.....	64
7.4.4	Temperature Sensor.....	64
7.4.5	12-bit DAC	64
7.4.6	LCD	65
7.4.7	Touch Key (TK)	65
7.4.8	Internal Voltage Reference.....	66
7.4.9	USB PHY Specifications.....	66
8	PACKAGE DIMENSIONS	68
8.1	128L LQFP (14x14x1.4 mm footprint 2.0 mm).....	68
8.2	64L LQFP (7x7x1.4 mm footprint 2.0 mm).....	69
8.3	48L LQFP (7x7x1.4 mm footprint 2.0 mm).....	71
9	REVISION HISTORY	72

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List of Figures

Figure 3-1 NuMicro™ Nano100 Series Selection Code 32

Figure 3-2 NuMicro™ Nano100 LQFP 128-pin Diagram 34

Figure 3-3 NuMicro™ Nano100 LQFP 64-pin Diagram 35

Figure 3-4 NuMicro™ Nano100 LQFP 48-pin Diagram 36

Figure 3-5 NuMicro™ Nano110 LQFP 128-pin Diagram 37

Figure 3-6 NuMicro™ Nano110 LQFP 64-pin Diagram 38

Figure 3-7 NuMicro™ Nano120 LQFP 128-pin Diagram 39

Figure 3-8 NuMicro™ Nano120 LQFP 64-pin Diagram 40

Figure 3-9 NuMicro™ Nano120 LQFP 48-pin Diagram 41

Figure 3-10 NuMicro™ Nano130 LQFP 128-pin Diagram 42

Figure 3-11 NuMicro™ Nano130 LQFP 64-pin Diagram 43

Figure 4-1 NuMicro™ Nano100 Block Diagram 44

Figure 4-2 NuMicro™ Nano110 Block Diagram 45

Figure 4-3 NuMicro™ Nano120 Block Diagram 46

Figure 4-4 NuMicro™ Nano130 Block Diagram 47

Figure 9-1 Typical Crystal Application Circuit 61



LIST OF TABLES

Table 1-1 Connectivity Support Table.....	7
Table 3-1 Nano100 Base Line Selection Table	33
Table 3-2 Nano110 LCD Line Selection Table	33
Table 3-3 Nano120 USB Connectivity Line Selection Table	33
Table 3-4 Nano130 Advanced Line Selection Table	33

1 GENERAL DESCRIPTION

The Nano100 series ultra-low power 32-bit microcontroller is embedded with ARM® Cortex™-M0 core operated at a wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded Flash and 8K/16K-byte embedded SRAM. Integrating LCD 4x40 or 6x38 (COM/Segment), USB 2.0 full-speed function, RTC, 12-bit SAR ADC, 12-bit DAC, Capacitive Touch-Key and provides high performance connectivity peripheral interfaces such as UART, SPI, I2C, I2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and ISO-7816-3 for Smart card, the Nano100 series supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano100 series provides low power voltage, low power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano100 series is suitable for a wide range of battery device applications such as:

- Portable Data Collector
- Portable Medical Monitor
- Portable RFID Reader
- Portable Barcode Scanner
- Security Alarm System
- System Supervisors
- Power Metering
- USB Accessories
- Smart Card Reader
- Wireless Game Control Device
- IPTV Remote Smart Keyboard
- Wireless Sensors Node Device (WSN)
- Wireless RF4CE Remote Control
- Wireless Audio
- Wireless Automatic Meter Reader (AMR)
- Electronic Toll Collection (ETC)

The Nano100 Base line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates RTC, 12- channels 12-bit SAR ADC, 2-channels 12-bit DAC, 16-channels Capacitive Touch-Key and provides high performance connectivity peripheral interfaces such as 2xUART, 3xSPI, 2xI2C, I2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano100 Base line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano110 LCD line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates LCD 4x40 or 6x38 (COM/Segment). RTC, 12-channels 12-bit SAR ADC, 2-channels 12-bit DAC, 16-channels Capacitive Touch-Key and provides high performance connectivity peripheral interfaces such as 2xUART, 2xSPI, 2xI2C, I2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano110 LCD line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via



many peripheral interfaces.

The Nano120 USB Connectivity line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates USB 2.0 full-speed device function, RTC, 12-channels 12-bit SAR ADC, 2-channels 12-bit DAC, 16-channels Capacitive Touch-Key and provides high performance connectivity peripheral interfaces such as 2xUART, 3xSPI, 2xI2C, I2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano120 USB Connectivity line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano130 Advanced line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrated LCD 4x40 or 6x38 (COM/Segment), USB 2.0 full-speed device function, RTC, 8-channels 12-bit SAR ADC, 2-channels 12-bit DAC, Capacitive Touch-Key and provides high performance connectivity peripheral interfaces such as 2xUART, 2xSPI, 2xI2C, I2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano130 Advanced line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

Product Line	UART	SPI	I2C	I2S	USB	LCD	ADC	DAC	TK	RTC	EBI	SC	Timer
Nano100	•	•	•	•			•	•	•	•	•	•	•
Nano110	•	•	•	•		•	•	•	•	•	•	•	•
Nano120	•	•	•	•	•		•	•	•	•	•	•	•
Nano130	•	•	•	•	•	•	•	•	•	•	•	•	•

Table 1-1 Connectivity Support Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano100 Features – Base Line

- Core
 - ◆ ARM® Cortex™-M0 core running up to 42 MHz
 - ◆ One 24-bit system timer
 - ◆ Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
 - ◆ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
 - ◆ Runs up to 42 MHz with zero wait state for discontinuous address read access
 - ◆ 64K/32K/123K bytes application program memory (APROM)
 - ◆ 4 KB in system programming (ISP) loader program memory (LDROM)
 - ◆ Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
 - ◆ 16K/8K bytes embedded SRAM
 - ◆ Supports DMA mode
- DMA: Supports 8 channels: one VDMA channel, 6 PDMA channels and one CRC channel
 - ◆ VDMA
 - Memory-to-memory transfer
 - Supports block transfer with stride
 - Supports word/half-word/byte boundary address
 - Supports address direction: increment and decrement
 - ◆ PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
 - Supports word/half-word/byte transfer data width from/to peripheral

- Supports address direction: increment, fixed, and wrap around
 - ◆ CRC
 - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
 - ◆ CRC-8: $X^8 + X^2 + X + 1$
 - ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
 - ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Clock Control
 - ◆ Flexible selection for different applications
 - ◆ Built-in 12MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12MHz OSC has 1 % deviation within all temperature range.
 - ◆ Low power 10 kHz OSC for watchdog and low power system operation
 - ◆ Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
 - ◆ External 4~24 MHz crystal input for precise timing operation
 - ◆ External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
 - ◆ Three I/O modes:
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
 - ◆ All inputs with Schmitt trigger
 - ◆ I/O pin configured as interrupt source with edge/level setting
 - ◆ Supports High Driver and High Sink I/O mode
 - ◆ Supports input 5V tolerance, except PA.0 ~ PA.7, PD.0 ~ PD.1 and PC.6 ~ PC.7
- Timer
 - ◆ Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
 - ◆ Independent Clock Source for each timer
 - ◆ Provides one-shot and periodic, and continuous operation modes
 - ◆ Internal trigger event to ADC, DAC module
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- Watchdog Timer

- ◆ Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
- ◆ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
- ◆ Interrupt or reset selectable when watchdog time-out
- ◆ Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
 - ◆ 6-bit down counter and 6-bit compare value to make the window period flexible
 - ◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
 - ◆ Supports software compensation by setting frequency compensate register (FCR)
 - ◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - ◆ Supports Alarm registers (second, minute, hour, day, month, year)
 - ◆ Selectable 12-hour or 24-hour mode
 - ◆ Automatic leap year recognition
 - ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - ◆ Wake system up from Power-down mode
 - ◆ Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
- PWM/Capture
 - ◆ Supports 2 PWM modules, each has two 16-bit PWM generators
 - ◆ Provides eight PWM outputs or four complementary paired PWM outputs
 - ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
 - ◆ (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
 - ◆ Supports One-shot and Continuous mode
 - ◆ Supports Capture interrupt
- UART
 - ◆ Up to two 16-byte FIFO UART controllers
 - ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
 - ◆ Supports IrDA (SIR) function
 - ◆ Supports LIN function
 - ◆ Supports RS-485 9 bit mode and direction control.
 - ◆ Programmable baud rate generator
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode

- SPI
 - ◆ Up to three sets of SPI controller
 - ◆ Master up to 32 MHz, and Slave up to 16 MHz
 - ◆ Supports SPI/MICROWIRE Master/Slave mode
 - ◆ Full duplex synchronous serial data transfer
 - ◆ Variable length of transfer data from 4 to 32 bits
 - ◆ MSB or LSB first data transfer
 - ◆ RX and TX on both rising or falling edge of serial clock independently
 - ◆ Two slave/device select lines when SPI controller is used as the master, and 1 slave/device select line when SPI controller is used as the slave
 - ◆ Supports byte suspend mode in 32-bit transmission
 - ◆ Supports two channel PDMA requests, one for transmit and another for receive
 - ◆ Supports three wire mode, no slave select signal, bi-direction interface
 - ◆ Wake system up from Power-down mode
- I2C
 - ◆ Up to two sets of I2C device
 - ◆ Master/Slave up to 1 Mbit/s
 - ◆ Bi-directional data transfer between masters and slaves
 - ◆ Multi-master bus (no central master)
 - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - ◆ Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
 - ◆ Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - ◆ Built-in 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allowing for versatile rate control
 - ◆ Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave addresses with mask option)
- I2S
 - ◆ Interface with external audio CODEC
 - ◆ Operated as either Master or Slave mode
 - ◆ Capable of handling 8, 16, 24 and 32 bit word sizes
 - ◆ Supports Mono and stereo audio data
 - ◆ Supports I2S and MSB justified data format
 - ◆ Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving

- ◆ Generates interrupt requests when buffer levels cross a programmable boundary
- ◆ Supports two PDMA requests: one for transmitting and the other for receiving
- ADC
 - ◆ 12-bit SAR ADC up to 2Msps conversion rate
 - ◆ Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3)
 - ◆ Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS.
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
 - ◆ Each channel with individual result register
 - ◆ Only scan on enabled channels
 - ◆ Threshold voltage detection (comparator function)
 - ◆ Conversion started by software programming or external input
 - ◆ Supports PDMA mode
 - ◆ Supports up to four timer time-out events (TRM0_CH0, TMR0_CH1, TMR1_CH0 and TMR1_CH1) to enable ADC
- DAC
 - ◆ 12-bit monotonic output with 400K conversion rate
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Synchronized update capability for two DACs (group function)
 - ◆ Supports up to four timer time-out events (TMR0_CH0, TMR0_CH1, TMR1_CH0, TMR1_CH1), software or PDMA to trigger DAC to conversion
- Touch Key(TK)
 - ◆ Supports programmable counter depth (16-bit, 14-bit, 12-bit and 10-bit) for sensitivity adjustment
 - ◆ Supports programmable charge current for sensitivity adjustment
 - ◆ Supports programmable Clock Source frequency for sensitivity adjustment
 - ◆ Supports up to 16 touch-keys scanning
 - ◆ Supports external reference capacitor for different sensing environment adjustment
- SmartCard (SC)
 - ◆ Compliant to ISO-7816-3 T=0, T=1
 - ◆ Supports up to three ISO-7816-3 ports
 - ◆ Separates receive/transmit 4 bytes entry FIFO for data payloads
 - ◆ Programmable transmission clock frequency
 - ◆ Programmable receiver buffer trigger level

- ◆ Programmable guard time selection (11 ETU ~ 266 ETU)
- ◆ A 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
- ◆ Supports auto inverse convention function
- ◆ Supports stop clock level and clock stop (clock keep) function
- ◆ Supports transmitter and receiver error retry and error limit function
- ◆ Supports hardware activation sequence process
- ◆ Supports hardware warm reset sequence process
- ◆ Supports hardware deactivation sequence process
- ◆ Supports hardware auto deactivation sequence when detect the card is removal
- ◆ Supports UART mode
- EBI (External bus interface) support
 - ◆ Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
 - ◆ Supports 8bit/16bit data width
 - ◆ Supports byte write in 16-bit Data Width mode
- One built-in temperature sensor with 1°C resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40°C ~85°C
- Packages:
 - ◆ All Green package (RoHS)
 - ◆ LQFP 128-pin(14x14) / 64-pin(7x7) / 48-pin(7x7)

2.2 Nano110 Features – LCD Line

- Core
 - ◆ ARM® Cortex™-M0 core running up to 42 MHz
 - ◆ One 24-bit system timer
 - ◆ Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
 - ◆ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
 - ◆ Runs up to 42 MHz with zero wait state for discontinuous address read access.
 - ◆ 64K/32K/123K bytes application program memory (APROM)
 - ◆ 4 KB In System Programming (ISP) loader program memory (LDROM)
 - ◆ Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
 - ◆ 16K/8K bytes embedded SRAM
 - ◆ Supports DMA mode
- DMA : Supports 8 channels: one VDMA channel, 6 PDMA channels, and one CRC channel
 - ◆ VDMA
 - Memory-to-memory transfer
 - Supports block transfer with stride
 - Supports word/half-word/byte boundary address
 - Supports address direction: increment and decrement
 - ◆ PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
 - Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address direction: increment, fixed, and wrap around
 - ◆ CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
 - ◆ CRC-8: $X^8 + X^2 + X + 1$
 - ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
 - ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Clock Control
 - ◆ Flexible selection for different applications
 - ◆ Built-in 12MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12MHz OSC has 1 % deviation within all temperature range.
 - ◆ Low power 10 kHz OSC for watchdog and low power system operation
 - ◆ Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
 - ◆ External 4~24 MHz crystal input for precise timing operation
 - ◆ External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
 - ◆ Three I/O modes:
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
 - ◆ All inputs with Schmitt trigger
 - ◆ I/O pin configured as interrupt source with edge/level setting
 - ◆ Supports High Driver and High Sink I/O mode
 - ◆ Supports input 5V tolerance, except PA.0 ~ PA.7, PD.0 ~ PD.1 and PC.6 ~ PC.7)
- Timer
 - ◆ Supports 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
 - ◆ Independent Clock Source for each timer
 - ◆ Provides one-shot and periodic, and continuous operation modes
 - ◆ Internal trigger event to ADC, DAC module
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- Watchdog Timer
 - ◆ Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)

- ◆ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
- ◆ Interrupt or reset selectable when watchdog time-out
- ◆ Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
 - ◆ 6-bit down counter and 6-bit compare value to make the window period flexible
 - ◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
 - ◆ Supports software compensation by setting frequency compensate register (FCR)
 - ◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - ◆ Supports Alarm registers (second, minute, hour, day, month, year)
 - ◆ Selectable 12-hour or 24-hour mode
 - ◆ Automatic leap year recognition
 - ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - ◆ Wake system up from Power-down mode
 - ◆ Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
- PWM/Capture
 - ◆ Supports 2 PWM modules, each has two 16-bit PWM generators
 - ◆ Provides eight PWM outputs or four complementary paired PWM outputs
 - ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
 - ◆ (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
 - ◆ Supports Capture interrupt
- UART
 - ◆ Up to two 16-byte FIFO UART controllers
 - ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
 - ◆ Supports IrDA (SIR) function
 - ◆ Supports LIN function
 - ◆ Supports RS-485 9 bit mode and direction control (Low Density Only)
 - ◆ Programmable baud rate generator
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- SPI
 - ◆ Up to three sets of SPI controller

- ◆ Master up to 32 MHz, and Slave up to 16 MHz
- ◆ Supports SPI/MICROWIRE Master/Slave mode
- ◆ Full duplex synchronous serial data transfer
- ◆ Variable length of transfer data from 4 to 32 bits
- ◆ MSB or LSB first data transfer
- ◆ RX and TX on both rising or falling edge of serial clock independently
- ◆ Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- ◆ Supports byte suspend mode in 32-bit transmission
- ◆ Supports two channel PDMA requests, one for transmit and another for receive
- ◆ Supports three wire mode, no slave select signal, bi-direction interface
- ◆ Wake system up from Power-down mode
- I2C
 - ◆ Up to two sets of I2C device
 - ◆ Master/Slave up to 1Mbit/s
 - ◆ Bidirectional data transfer between masters and slaves
 - ◆ Multi-master bus (no central master)
 - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - ◆ Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
 - ◆ Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - ◆ Built-in 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allow versatile rate control
 - ◆ Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave address with mask option)
- I2S
 - ◆ Interface with external audio CODEC
 - ◆ Operated as either Master or Slave mode
 - ◆ Capable of handling 8, 16, 24 and 32 bit word sizes
 - ◆ Supports Mono and stereo audio data
 - ◆ Supports I2S and MSB justified data format
 - ◆ Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
 - ◆ Generates interrupt requests when buffer levels cross a programmable boundary
 - ◆ Supports two PDMA requests: one for transmitting and the other for receiving

- ADC
 - ◆ 12-bit SAR ADC up to 2Msps conversion rate
 - ◆ Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3)
 - ◆ Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Single scan/single cycle scan/continuous scan
 - ◆ Each channel with individual result register
 - ◆ Only scan on enabled channels
 - ◆ Threshold voltage detection (comparator function)
 - ◆ Conversion start by software programming or external input
 - ◆ Supports PDMA mode
 - ◆ Supports up to four timer time-out events (TMR0_CH0, TMR0_CH1, TMR1_CH0, and TMR1_CH1) to enable ADC
- DAC
 - ◆ 12-bit monotonic output with 400K conversion rate
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Synchronized update capability for two DACs (group function)
 - ◆ Supports up to four timer time-out events (TMR0_CH0, TMR0_CH1, TMR1_CH0, TMR1_CH1), software or PDMA to trigger DAC to conversion
- Touch Key(TK)
 - ◆ Supports programmable counter depth(16-bit, 14-bit, 12-bit and 10-bit) for sensitivity adjustment
 - ◆ Supports programmable charge current for sensitivity adjustment
 - ◆ Supports programmable Clock Source frequency for sensitivity adjustment
 - ◆ Supports up to 16 touch-keys scanning
 - ◆ Supports external reference capacitor for different sensing environment adjustment
- SmartCard (SC)
 - ◆ Compliant to ISO-7816-3 T=0, T=1
 - ◆ Supports up to three ISO-7816-3 ports
 - ◆ Separates receive / transmit 4 bytes entry FIFO for data payloads
 - ◆ Programmable transmission clock frequency
 - ◆ Programmable receiver buffer trigger level
 - ◆ Programmable guard time selection (11 ETU ~ 266 ETU)
 - ◆ A 24-bit and two 8-bit time-out counter for Answer to Request (ATR) and waiting times processing

- ◆ Supports auto inverse convention function
- ◆ Supports stop clock level and clock stop (clock keep) function
- ◆ Supports transmitter and receiver error retry and error limit function
- ◆ Supports hardware activation sequence process
- ◆ Supports hardware warm reset sequence process
- ◆ Supports hardware deactivation sequence process
- ◆ Supports hardware auto deactivation sequence when detect the card is removal
- ◆ Supports UART mode
- LCD
 - ◆ LCD driver for up to 4 COM x 40 SEG or 6 COM x 38 SEG
 - ◆ Supports Static, 1/2 bias and 1/3 bias voltage
 - ◆ Four display modes; Static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty.
 - ◆ Selectable LCD frequency by frequency divider
 - ◆ Configurable frame frequency
 - ◆ Internal Charge pump, adjustable contrast adjustment
 - ◆ Configurable Charge pump frequency
 - ◆ Blinking capability
 - ◆ Supports R-type/C-type method
 - ◆ LCD frame interrupt
- One built-in temperature sensor with 1°C resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40°C ~85°C
- Packages:
 - ◆ All Green package (RoHS)
 - ◆ LQFP 128-pin(14x14) / 64-pin(7x7)

2.3 Nano120 Features – USB Connectivity Line

- Core
 - ◆ ARM® Cortex™-M0 core running up to 42 MHz
 - ◆ One 24-bit system timer
 - ◆ Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
 - ◆ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
 - ◆ Runs up to 42 MHz with zero wait state for discontinuous address read access.
 - ◆ 64K/32K/123K bytes application program memory (APROM)
 - ◆ 4KB in system programming (ISP) loader program memory (LDROM)
 - ◆ Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
 - ◆ 16K/8K bytes embedded SRAM
 - ◆ Supports PDMA mode
- DMA: Support 8 channels: one VDMA channel, 6 PDMA channels, and one CRC channel
 - ◆ VDMA
 - Memory-to-memory transfer
 - Supports block transfer with stride
 - Supports word/half-word/byte boundary address
 - Supports address direction: increment and decrement
 - ◆ PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
 - Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address: increment, fixed, and wrap around
 - ◆ CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
 - ◆ CRC-8: $X^8 + X^2 + X + 1$
 - ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
 - ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Clock Control
 - ◆ Flexible selection for different applications
 - ◆ Built-in 12MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12MHz OSC has 1 % deviation within all temperature range
 - ◆ Low power 10 kHz OSC for watchdog and low power system operation
 - ◆ Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
 - ◆ External 4~24 MHz crystal input for precise timing operation
 - ◆ External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
 - ◆ Three I/O modes:
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
 - ◆ All inputs with Schmitt trigger
 - ◆ I/O pin can be configured as interrupt source with edge/level setting
 - ◆ High driver and high sink IO mode support
 - ◆ Supports input 5V tolerance (except ADC and DAC shared pins)
- Timer
 - ◆ Supports 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
 - ◆ Independent Clock Source for each timer
 - ◆ Provides one-shot, periodic, and continuous operation modes
 - ◆ Internal trigger event to ADC, DAC module
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- Watchdog Timer
 - ◆ Clock Source from LIRC. (Internal 10 kHz Low Speed Oscillator Clock)
 - ◆ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)

- ◆ Interrupt or reset selectable on watchdog time-out
- ◆ Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
 - ◆ 6-bit down counter and 6-bit compare value to make the window period flexible
 - ◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
 - ◆ Supports software compensation by setting frequency compensate register (FCR)
 - ◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - ◆ Supports Alarm registers (second, minute, hour, day, month, year)
 - ◆ Selectable 12-hour or 24-hour mode
 - ◆ Automatic leap year recognition
 - ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - ◆ Wake system up from Power-down or Idle mode
 - ◆ Support 80 bytes spare registers and a snoop pin to clear the content of these spare registers
- PWM/Capture
 - ◆ Supports 2 PWM module, each has two 16-bit PWM generators
 - ◆ Provide eight PWM outputs or four complementary paired PWM outputs
 - ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-Zone generator for complementary paired PWM
 - ◆ (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
 - ◆ Supports one shot and continuous mode
 - ◆ Supports Capture interrupt
- UART
 - ◆ Up to two 16-byte FIFO UART controllers
 - ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
 - ◆ Supports IrDA (SIR) function
 - ◆ Supports LIN function
 - ◆ Supports RS-485 9 bit mode and direction control. (Low Density Only)
 - ◆ Programmable baud rate generator
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- SPI
 - ◆ Up to three sets of SPI controller

- ◆ Master up to 32 MHz, and Slave up to 16 MHz
- ◆ Supports SPI/MICROWIRE Master/Slave mode
- ◆ Full duplex synchronous serial data transfer
- ◆ Variable length of transfer data from 4 to 32 bits
- ◆ MSB or LSB first data transfer
- ◆ RX and TX on both rising or falling edge of serial clock independently
- ◆ Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- ◆ Supports byte suspend mode in 32-bit transmission
- ◆ Supports two channel PDMA requests, one for transmit and another for receive
- ◆ Supports three wire, no slave select signal, bi-direction interface
- ◆ Wake system up from Power-down mode
- I2C
 - ◆ Up to two sets of I2C device
 - ◆ Master/Slave up to 1Mbit/s
 - ◆ Bi-directional data transfer between masters and slaves
 - ◆ Multi-master bus (no central master)
 - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - ◆ Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
 - ◆ Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - ◆ Built-in 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allow versatile rate control
 - ◆ Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave addresses with mask option)
- I2S
 - ◆ Interface with external audio CODEC
 - ◆ Operated as either Master or Slave mode
 - ◆ Capable of handling 8, 16, 24 and 32 bit word sizes
 - ◆ Supports Mono and stereo audio data
 - ◆ Supports I2S and MSB justified data format
 - ◆ Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
 - ◆ Generates interrupt requests when buffer levels cross a programmable boundary
 - ◆ Supports two PDMA requests: one for transmitting and the other for receiving

- ADC
 - ◆ 12-bit SAR ADC up to 2Msps conversion rate
 - ◆ Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3).
 - ◆ Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS.
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD
 - ◆ Supports single scan, single cycle scan, and continuous scan modes
 - ◆ Each channel with individual result register
 - ◆ Only scan on enabled channels
 - ◆ Threshold voltage detection (comparator function)
 - ◆ Conversion start by software programming or external input
 - ◆ Supports PDMA mode
 - ◆ Supports up to four timer time-out events (TMR0_CH0, TMR0_CH1, TMR1_CH0, TMR1_CH1) to enable ADC
- DAC
 - ◆ 12-bit monotonic output with 400K conversion rate
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Synchronized update capability for two DACs (group function)
 - ◆ Supports up to four timer time-out event (TMR0_CH0, TMR0_CH1, TMR1_CH0, and TMR1_CH1), software or PDMA to trigger DAC to conversion
- Touch Key(TK)
 - ◆ Supports programmable counter depth(16-bit, 14-bit, 12-bit and 10-bit) for sensitivity adjustment
 - ◆ Supports programmable charge current for sensitivity adjustment
 - ◆ Supports programmable Clock Source frequency for sensitivity adjustment
 - ◆ Supports up to 16 touch-keys scanning
 - ◆ Supports external reference capacitor for different sensing environment adjustment
- SmartCard (SC)
 - ◆ Compliant to ISO-7816-3 T=0, T=1
 - ◆ Supports up to three ISO-7816-3 ports
 - ◆ Separates receive / transmit 4 bytes entry FIFO for data payloads
 - ◆ Programmable transmission clock frequency
 - ◆ Programmable receiver buffer trigger level
 - ◆ Programmable guard time selection (11 ETU ~ 266 ETU)
 - ◆ A 24-bit and two 8-bit time-out counter for Answer to Request (ATR) and waiting times processing

- ◆ Supports auto inverse convention function
- ◆ Supports stop clock level and clock stop (clock keep) function
- ◆ Supports transmitter and receiver error retry and error limit function
- ◆ Supports hardware activation sequence process
- ◆ Supports hardware warm reset sequence process
- ◆ Supports hardware deactivation sequence process
- ◆ Supports hardware auto deactivation sequence when detect the card is removal
- ◆ Supports UART mode
- USB 2.0 Full-Speed Device
 - ◆ One set of USB 2.0 FS Device 12Mbps
 - ◆ On-chip USB Transceiver
 - ◆ Provides 1 interrupt source with 4 interrupt events
 - ◆ Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
 - ◆ Auto suspend function when no bus signaling for 3 ms
 - ◆ Provides 8 programmable endpoints
 - ◆ Includes 512 Bytes internal SRAM as USB buffer
 - ◆ Provides remote wake-up capability
- EBI (External bus interface) support
 - ◆ Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
 - ◆ Supports 8bit/16bit data width
 - ◆ Supports byte write in 16-bit Data Width mode
- One built-in temperature sensor with 1°C resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40°C~85°C
- Packages:
 - ◆ All Green package (RoHS)
 - ◆ LQFP 128-pin(14x14) / 64-pin(7x7) / 48-pin(7x7)

2.4 Nano130 Features – Advanced Line

- Core
 - ◆ ARM® Cortex™-M0 core running up to 42 MHz
 - ◆ One 24-bit system timer
 - ◆ Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
 - ◆ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
 - ◆ Runs up to 42 MHz with zero wait state for discontinuous address read access.
 - ◆ 64K/32K/123K bytes application program memory (APROM)
 - ◆ 4KB in system programming (ISP) loader program memory (LDRM)
 - ◆ Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
 - ◆ 16K/8K bytes embedded SRAM
 - ◆ Supports DMA mode
- DMA : Supports 8 channels: one VDMA channel, 6 PDMA channels, and one CRC channel
 - ◆ VDMA
 - Memory-to-memory transfer
 - Supports block transfer with stride
 - Supports word/half-word/byte boundary address
 - Supports address direction: increment and decrement
 - ◆ PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
 - Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address direction: increment, fixed, and wrap around
 - ◆ CRC
 - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32

- ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
- ◆ CRC-8: $X^8 + X^2 + X + 1$
- ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
- ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Clock Control
 - ◆ Flexible selection for different applications
 - ◆ Built-in 12MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12MHz OSC has 1 % deviation within all temperature range.
 - ◆ Low power 10 kHz OSC for watchdog and low power system operation
 - ◆ Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
 - ◆ External 4~24 MHz crystal input for precise timing operation
 - ◆ External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
 - ◆ Three I/O modes:
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
 - ◆ All inputs with Schmitt trigger
 - ◆ I/O pin configured as interrupt source with edge/level setting
 - ◆ Supports High Driver and High Sink I/O mode
 - ◆ Supports input 5V tolerance (except ADC and DAC shared pins)
- Timer
 - ◆ Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
 - ◆ Independent Clock Source for each timer
 - ◆ Provides One-shot, Periodic Operation, and continuous modes
 - ◆ Supports internal trigger event to ADC, DAC and PDMA
 - ◆ Wake system up from Power-down mode
- Watchdog Timer
 - ◆ Clock Source is from LIRC. (Internal 10 kHz Low Speed Oscillator Clock)
 - ◆ Selectable time-out period from 1.6ms ~ 26sec (depends on clock source)
 - ◆ Interrupt or reset selectable on watchdog time-out
 - ◆ WDT can wake system up from Power-down mode
- Window Watchdog Timer(WWDT)

- ◆ 6-bit down counter and 6-bit compare value to make the window period flexible
- ◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
 - ◆ Supports software compensation by setting frequency compensate register (FCR)
 - ◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - ◆ Supports Alarm registers (second, minute, hour, day, month, year)
 - ◆ Selectable 12-hour or 24-hour mode
 - ◆ Automatic leap year recognition
 - ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - ◆ Wake system up from Power-down or Idle mode
 - ◆ Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
- PWM/Capture
 - ◆ Supports 2 PWM module, each with two 16-bit PWM generators
 - ◆ Provides eight PWM outputs or four complementary paired PWM outputs
 - ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-Zone generator for complementary paired PWM
 - ◆ (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
 - ◆ Supports Capture interrupt
- UART
 - ◆ Up to two 16-byte FIFO UART controllers
 - ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
 - ◆ Supports IrDA (SIR) function
 - ◆ Supports LIN function
 - ◆ Supports RS-485 9 bit mode and direction control (Low Density Only)
 - ◆ Programmable baud rate generator
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down or Idle mode
- SPI
 - ◆ Up to 3 sets of SPI controller
 - ◆ Master up to 32 MHz, and Slave up to 16 MHz
 - ◆ Supports SPI/MICROWIRE Master/Slave mode
 - ◆ Full duplex synchronous serial data transfer
 - ◆ Variable length of transfer data from 4 to 32 bits
 - ◆ MSB or LSB first data transfer

- ◆ RX and TX on both rising or falling edge of serial clock independently
- ◆ Two slave/device select lines when used as the master, and 1 slave/device select line when used as the slave
- ◆ Supports byte suspend mode in 32-bit transmission
- ◆ Supports two channel PDMA request, one for transmit and another for receive
- ◆ Supports three wire, no slave select signal, bi-direction interface
- ◆ Wake system up from Power-down or Idle mode
- I2C
 - ◆ Up to two sets of I2C device
 - ◆ Master/Slave up to 1Mbit/s
 - ◆ Bi-directional data transfer between masters and slaves
 - ◆ Multi-master bus (no central master)
 - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - ◆ Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
 - ◆ Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
 - ◆ Built-in 14-bit time-out counter will request the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allowing for versatile rate control
 - ◆ Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave addresses with mask option)
- I2S
 - ◆ Interface with external audio CODEC
 - ◆ Operate as either Master or Slave mode
 - ◆ Capable of handling 8, 16, 24 and 32 bit word sizes
 - ◆ Supports Mono and stereo audio data
 - ◆ Supports I2S and MSB justified data format
 - ◆ Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
 - ◆ Generates interrupt requests when buffer levels cross a programmable boundary
 - ◆ Supports two PDMA requests: one for transmitting and the other for receiving
- ADC
 - ◆ 12-bit SAR ADC up to 2Msps conversion rate
 - ◆ Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3)
 - ◆ Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS.

- ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD
- ◆ Single scan/single cycle scan/continuous scan
- ◆ Each channel with individual result register
- ◆ Scan on enabled channels
- ◆ Threshold voltage detection (comparator function)
- ◆ Conversion start by software programming or external input
- ◆ Supports PDMA mode
- ◆ Supports up to four timer time-out events (TMR0_CH0, TMR0_CH1, TMR1_CH0, TMR1_CH1) to enable ADC
- DAC
 - ◆ 12-bit monotonic output with 400K conversion rate
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Synchronized update capability for two DACs (group function)
 - ◆ Supports up to four timer time-out events (TMR0_CH0, TMR0_CH1, TMR1_CH0, and TMR1_CH1), software or PDMA to trigger DAC to conversion
- Touch Key(TK)
 - ◆ Supports programmable counter depth(16-bit, 14-bit, 12-bit and 10-bit) for sensitivity adjustment
 - ◆ Supports programmable charge current for sensitivity adjustment
 - ◆ Supports programmable Clock Source frequency for sensitivity adjustment
 - ◆ Supports up to 16 touch-keys scanning
 - ◆ Supports external reference capacitor for different sensing environment adjustment
- SmartCard (SC)
 - ◆ Compliant to ISO-7816-3 T=0, T=1
 - ◆ Supports up to three ISO-7816-3 ports
 - ◆ Separates receive/transmit 4 bytes entry FIFO for data payloads
 - ◆ Programmable transmission clock frequency
 - ◆ Programmable receiver buffer trigger level
 - ◆ Programmable guard time selection (11 ETU ~ 266 ETU)
 - ◆ A 24-bit and two 8-bit time-out counter for Answer to Request (ATR) and waiting times processing
 - ◆ Supports auto inverse convention function
 - ◆ Supports stop clock level and clock stop (clock keep) function
 - ◆ Supports transmitter and receiver error retry and error limit function
 - ◆ Supports hardware activation sequence process
 - ◆ Supports hardware warm reset sequence process
 - ◆ Supports hardware deactivation sequence process

- ◆ Supports hardware auto deactivation sequence when detecting the card is removed
- ◆ Support UART mode
- LCD
 - ◆ LCD driver for up to 4 COM x 40 SEG or 6 COM x 38 SEG
 - ◆ Supports Static, 1/2 bias and 1/3 bias voltage
 - ◆ Four display modes: Static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty.
 - ◆ Selectable LCD frequency by frequency divider
 - ◆ Configurable frame frequency
 - ◆ Internal Charge pump, adjustable contrast adjustment
 - ◆ Configurable Charge pump frequency
 - ◆ Blinking capability
 - ◆ Supports R-type/C-type method
 - ◆ LCD frame interrupt
- USB 2.0 Full-speed Device
 - ◆ One set of USB 2.0 FS Device 12Mbps
 - ◆ On-chip USB Transceiver
 - ◆ Provides 1 interrupt source with 4 interrupt events
 - ◆ Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
 - ◆ Auto suspend function when no bus signaling for 3 ms
 - ◆ Provides 8 programmable endpoints
 - ◆ Includes 512 Bytes internal SRAM as USB buffer
 - ◆ Provides remote wake-up capability
- EBI (External bus interface)
 - ◆ Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
 - ◆ Supports 8bit/16bit data width
 - ◆ Supports byte write in 16-bit data width mode
- One built-in temperature sensor with 1°C resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40°C~85°C
- Packages:
 - ◆ All Green package (RoHS)
 - ◆ LQFP 128-pin(14x14) / 64-pin (7x7)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ Nano100 Series Selection Code

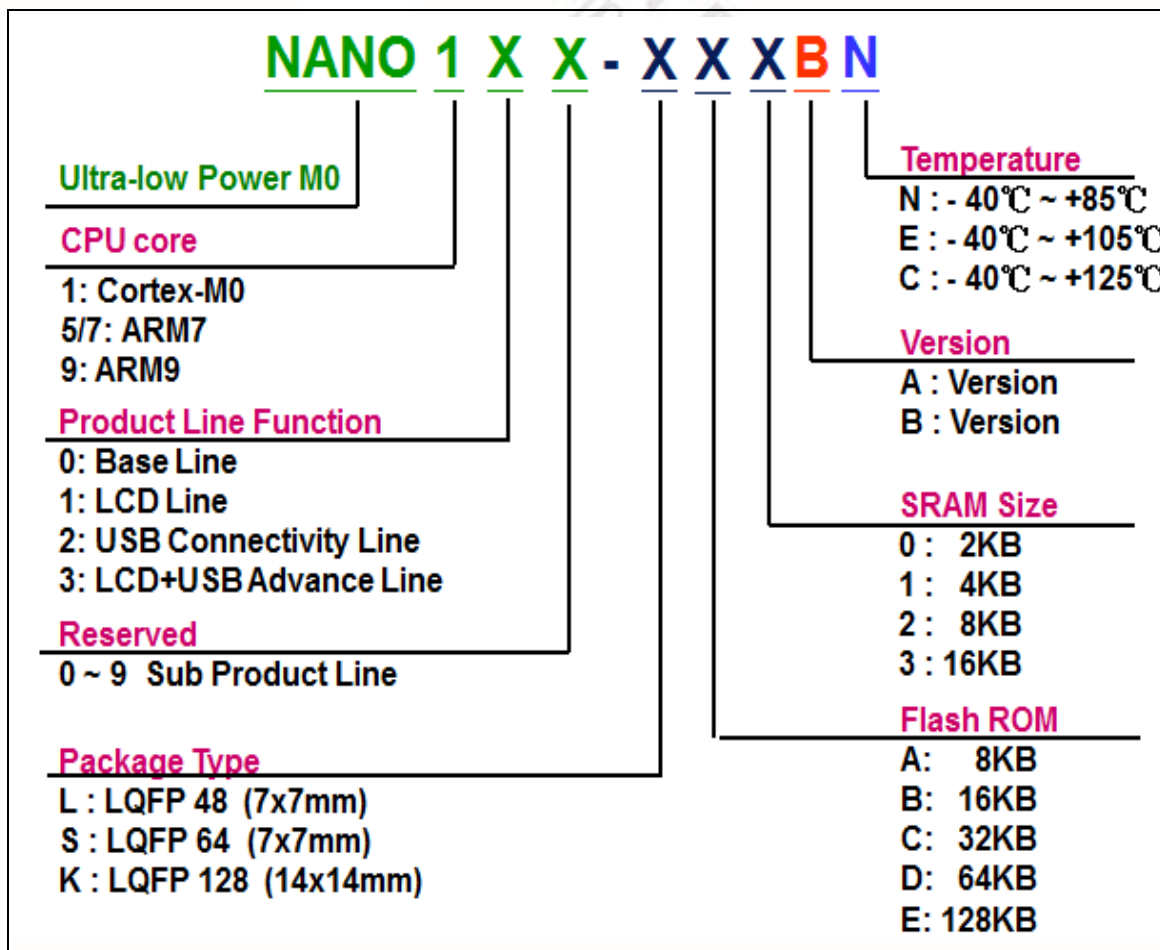


Figure 3-1 NuMicro™ Nano100 Series Selection Code

新唐科技 NUVOTON
INTELLECTUAL PROPERTY

3.3 Pin Configuration

3.3.1 NuMicro™ Nano100 Pin Diagrams

3.3.1.1 NuMicro™ Nano100 LQFP 128-pin

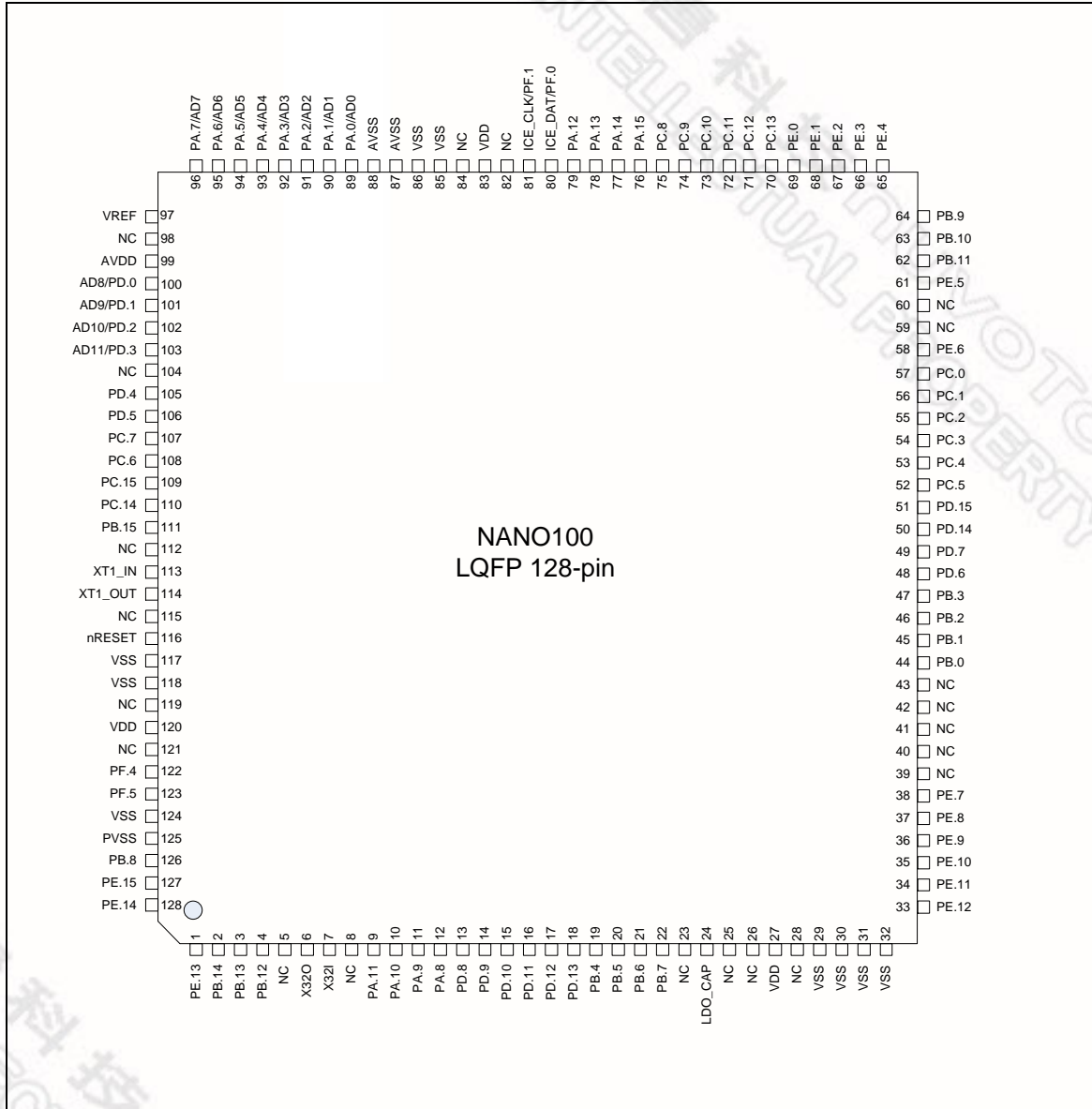


Figure 3-2 NuMicro™ Nano100 LQFP 128-pin Diagram

3.3.1.2 NuMicro™ Nano100 LQFP 64-pin

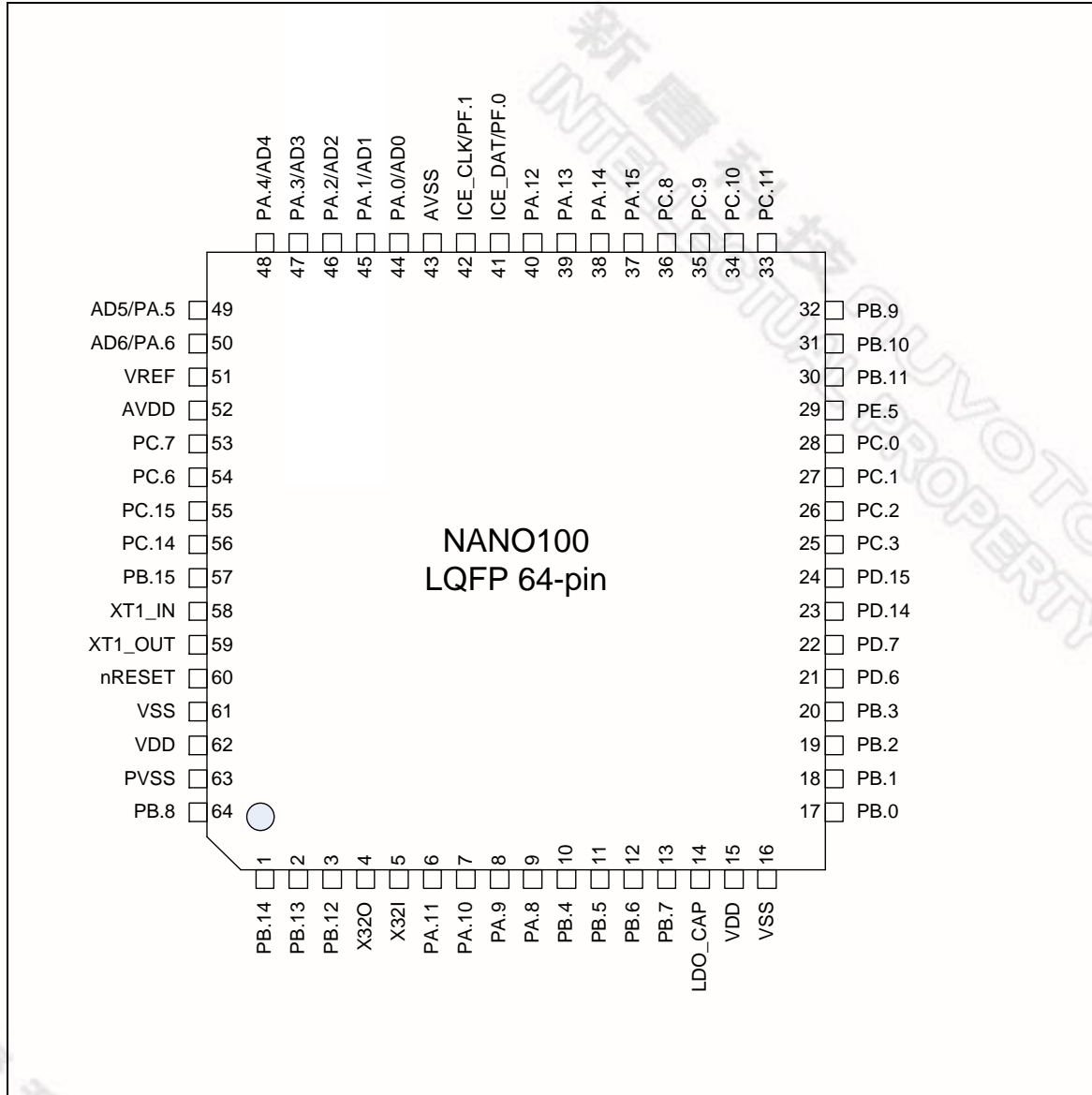


Figure 3-3 NuMicro™ Nano100 LQFP 64-pin Diagram

3.3.1.3 NuMicro™ Nano100 LQFP 48-pin

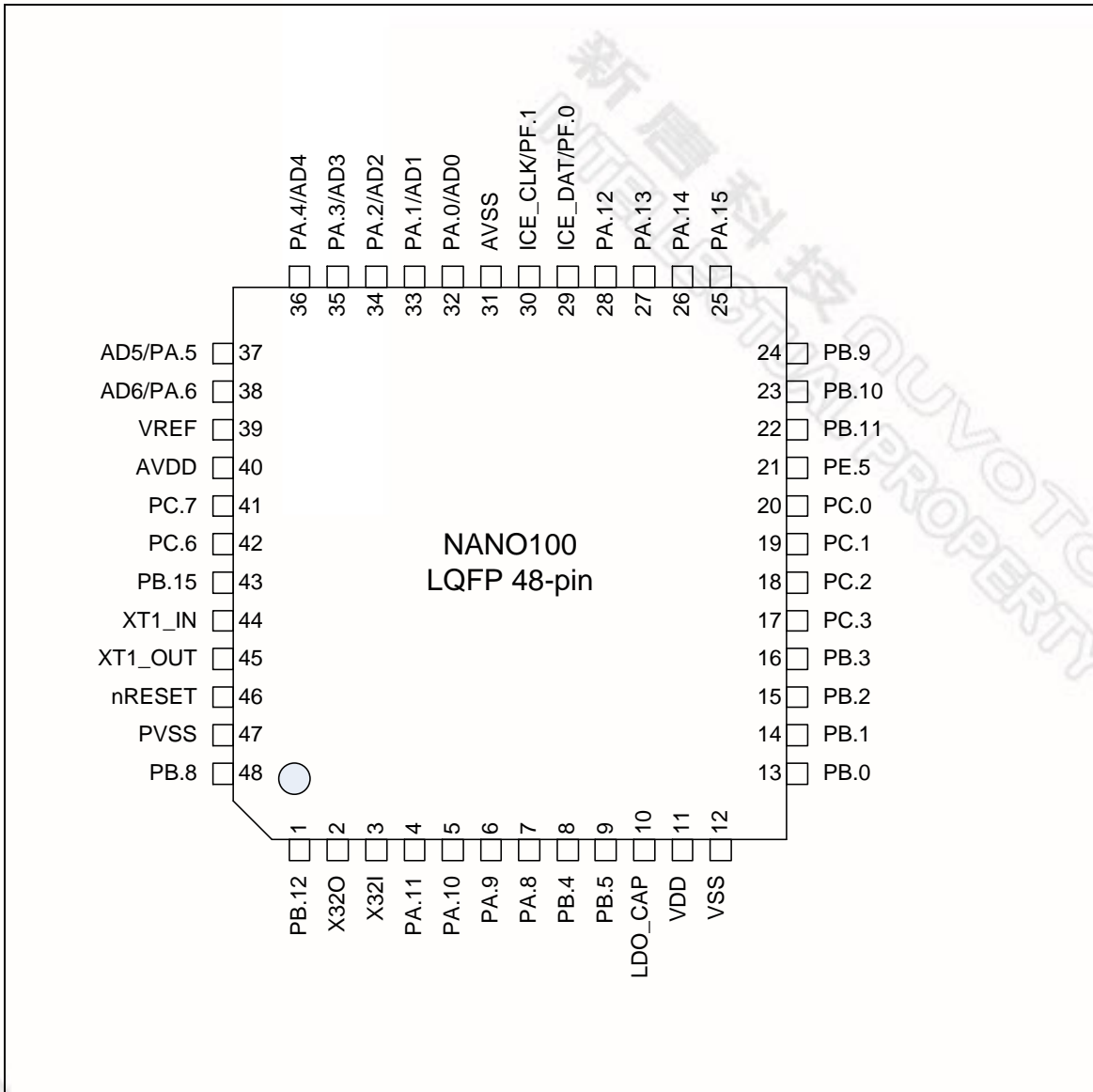


Figure 3-4 NuMicro™ Nano100 LQFP 48-pin Diagram

3.3.2 NuMicro™ Nano110 Pin Diagrams

3.3.2.1 NuMicro™ Nano110 LQFP 128-pin

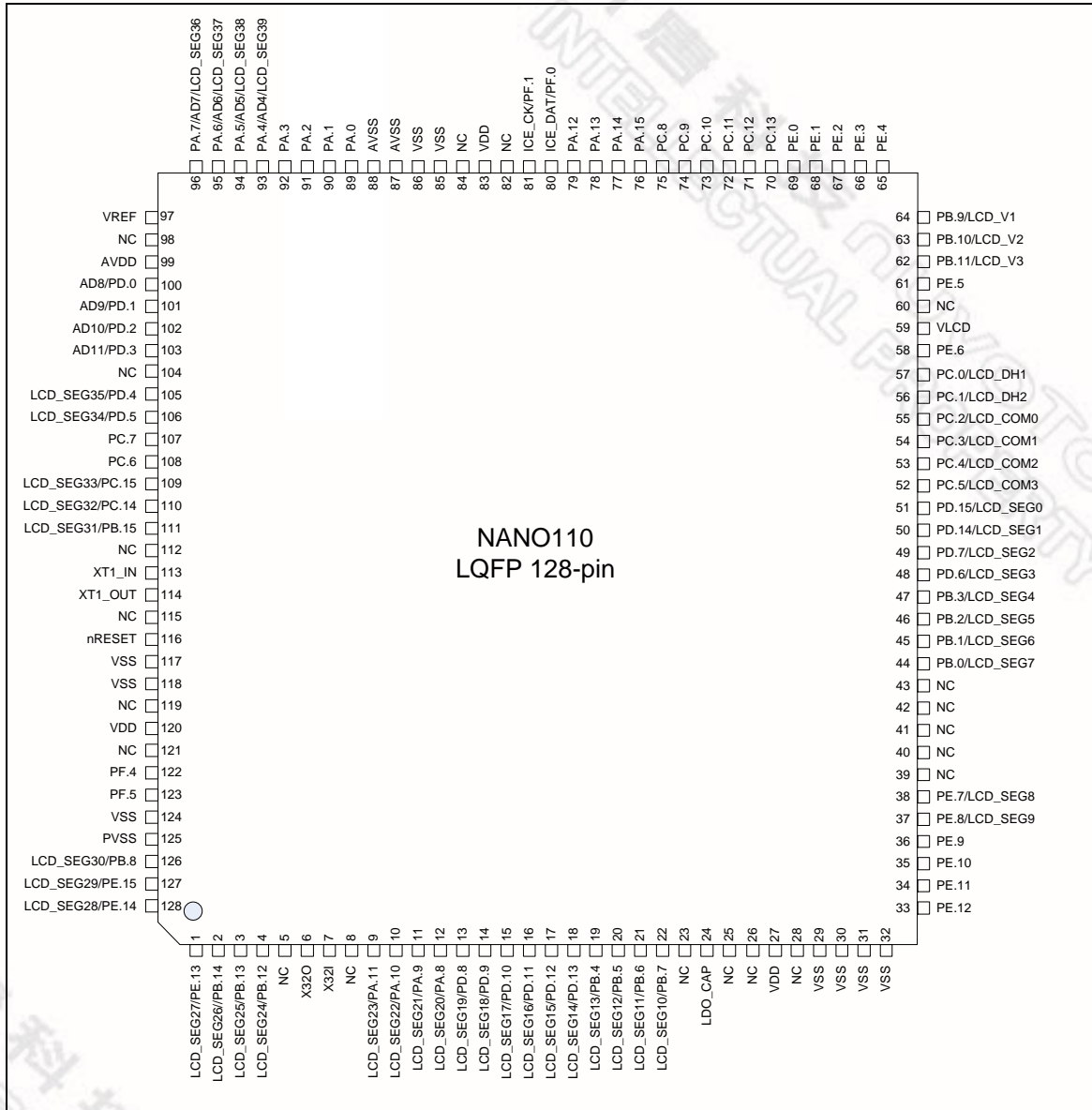


Figure 3-5 NuMicro™ Nano110 LQFP 128-pin Diagram

3.3.2.2 NuMicro™ Nano110 LQFP 64-pin

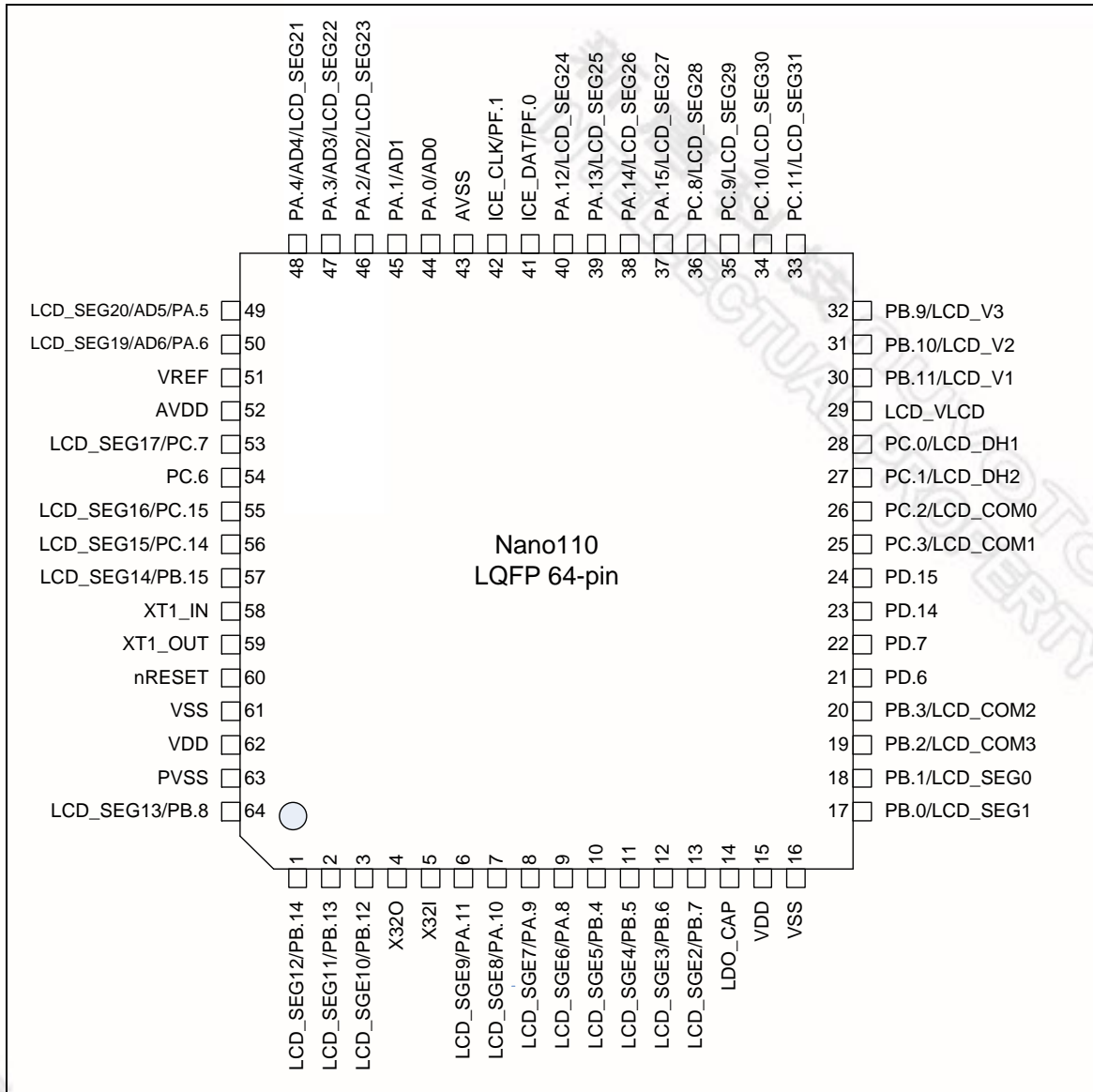


Figure 3-6 NuMicro™ Nano110 LQFP 64-pin Diagram

3.3.3 NuMicro™ Nano120 Pin Diagrams

3.3.3.1 NuMicro™ Nano120 LQFP 128-pin

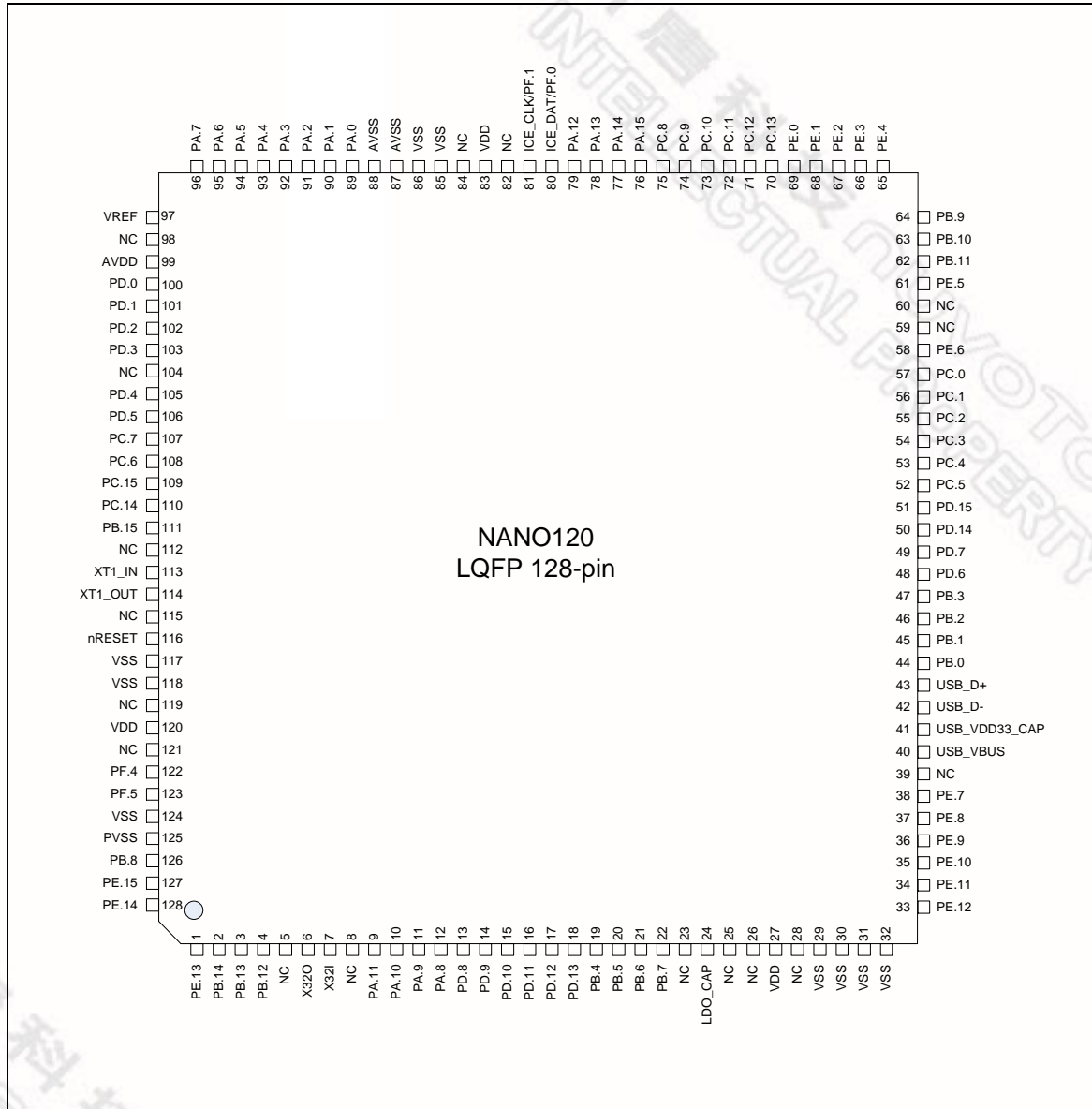


Figure 3-7 NuMicro™ Nano120 LQFP 128-pin Diagram

3.3.3.2 NuMicro™ Nano120 LQFP 64-pin

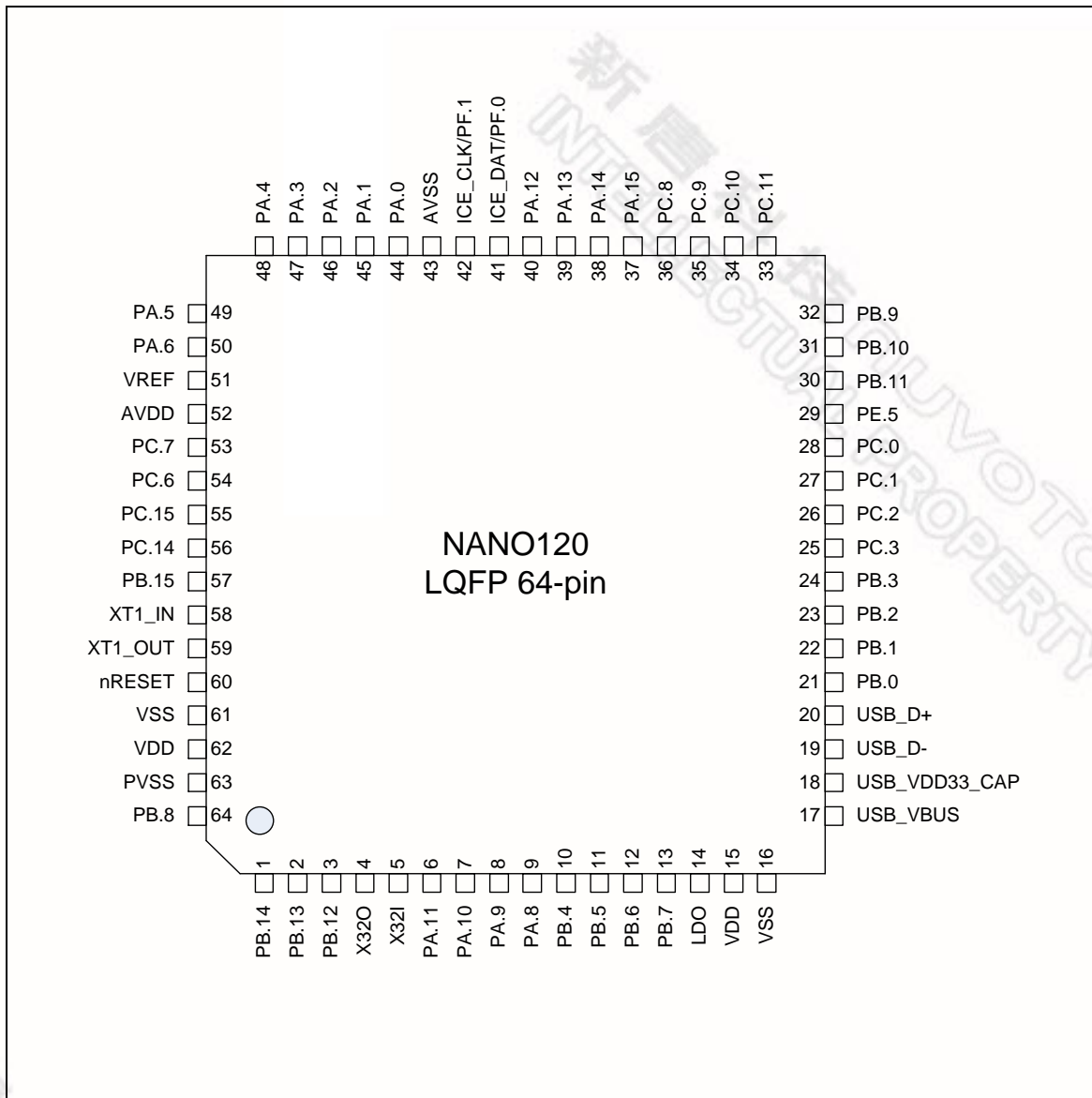


Figure 3-8 NuMicro™ Nano120 LQFP 64-pin Diagram

3.3.3.3 NuMicro™ Nano120 LQFP 48-pin

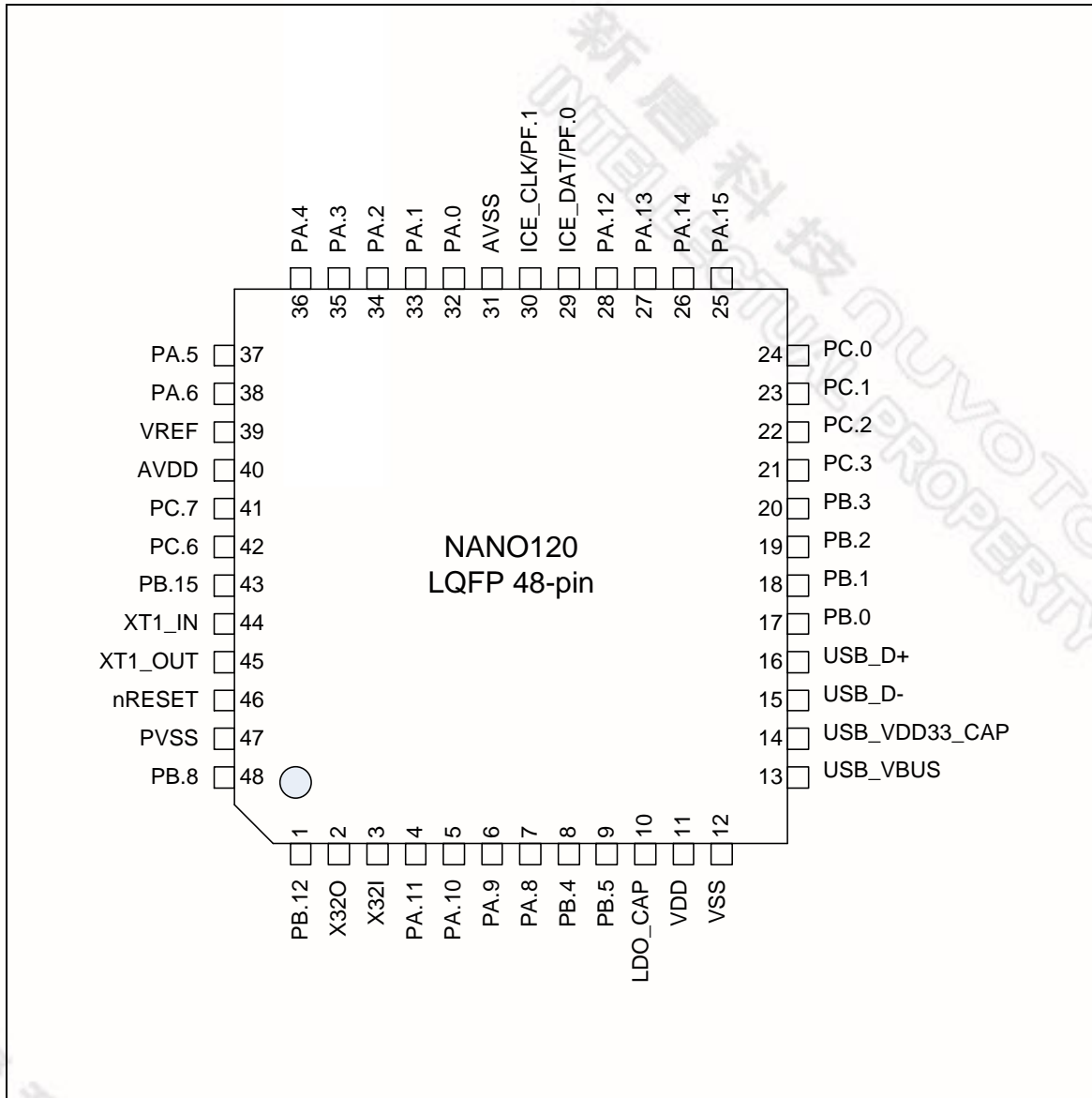


Figure 3-9 NuMicro™ Nano120 LQFP 48-pin Diagram

3.3.4 NuMicro™ Nano130 Pin Diagrams

3.3.4.1 NuMicro™ Nano130 LQFP 128-pin

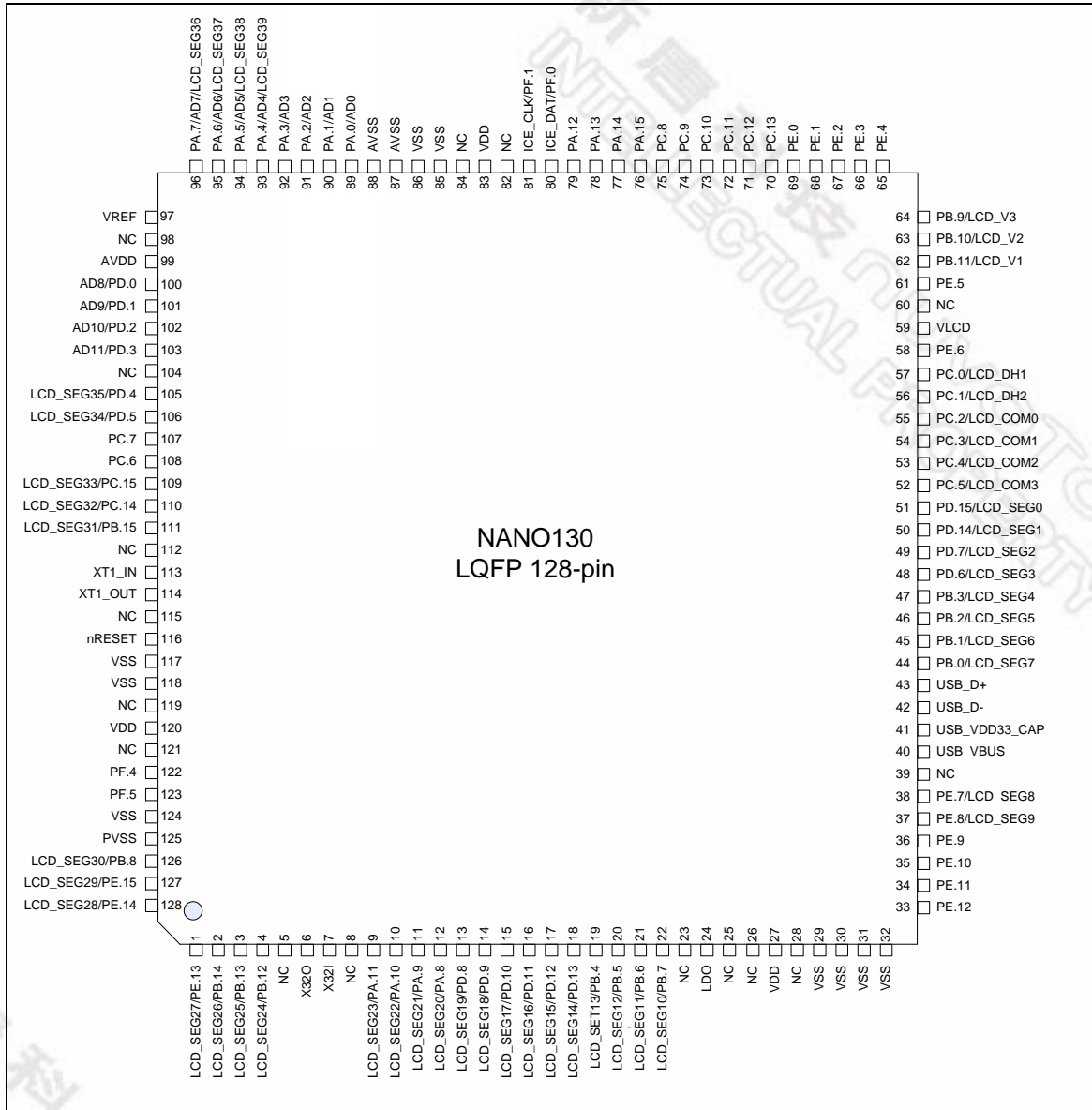


Figure 3-10 NuMicro™ Nano130 LQFP 128-pin Diagram



3.3.4.2 NuMicro™ Nano130 LQFP 64-pin

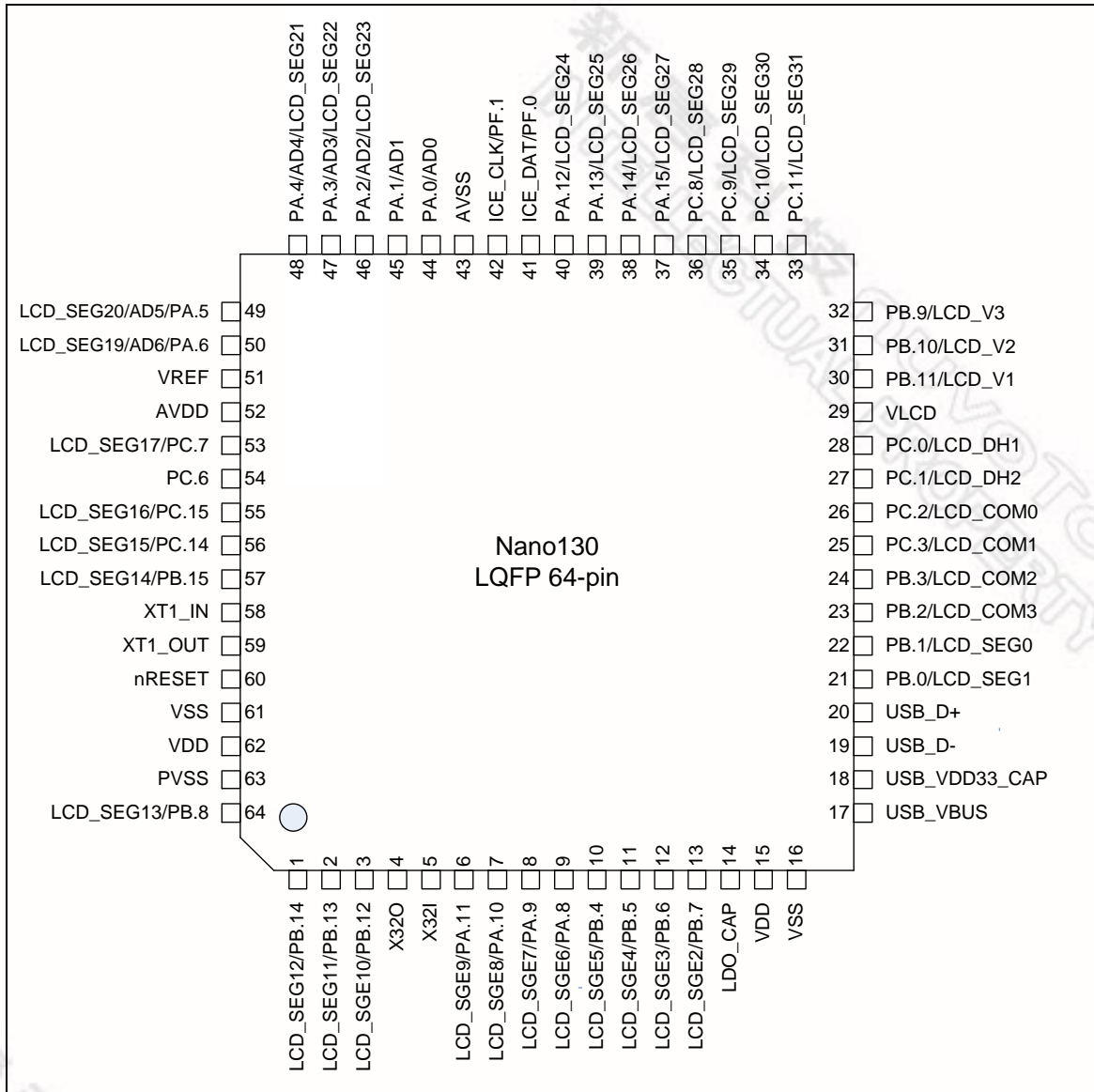


Figure 3-11 NuMicro™ Nano130 LQFP 64-pin Diagram

4 BLOCK DIAGRAM

4.1 Nano100 Block Diagram

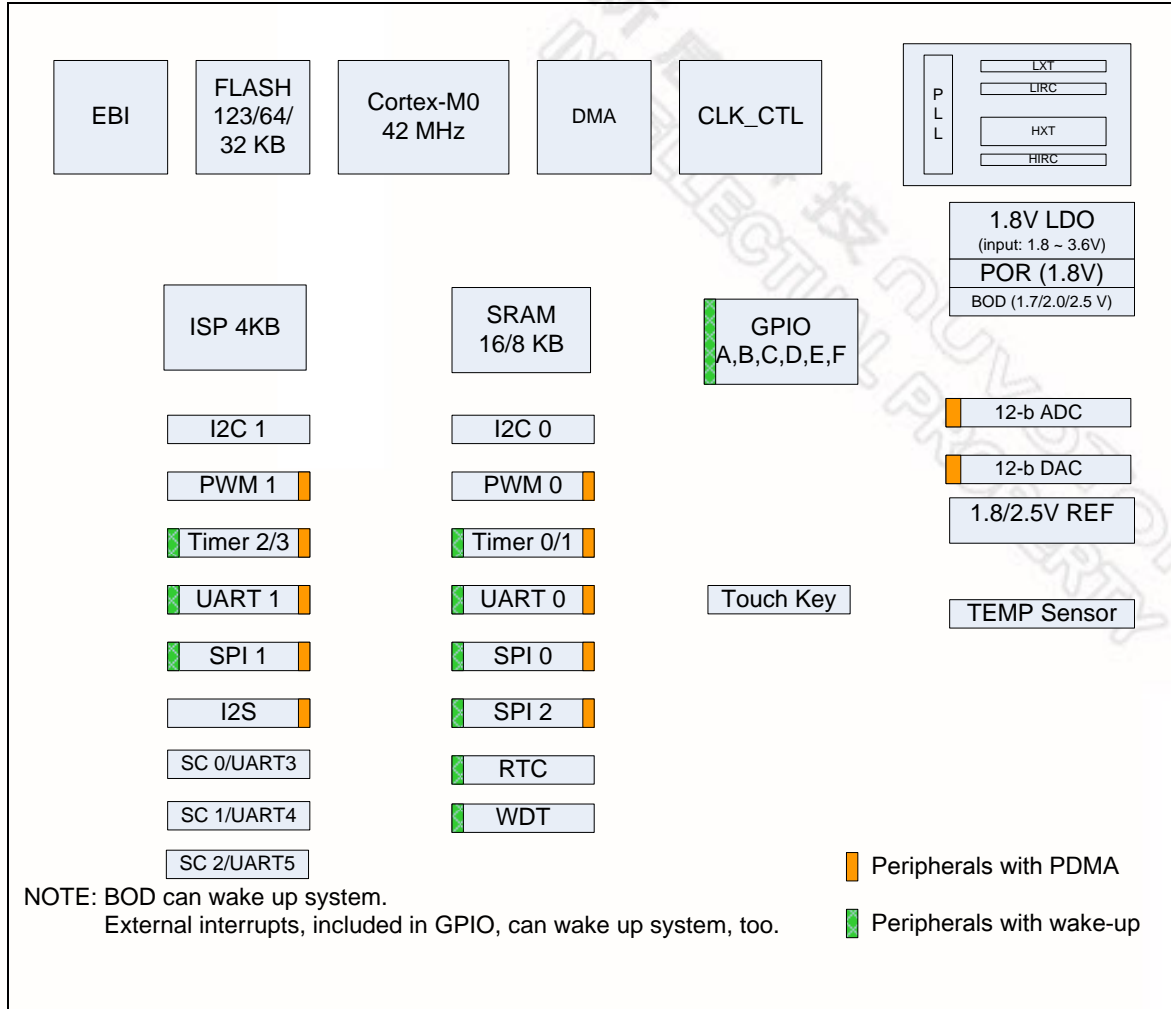


Figure 4-1 NuMicro™ Nano100 Block Diagram

4.2 Nano110 Block Diagram

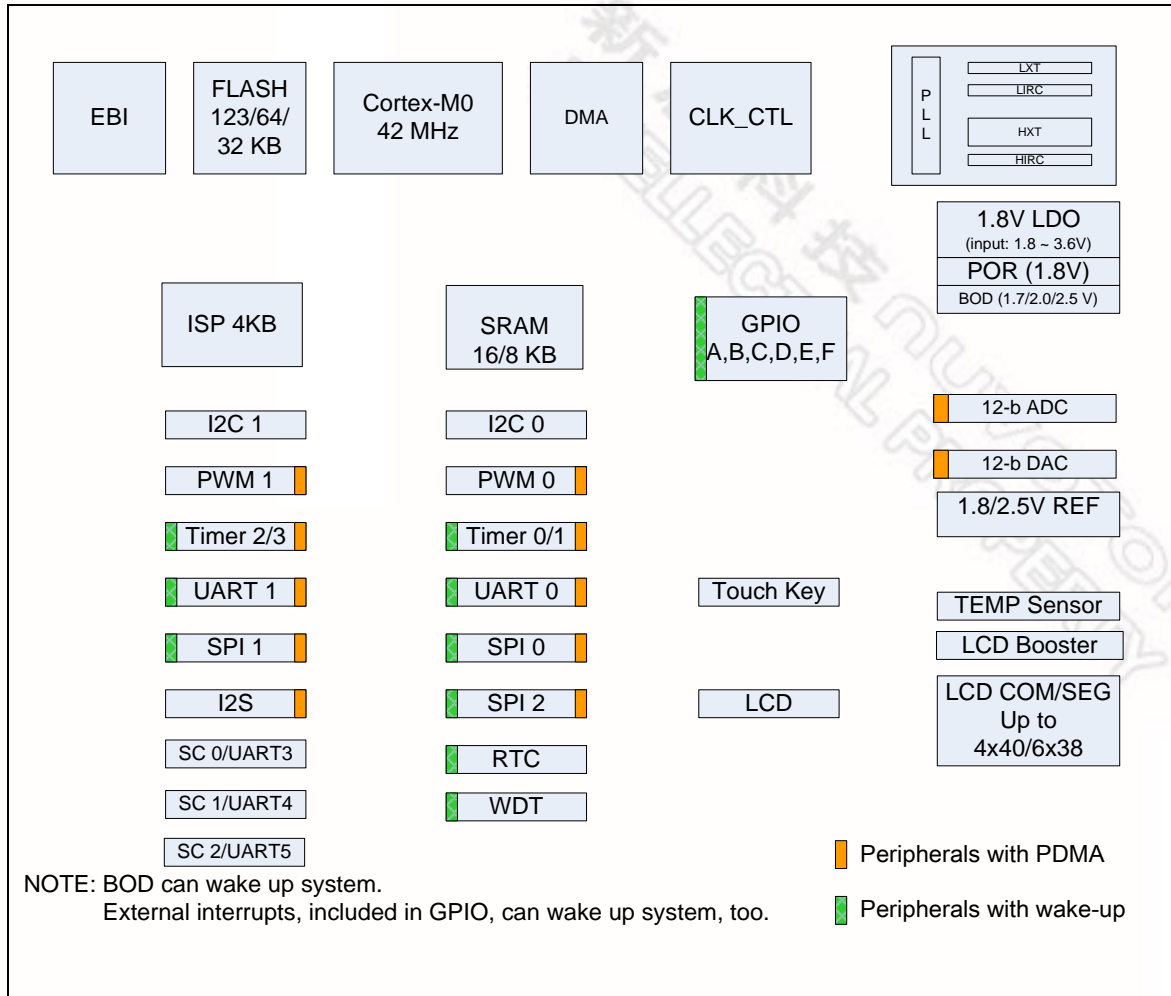


Figure 4-2 NuMicro™ Nano110 Block Diagram

4.3 Nano120 Block Diagram

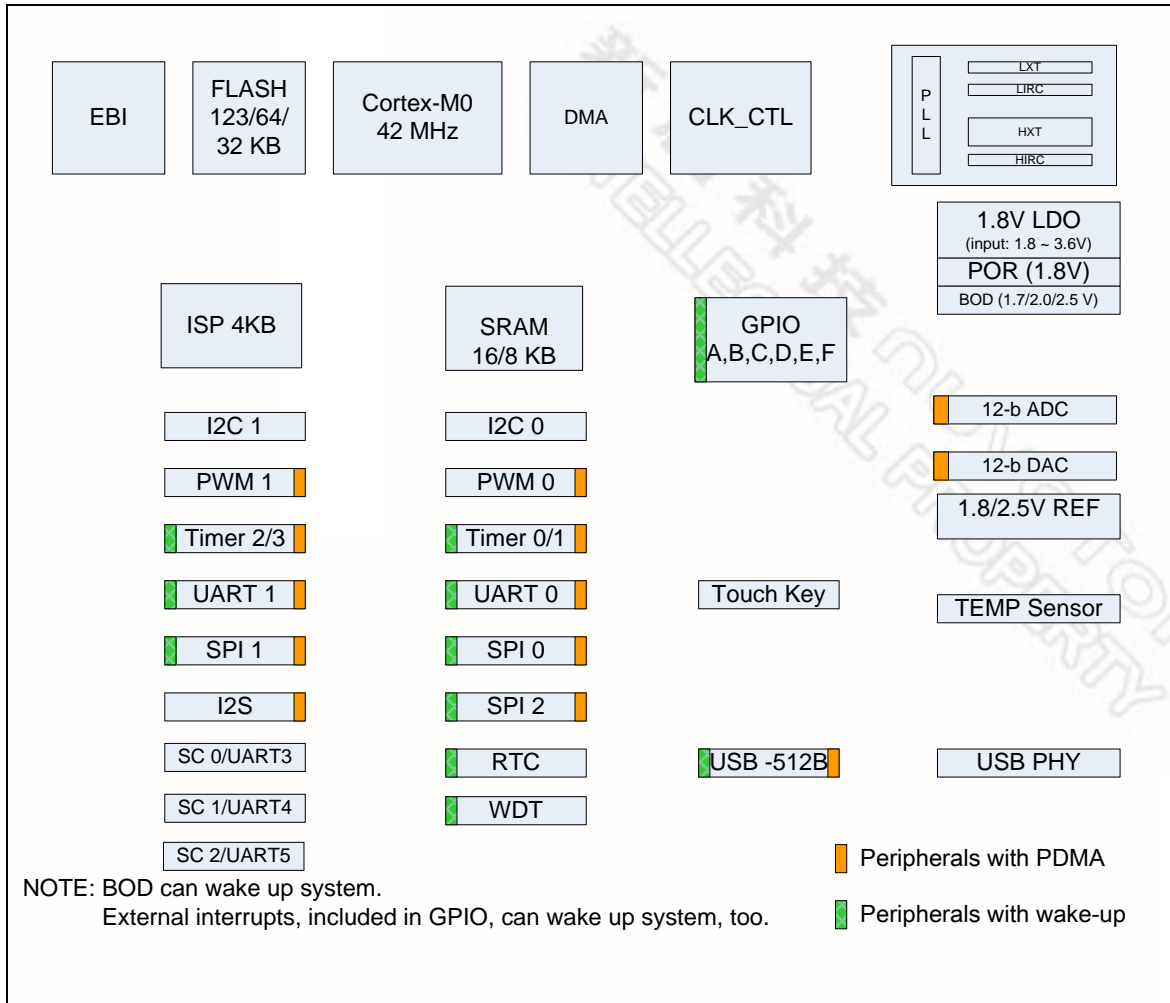


Figure 4-3 NuMicro™ Nano120 Block Diagram

4.4 Nano130 Block Diagram

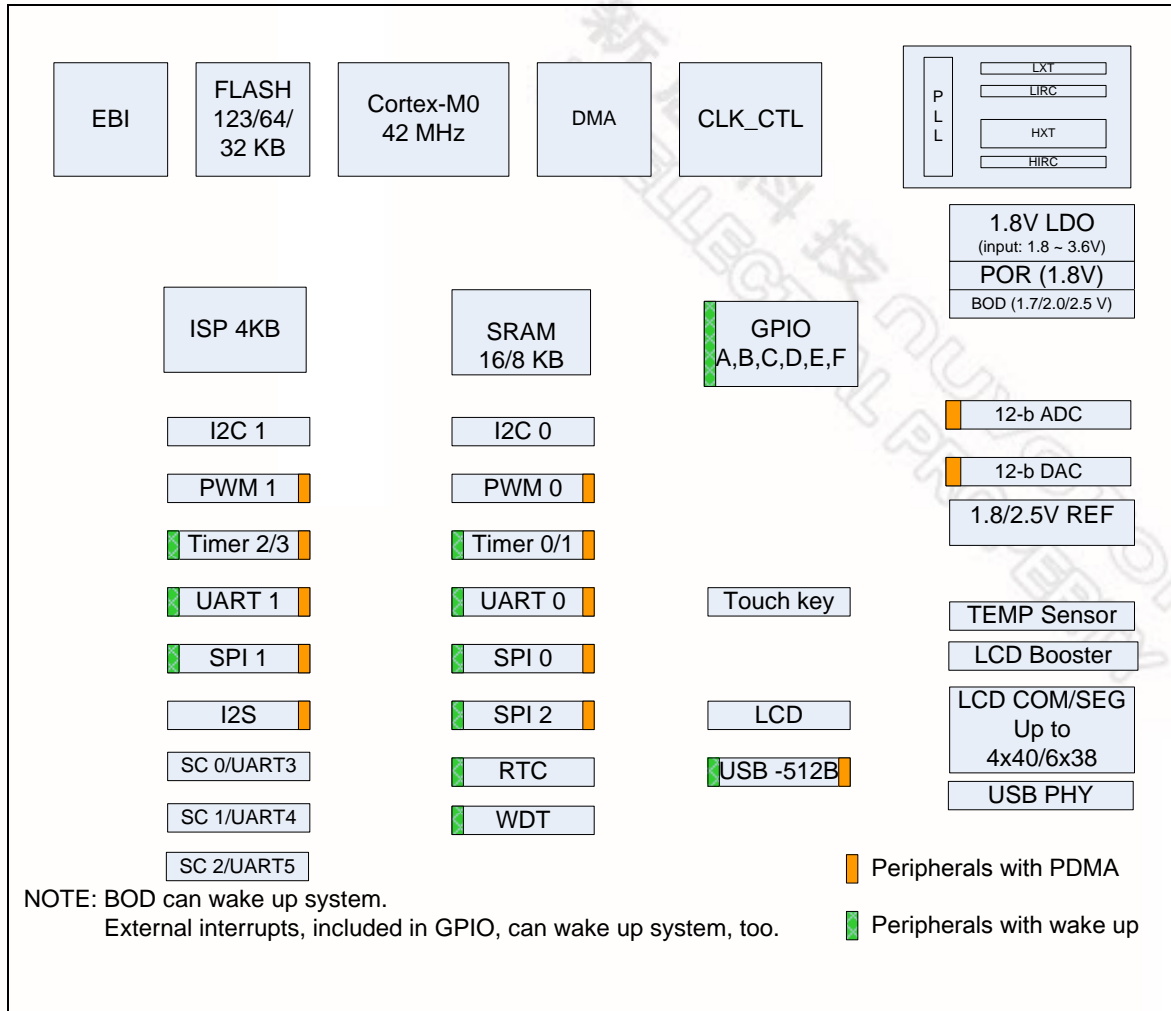
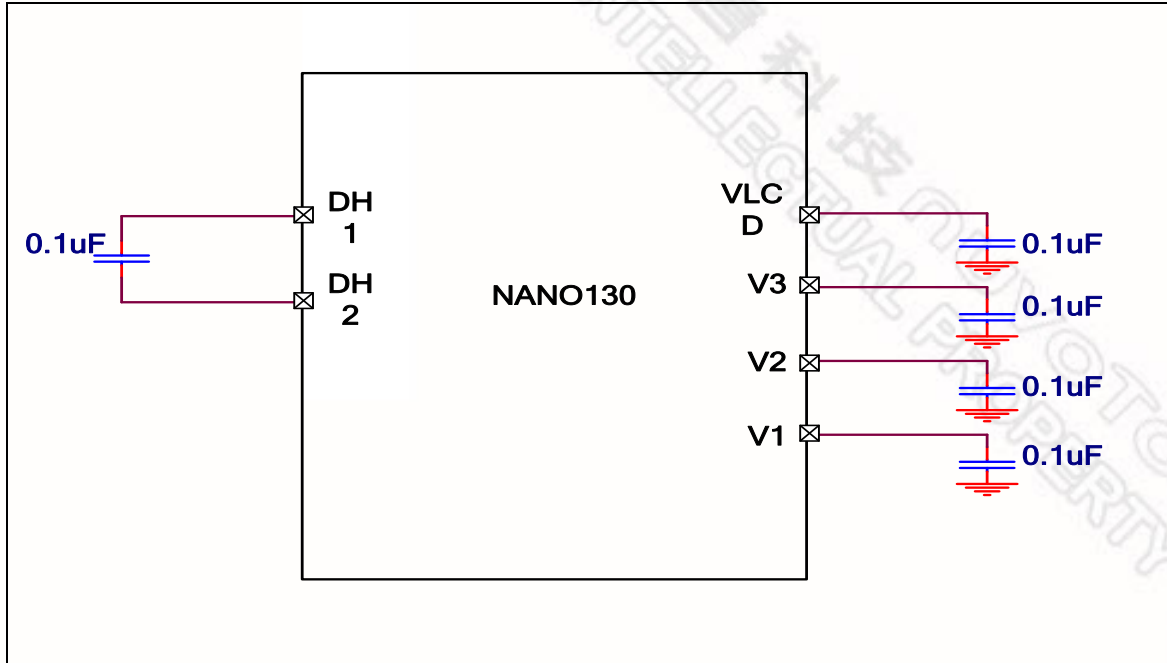


Figure 4-4 NuMicro™ Nano130 Block Diagram

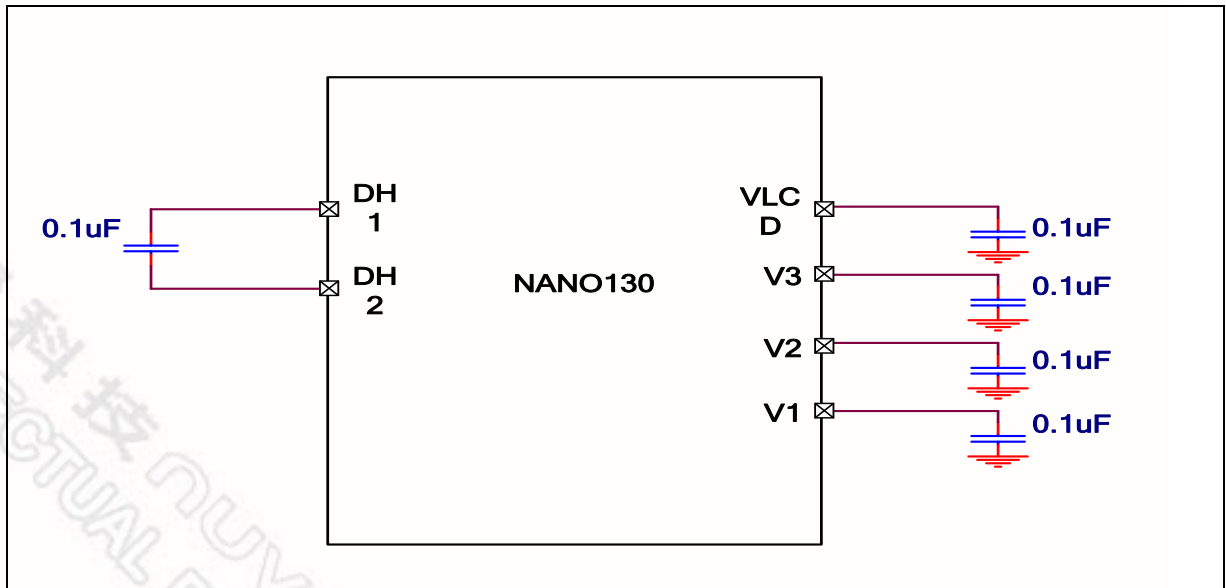
5 APPLICATION CIRCUIT

5.1 LCD Charge Pump

5.1.1 C-type 1/3 Bias



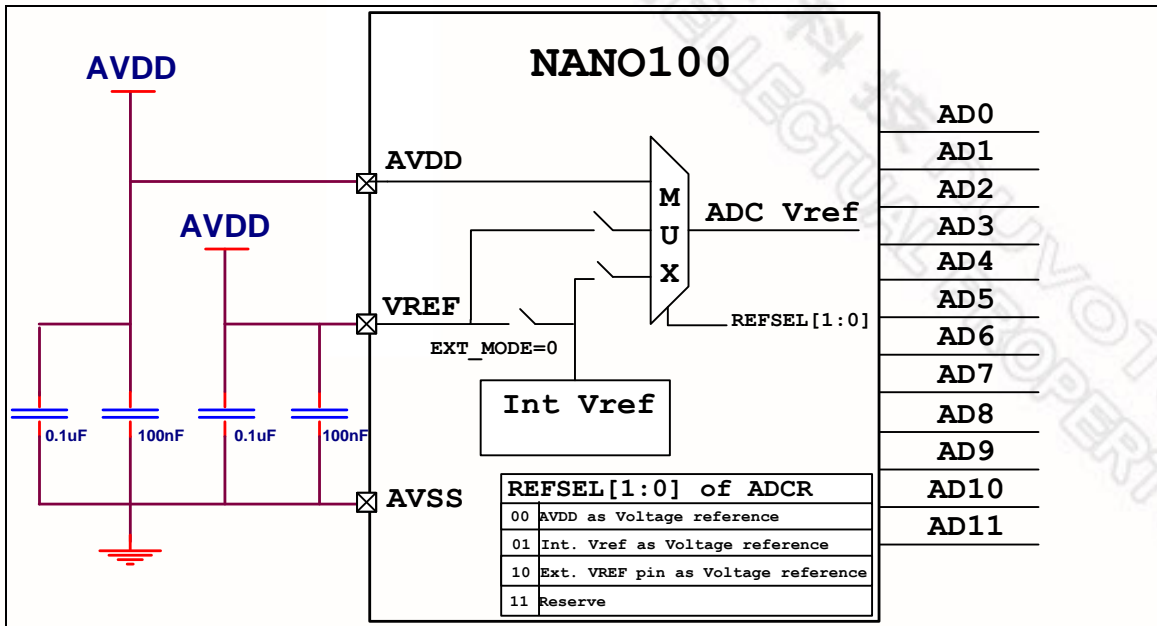
5.1.2 C-type 1/2 Bias



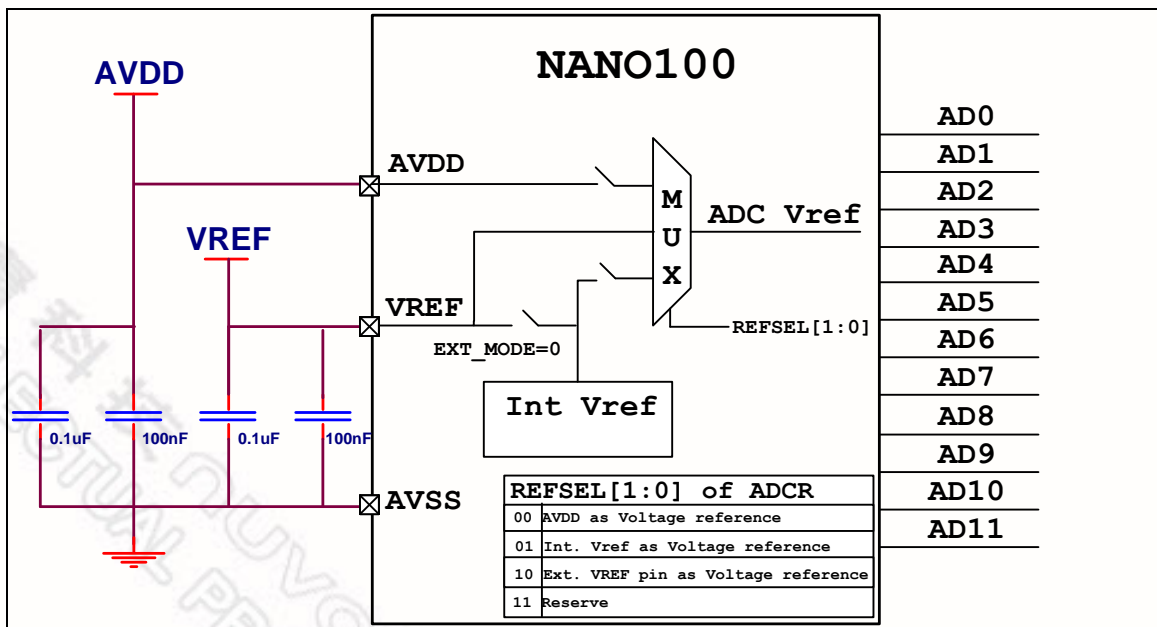
5.2 ADC Application Circuit

5.2.1 Voltage Reference Source

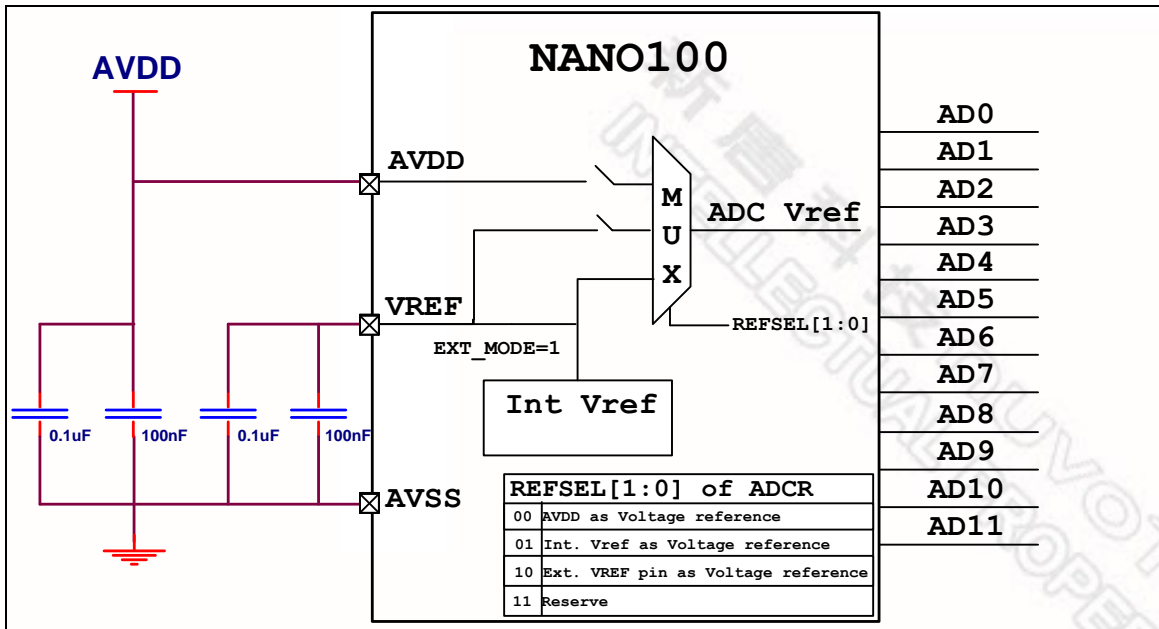
5.2.1.1 AVDD



5.2.1.2 Vref Pin



5.2.1.3 Int Vref

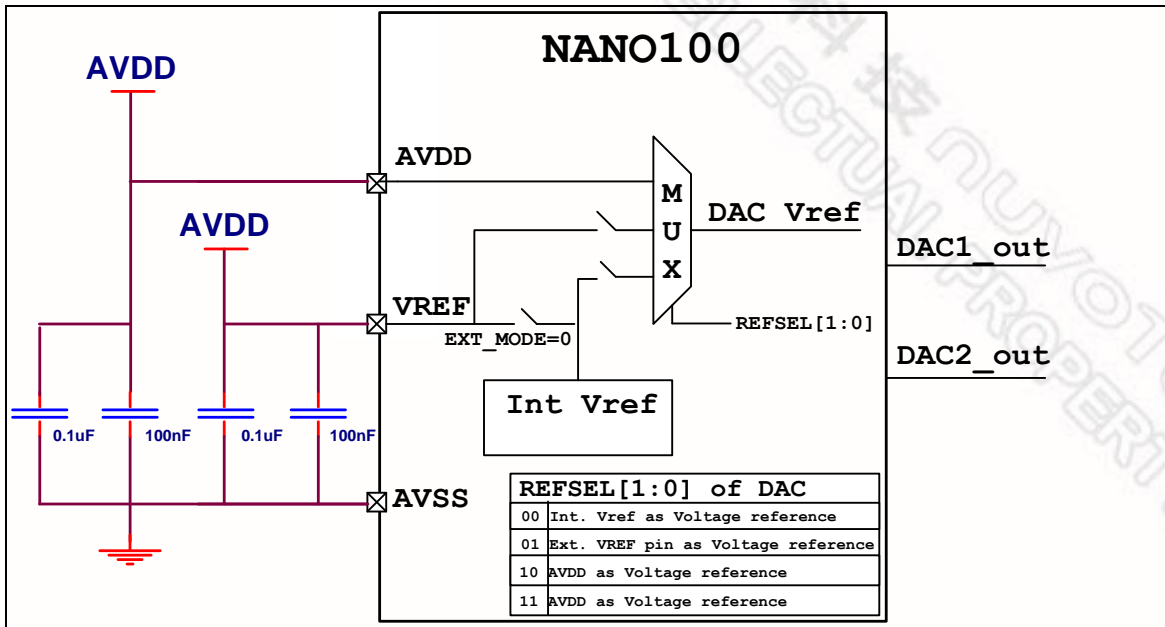


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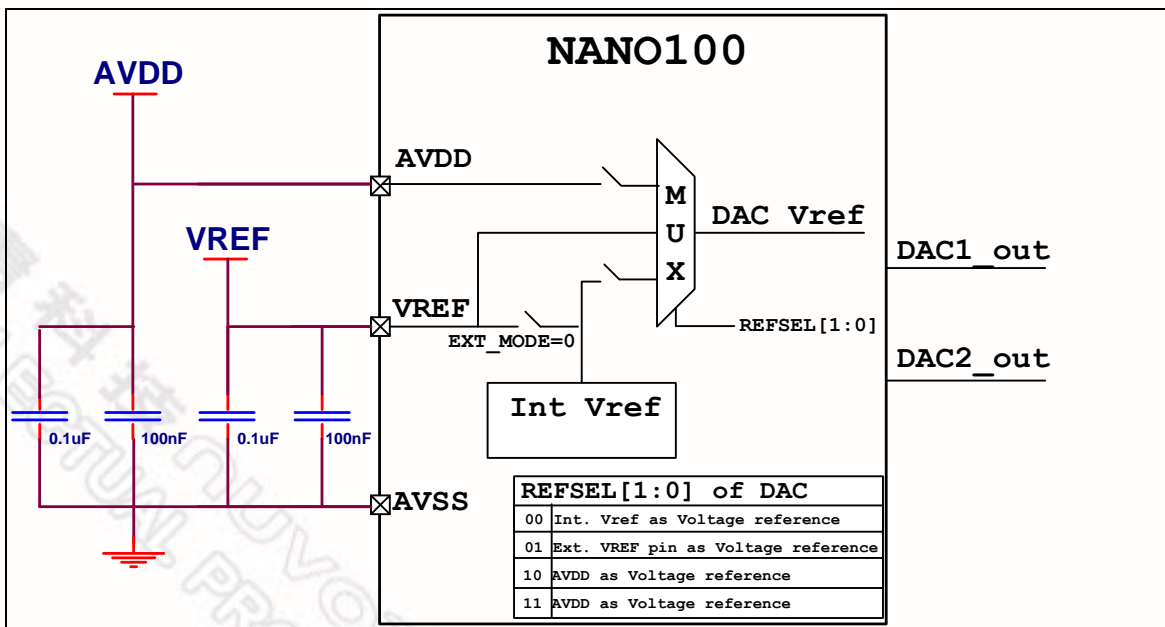
5.3 DAC Application Circuit

5.3.1 Voltage Reference Source

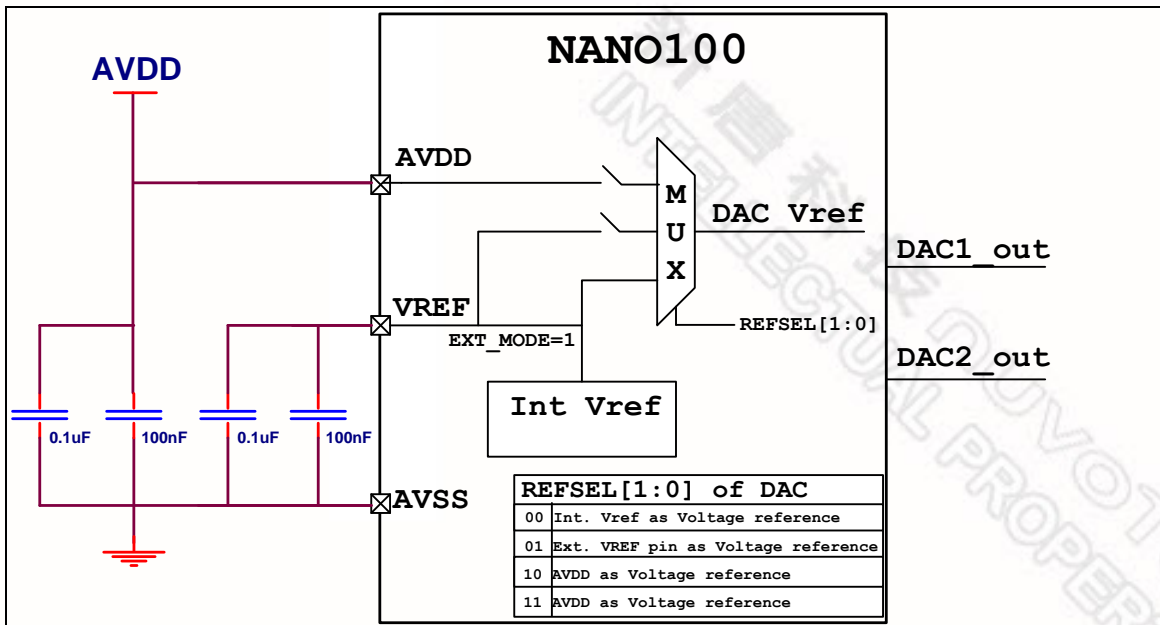
5.3.1.1 AVDD



5.3.1.2 Vref Pin

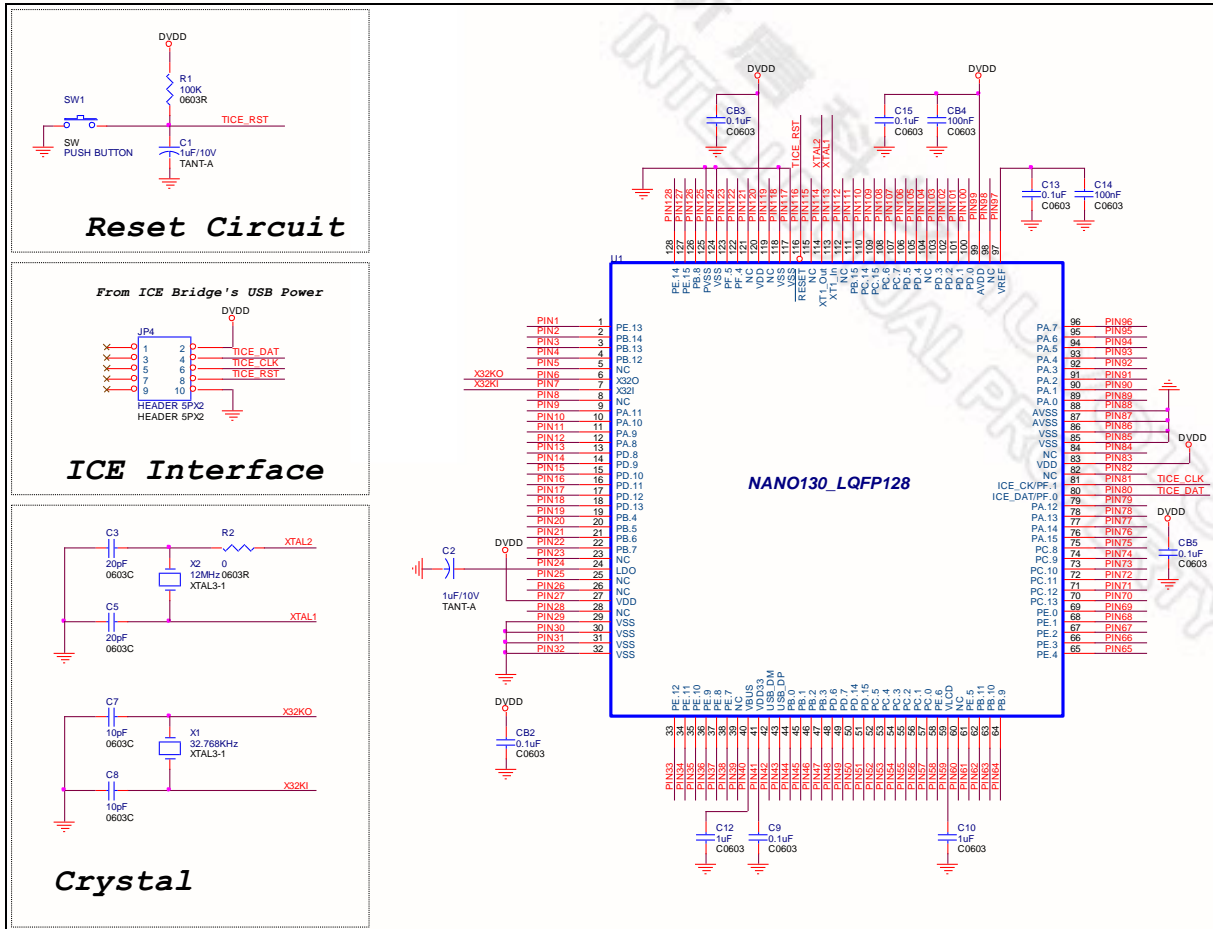


5.3.1.3 Int Vref





5.4 Whole Chip Application Circuit



6 POWER COMSUMPTION

Nano100 (B) series 128 KB Flash 16 KB RAM	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12 MHz Crystal Oscillator Disable all peripheral	3.3V	12MHz	2.41mA 200uA/MHz
		1.8V	12MHz	N/A
	Idle Mode: CPU stop Clock = 12MHz Crystal Oscillator Disable all peripheral	3.3V	12MHz	900uA 75uA/MHz
		1.8V	12MHz	N/A
	RTC + LCD Mode: (RAM retention) (Power down with 32K and LCD enabled) CPU stop Clock = 32.768 kHz Crystal Oscillator Disable all peripheral except RTC and LCD circuit Without panel loading	3.3V	-	10uA
		1.8V	-	-
	RTC Mode: (RAM retention) (Power down with 32K enabled) CPU stop Clock = 32.768 kHz Crystal Oscillator Disable all peripheral except RTC circuit	3.3V	-	2.5uA
		1.8V	-	N/A
	Power-down Mode: (RAM retention) CPU and all clocks stop	3.3V	-	1uA
		1.8V	-	0.8uA
	Wake-Up from Power-down Mode	3.3V	7us	

Note: Wake-up time: 7us from wake-up event to first CPU core valid clock; 10us from interrupt event to interrupt service routine first instruction.



7 ELECTRICAL CHARACTERISTIC

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	$V_{DD}-V_{SS}$	-0.3	+4.0	V
Input Voltage on 5V Tolerance Pin	V_{IN}	$V_{SS}-0.3$	$V_{DD}+3.7$	V
Input Voltage on Any Other Pin without 5V Tolerance Pin	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+85	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into VDD		-	150	mA
Maximum Current out of VSS		-	150	mA
Maximum Current sunk by a I/O Pin		-	25	mA
Maximum Current Sourced by a I/O Pin		-	25	mA
Maximum Current Sunk by Total I/O Pins		-	100	mA
Maximum Current Sourced by Total I/O Pins		-	100	mA

7.2 Nano100/Nano110/Nano120/Nano130 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 32 MHz unless otherwise specified.)

PARAMETER		SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V _{DD}	1.8	-	3.6	V	V _{DD} = 1.8V up to 32 MHz
Power Ground	V _{SS} AV _{SS}	-0.3	-		V	
LDO Output Voltage	V _{LDO1}	1.62	1.8	1.98	V	MCU operating in Run or Idle mode
	V _{LDO2}	1.49	1.66	1.83	V	MCU operating in Power-down mode
Analog Operating Voltage	AV _{DD}		V _{DD}		V	
Operating Current Run Mode at XTAL 12MHz, HCLK = 32 MHz	I _{DD1}		19.5		mA	V _{DD} = 3.6V at 32 MHz, all IP and PLL enabled
	I _{DD2}		10		mA	V _{DD} = 3.6V at 32 MHz all IP disabled and PLL enabled
	I _{DD3}		15.5		mA	V _{DD} = 1.8V at 32 MHz all IP and PLL enabled
	I _{DD4}		9		mA	V _{DD} = 1.8V at 32 MHz all IP disabled and PLL enabled
Operating Current Run Mode at XTAL 12MHz, HCLK = 12MHz	I _{DD5}		6		mA	V _{DD} = 3.6V at 12 MHz, all IP enabled and PLL disabled
	I _{DD6}		2.5		mA	V _{DD} = 3.6V at 12 MHz, all IP and PLL disabled
	I _{DD7}		5.5		mA	V _{DD} = 1.8V at 12 MHz, all IP enabled and PLL disabled
	I _{DD8}		2.4		mA	V _{DD} = 1.8V at 12 MHz, all IP and PLL disabled
Operating Current Run Mode at IRC 12MHz, HCLK = 12MHz	I _{DD9}		6.7		mA	V _{DD} = 3.6V at 12MHz, all IP enabled and PLL disabled
	I _{DD10}		2.9		mA	V _{DD} = 3.6V at 12 MHz, all IP and PLL disabled



PARAMETER	SPECIFICATIONS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNIT	
	I _{DD11}		6.4	mA	V _{DD} = 1.8V at 12 MHz, all IP enabled and PLL disabled
	I _{DD12}		2.8	mA	V _{DD} = 1.8V at 12 MHz, all IP and PLL disabled
Operating Current Run Mode at XTAL 4MHz, HCLK = 4MHz	I _{DD13}		2.3	mA	V _{DD} = 3.6V at 4 MHz, all IP enabled and PLL disabled
	I _{DD14}		1.2	mA	V _{DD} = 3.6V at 4 MHz, all IP and PLL disabled
	I _{DD15}		2.2	mA	V _{DD} = 1.8V at 4 MHz, all IP enabled and PLL disabled
	I _{DD16}		1.1	mA	V _{DD} = 1.8V at 4 MHz, all IP and PLL disabled
Operating Current Run Mode at XTAL 32.768 kHz, HCLK = 32.768 kHz	I _{DD17}		90	uA	V _{DD} = 3.6V at 32.768 kHz all IP enabled and PLL disabled,
	I _{DD18}		80	uA	V _{DD} = 3.6V at 32.768 kHz all IP and PLL disabled
	I _{DD19}		75	uA	V _{DD} = 1.8V at 32.768 kHz all IP enabled and PLL disabled
	I _{DD20}		72	uA	V _{DD} = 1.8V at 32.768 kHz all IP and PLL disabled
Operating Current Run Mode at IRC 10kHz, HCLK = 10kHz	I _{DD21}		80	uA	V _{DD} = 3.6V at 10 kHz all IP enabled and PLL disabled
	I _{DD22}		75	uA	V _{DD} = 3.6V at 10 kHz all IP and PLL disabled
	I _{DD23}		67	uA	V _{DD} = 1.8V at 10 kHz all IP enabled and PLL disabled
	I _{DD24}		65	uA	V _{DD} = 1.8V at 10 kHz all IP and PLL disabled
Operating Current Idle Mode at XTAL 12 MHz, HCLK = 32 MHz	I _{IDLE1}		14	mA	V _{DD} = 3.6V at 32 MHz all IP and PLL enabled,
	I _{IDLE2}		4.5	mA	V _{DD} =3.6V at 32 MHz all IP disabled and PLL enabled

PARAMETER		SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I _{IDLE3}		11.7		mA	V _{DD} = 1.8V at 32MHz all IP and PLL enabled
	I _{IDLE4}		4.3		mA	V _{DD} = 1.8V at 32 MHz all IP disabled and PLL enabled
Operating Current Idle Mode at XTAL 12MHz, HCLK = 12MHz	I _{IDLE5}		3.6		mA	V _{DD} = 3.6V at 12 MHz, all IP enabled and PLL disabled
	I _{IDLE6}		0.8		mA	V _{DD} = 3.6V at 12 MHz, all IP and PLL disabled
	I _{IDLE7}		3.5		mA	V _{DD} = 1.8V at 12 MHz, all IP enabled and PLL disabled
	I _{IDLE8}		0.75		mA	V _{DD} = 1.8V at 12 MHz, all IP and PLL disabled
Operating Current Idle Mode at IRC 12MHz, HCLK = 12MHz	I _{IDLE9}		4.7		mA	V _{DD} = 3.6V at 12 MHz, all IP enabled and PLL disabled
	I _{IDLE10}		0.9		mA	V _{DD} = 3.6V at 12 MHz, all IP and PLL disabled
	I _{IDLE11}		4.6		mA	V _{DD} = 1.8V at 12 MHz, all IP enabled and PLL disabled
	I _{IDLE12}		0.8		mA	V _{DD} = 1.8V at 12 MHz, all IP and PLL disabled
Operating Current Idle Mode at XTAL 4MHz, HCLK = 4MHz	I _{IDLE13}		1.72		mA	V _{DD} = 3.6V at 4 MHz, all IP enabled and PLL disabled
	I _{IDLE14}		0.6		mA	V _{DD} = 3.6V at 4 MHz, all IP and PLL disabled
	I _{IDLE15}		1.6		mA	V _{DD} = 1.8V at 4 MHz, all IP enabled and PLL disabled
	I _{IDLE16}		0.6		mA	V _{DD} = 1.8V at 4 MHz, all IP and PLL disabled
Operating Current Idle Mode at XTAL 32.768 kHz, HCLK = 32.768 kHz	I _{IDLE17}		85		uA	V _{DD} = 3.6V at 32.768 kHz all IP enabled and PLL disabled
	I _{IDLE18}		75		uA	V _{DD} = 3.6V at 32.768 kHz all IP and PLL disabled



PARAMETER		SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I _{IDLE19}		70		uA	V _{DD} = 1.8V at 32.768 kHz all IP enabled and PLL disabled
	I _{IDLE20}		65		uA	V _{DD} = 1.8V at 32.768 kHz all IP and PLL disabled
Operating Current Idle Mode at IRC 10 kHz, HCLK = 10 kHz	I _{IDLE21}		80		uA	V _{DD} = 3.6V at 10 kHz all IP enabled and PLL disabled
	I _{IDLE22}		75		uA	V _{DD} = 3.6V at 10 kHz all IP and PLL disabled
	I _{IDLE23}		65		uA	V _{DD} = 1.8V at 10 kHz all IP enabled and PLL disabled
	I _{IDLE24}		63		uA	V _{DD} = 1.8V at 10 kHz all IP and PLL disabled
Standby Current Power-down Mode	I _{PWD1}		1.5		μA	V _{DD} = 3.6V, RTC OFF, all clock stop With RAM Retention, IO no loading
	I _{PWD2}		0.8		μA	V _{DD} = 1.8V, RTC OFF, all clock stop With RAM Retention, IO no loading
	I _{PWD3}		3		μA	V _{DD} = 3.6V, RTC ON, all clock stop except 32.768 kHz With RAM Retention, IO no loading
	I _{PWD4}		2.0		μA	V _{DD} = 1.8V, RTC ON, all clock stop except 32.768 kHz With RAM Retention, IO no loading
Input Pull Up Resistor PA, PB, PC, PD, PE, PF	R _{IN}		40		KΩ	V _{DD} = 3.3V
			98		KΩ	V _{DD} = 1.8V
Input Leakage Current PA, PB, PC, PD, PE, PF	I _{LK}	-0.1	-	+0.1	μA	V _{DD} = 3.3V, 0 < V _{IN} < V _{DD}
Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V _{IL1}		-	0.4V _{DD}	V	
Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V _{IH1}	0.6V _{DD}		5.5	V	ADC and DAC shared pins without Input 5V tolerance.
Hysteresis voltage of PA~PF (Schmitt input)	V _{HY}		0.2V _{DD}		V	

PARAMETER		SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage XT1 ^[1,2]	V _{IL2}	0	-	0.4		V _{DD} = 3.3V
Input High Voltage XT1 ^[1,2]	V _{IH2}	1.5	-	V _{DD} +0.2	V	V _{DD} = 3.3V
Input Low Voltage X321 ^[1,2]	V _{IL4}	0	-	0.3	V	
Input High Voltage X321 ^[1,2]	V _{IH4}	1.5	-	1.98	V	
Negative going threshold (Schmitt input), /RESET	V _{ILS}	1.28	1.33	1.37	V	V _{DD} = 3.3V
Positive going threshold (Schmitt input), /RESET	V _{IHS}	1.75	1.98	2.25	V	V _{DD} = 3.3V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I _{SR21}	-10	-14	-	mA	V _{DD} = 3.3V, V _S = V _{DD} -0.7V
	I _{SR22}	-3	-5	-	mA	V _{DD} = 1.8V, V _S = V _{DD} -0.45V
Sink Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I _{SK1}	10	15	-	mA	V _{DD} = 3.3V, V _S = 0.7V
	I _{SK1}	3	6	-	mA	V _{DD} = 1.8V, V _S = 0.45V

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.
4. For ensuring power stability, a 4.7uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise

7.3 AC Electrical Characteristics

7.3.1 External Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t _{CHCX}	20	-		nS	
Clock Low Time	t _{CLCX}	20	-		nS	
Clock Rise Time	t _{CLCH}		-	10	nS	
Clock Fall Time	t _{CHCL}		-	10	nS	

The diagram shows a square wave signal with various timing parameters labeled: t_{CHCX} (clock high time), t_{CLCX} (clock low time), t_{CLCH} (clock rise time), t_{CHCL} (clock fall time), and t_{CLCL} (clock period).

7.3.2 External 4~24 MHz XTAL Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f _{HXTAL}	4	12	24	MHz	VDD = 1.8V ~ 3.6V
Temperature	T _{HXTAL}	-40	-	+85	°C	
Operating current	I _{HXTAL}		0.3		mA	VDD = 3.0V

7.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	Optional(Depend on crystal specification)		without

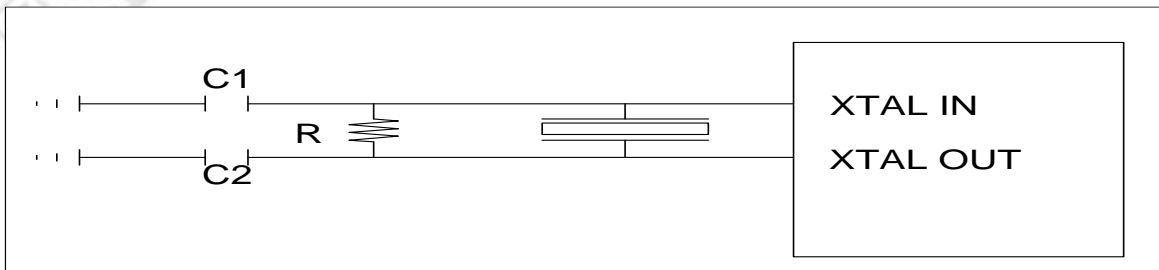


Figure 7-1 Typical Crystal Application Circuit

7.3.3 External 32.768 kHz Crystal

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f _{LXTAL}		32.768		kHz	V _{DD} = 1.8V ~ 3.6V
Temperature	T _{LXTAL}	-40	-	+85	°C	
Operating current	I _{HXTAL}		1.2		μA	V _{DD} = 3.0V

7.3.4 Internal 12 MHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage ^[1]	V _{HRC}		1.8		V	
Calibrated Internal Oscillator Frequency	F _{HRC}	11.88	12	12.12	MHz	25°C, V _{DD} = 3V
		11.76	12	12.24	MHz	-40°C~+85°C, V _{DD} = 1.8V~3.6V
		11.97	12	12.03	MHz	-40°C~+85°C, V _{DD} = 1.8V~3.6V Enable 32.768K crystal oscillator and set TRIM_SEL[1:0]="10"
Operating current	I _{HRC}		TBD		mA	

Note: Internal oscillator operation voltage comes from LDO.

7.3.5 Internal 10 kHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage ^[1]	V _{LRC}		1.8		V	
Center Frequency	F _{LRC}	7	10	13	kHz	25°C, V _{DD} = 3V
		5	10	15	kHz	-40°C~+85°C, V _{DD} = 1.8V~3.6V
Operating current	I _{LRC}		0.7		μA	V _{DD} = 3V

Note: Internal oscillator operation voltage comes from LDO.

7.4 Analog Characteristics

7.4.1 12-bit ADC

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV _{DD}	1.8		3.6	V	AV _{DD} = V _{DD}
Operating current	I _{ADC}		TBD		mA	AV _{DD} = V _{DD} = 3.0V
Resolution	R _{ADC}			12	Bit	
Reference voltage	V _{REF}	1.8		AV _{DD}	V	
Reference input current (Avg.)	I _{REF}		TBD		μA	
ADC input voltage	V _{IN}	0		V _{REF}	V	
Conversion time	T _{CONV}	0.5			μS	
Sampling Rate	F _{SPS}			2M	Hz	V _{DD} = 3V
Integral Non-Linearity Error	INL		±1	±2	LSB	V _{REF} is external Vref pin
Differential Non-Linearity	DNL		±0.8	-1~+1.5	LSB	V _{REF} is external Vref pin
Gain error	E _G		-	±2	LSB	V _{REF} is external Vref pin
Offset error	E _{OFFSET}		-	±3	LSB	V _{REF} is external Vref pin
Absolute error	E _{ABS}		-	±6	LSB	V _{REF} is external Vref pin
ADC Clock frequency	F _{ADC}	TBD		42	MHz	
Clock cycle	AD _{CYC}	20			Cycle	
Internal Capacitance	C _{IN}	-	5	-	pF	
Monotonic	-	Guaranteed			-	

7.4.2 Brown-out Detector

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V _{BOD}	1.8		3.6	V	
BOD17 Quiescent current	I _{BOD17}		TBD		μA	AV _{DD} = 3.0V, BOD17 enabled
BOD20 Quiescent current	I _{BOD20}		TBD		μA	AV _{DD} = 3.0V, BOD20 enabled
BOD25 Quiescent current	I _{BOD25}		TBD		μA	AV _{DD} = 3.0V, BOD25 enabled
BOD17 detection level	V _{B17dt}	1.6	1.7	1.8	V	25°C
BOD20 detection level	V _{B20dt}	1.9	2.0	2.1	V	25°C
BOD25 detection level	V _{B25dt}	2.4	2.5	2.6	V	25°C

7.4.3 Power-on Reset

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Reset voltage	V _{POR}	-	1.6	-	V	
Quiescent current	I _{POR}	-	1	-	nA	LDO output > Reset voltage

7.4.4 Temperature Sensor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Detection Temperature	T _{DET}	-40		+125	°C	
Operating current	I _{TEMP}	-	5	-	μA	
Gain	V _{TG}	-	-1.73	-	mV/ °C	
Offset	V _{TO}	-	740	-	mV	Temperature at 0 °C

Note: Internal operation voltage comes from LDO.

7.4.5 12-bit DAC

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV _{DD}	2.0		3.6	V	AV _{DD} = V _{DD}
Operating current	IDAC		500		μA	AV _{DD} = V _{DD} = 3.0V
Resolution	R _{ADC}			12	Bit	
Reference voltage	V _{REF}	1.8		AV _{DD}	V	
Reference input current (Avg.)	I _{REF}		TBD		μA	
DAC output swin range	V _{OUT}	0.1 x V _{REF}	-	0.9 x V _{REF}	V	
Conversion Rate (code to adjacent code)	F _{SPS}			400	kHz	V _{DD} = 3V
Integral Non-Linearity Error	INL		±2	TBD	LSB	V _{REF} is external Vref pin Not include offset and gain error
Differential Non-Linearity	DNL		±1	TBD	LSB	V _{REF} is external Vref pin Not include offset and gain error
Gain error	E _G		-	TBD	LSB	
Offset error	E _{OFFSET}		-	TBD	LSB	

7.4.6 LCD

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V _{DD}	1.8	-	3.6	V	
VLCD voltage	V _{LCD34}	-	3.4	-	V	CPUMP_VOL_SET=111, no loading
Reset voltage	V _{LCD33}	-	3.3	-	V	CPUMP_VOL_SET=110, no loading
Reset voltage	V _{LCD32}	-	3.2	-	V	CPUMP_VOL_SET=101, no loading
Reset voltage	V _{LCD31}	-	3.1	-	V	CPUMP_VOL_SET=100, no loading
Reset voltage	V _{LCD30}	-	3.0	-	V	CPUMP_VOL_SET=011, no loading
Reset voltage	V _{LCD29}	-	2.9	-	V	CPUMP_VOL_SET=010, no loading
Reset voltage	V _{LCD28}	-	2.8	-	V	CPUMP_VOL_SET=001, no loading
Reset voltage	V _{LCD27}	-	2.7	-	V	CPUMP_VOL_SET=000, no loading
Operating current	I _{LCD}	-	10	-	μA	V _{DD} = 3V, frame rate = 32Hz Without loading

7.4.7 Touch Key (TK)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V _{DD}	1.8	-	3.6	V	
Operating current	I _{TK}	-	TBD	-	μA	V _{DD} = 3V
TK oscillator frequency	F _{TKOSC}	-	10	-	MHz	

7.4.8 Internal Voltage Reference

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV _{DD}	1.8	-	3.6	V	
1.8V voltage reference	V _{REF1}	-	1.8	-	V	AV _{DD} >= 2.0V
2.5V voltage reference	V _{REF2}	-	2.5	-	V	AV _{DD} >= 2.8V
Stable Time	T _{REFTAB}	-	1	-	ms	
Operating current	I _{VREF}	-	30	-	μA	AV _{DD} = 3V

7.4.9 USB PHY Specifications

7.4.9.1 USB PHY DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input high (driven)		2.0	-		V
V _{IL}	Input low			-	0.8	V
V _{DI}	Differential input sensitivity	PADP-PADM	0.2	-		V
V _{CM}	Differential common-mode range	Includes V _{DI} range	0.8	-	2.5	V
V _{SE}	Single-ended receiver threshold		0.8	-	2.0	V
	Receiver hysteresis			200		mV
V _{OL}	Output low (driven)		0	-	0.3	V
V _{OH}	Output high (driven)		2.8	-	3.6	V
V _{CRS}	Output signal cross voltage		1.3	-	2.0	V
R _{PU}	Pull-up resistor		1.425	-	1.575	kΩ
R _{PD}	Pull-down resistor		14.25	-	15.75	kΩ
V _{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0	-	3.6	V
Z _{DRV}	Driver output resistance	Steady state drive*		10		Ω
C _{IN}	Transceiver capacitance	Pin to GND		-	20	pF

*Driver output resistance doesn't include series resistor resistance.

7.4.9.2 USB PHY Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
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T_{FR}	Rise Time	$C_L=50p$	4	-	20	ns
T_{FF}	Fall Time	$C_L=50p$	4	-	20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90	-	111.11	%

7.4.9.3 USB PHY Power Dissipation

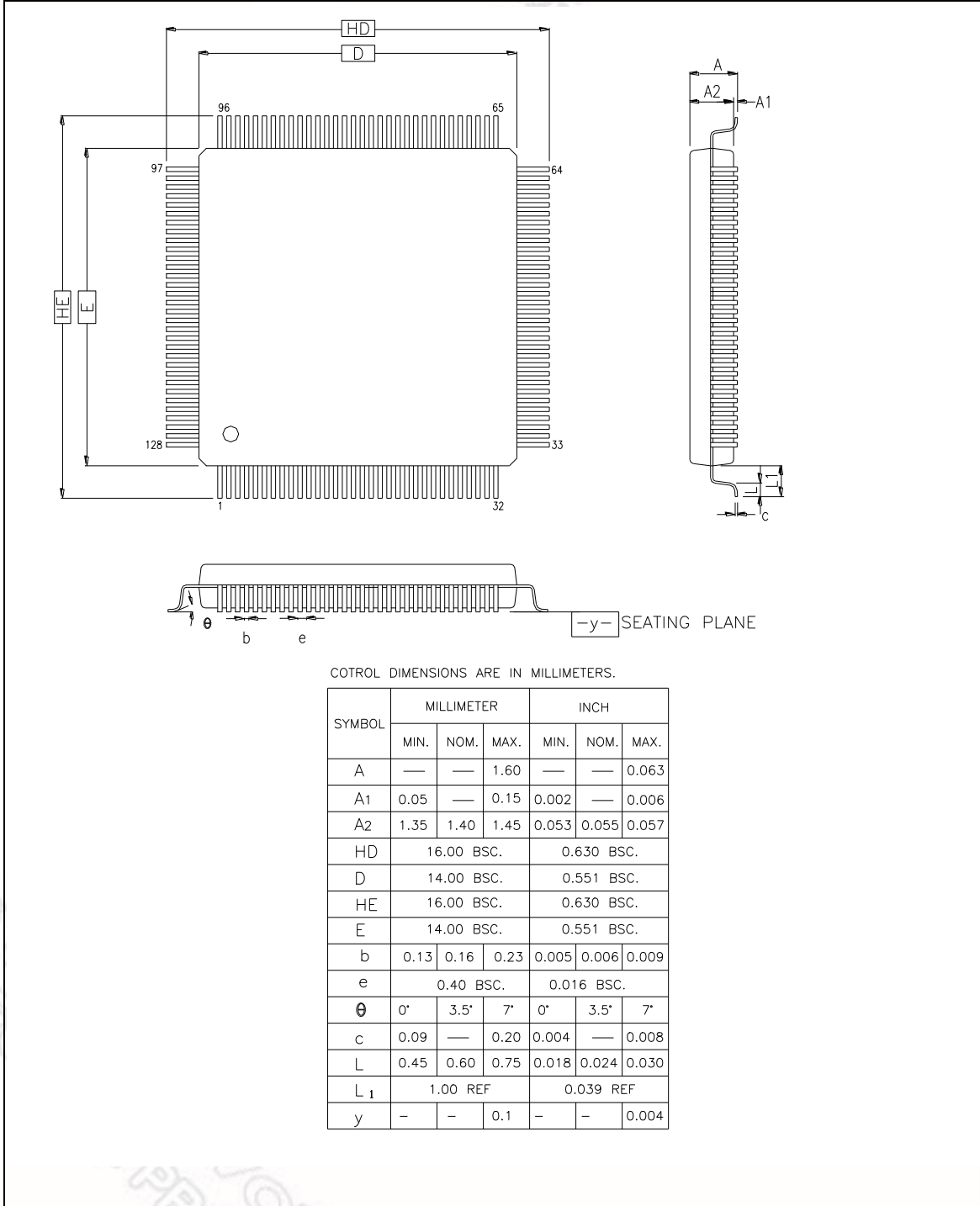
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	VDDD and VDDREG Supply Current (Steady State)	Standby		50		uA
		Input mode		TBD		uA
		Output mode		TBD		uA

7.4.9.4 USB LDO DC Electrical Characteristics

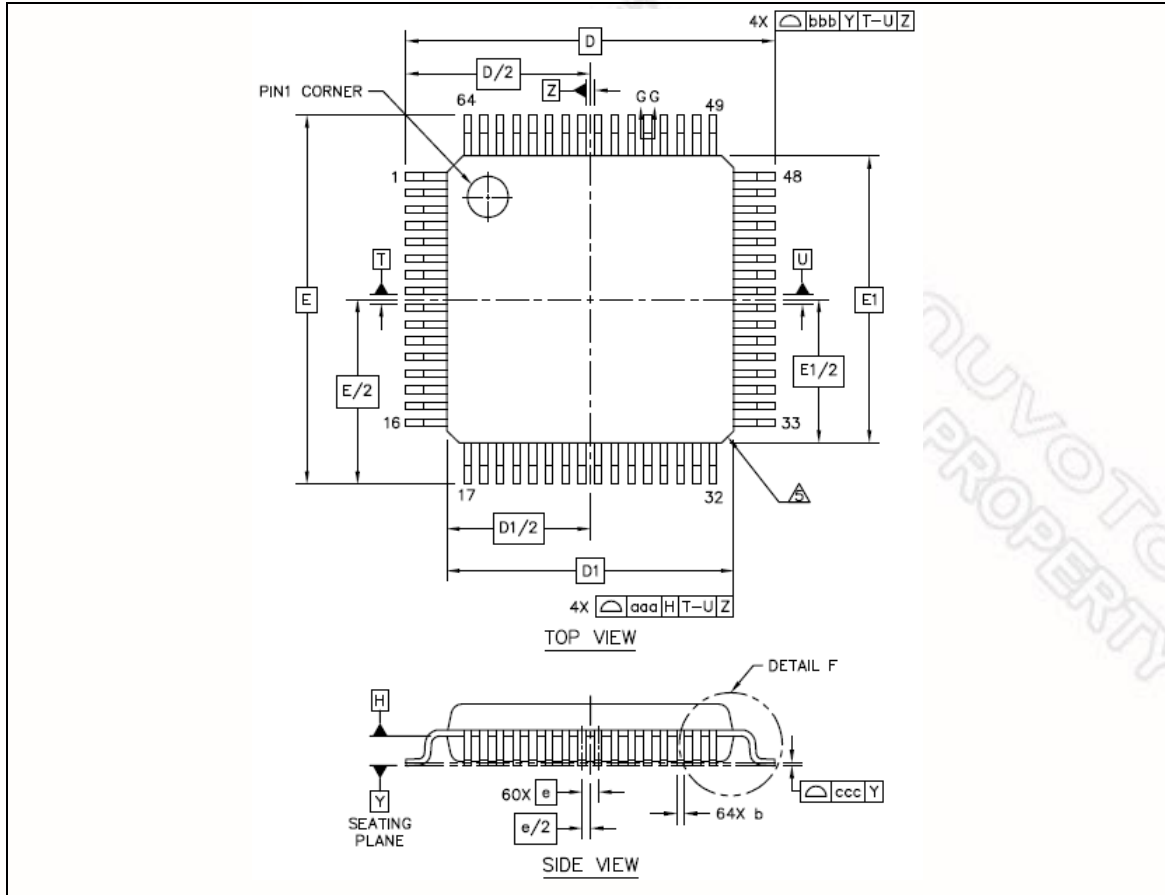
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
VBUS				5		V
V33	Output voltage	VBUS = 5V, 25°C	2.97	3.3	3.63	V
Iop	Operation Current			TBD		uA

8 PACKAGE DIMENSIONS

8.1 128L LQFP (14x14x1.4 mm footprint 2.0 mm)



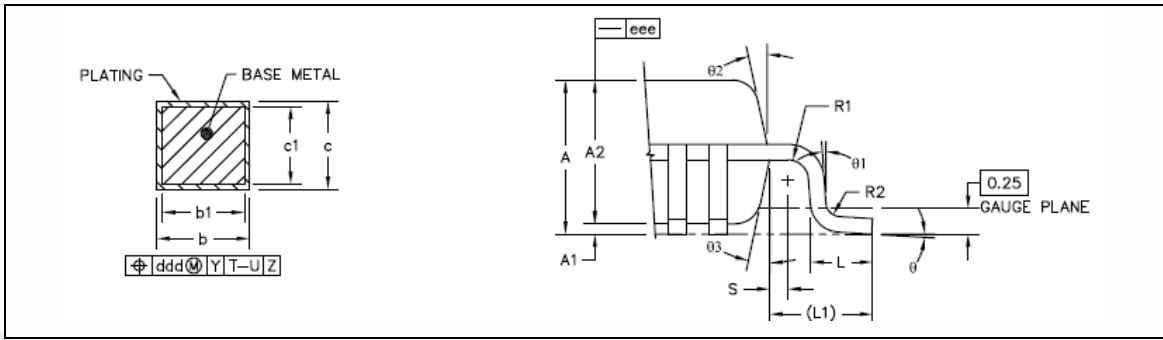
8.2 64L LQFP (7x7x1.4 mm footprint 2.0 mm)



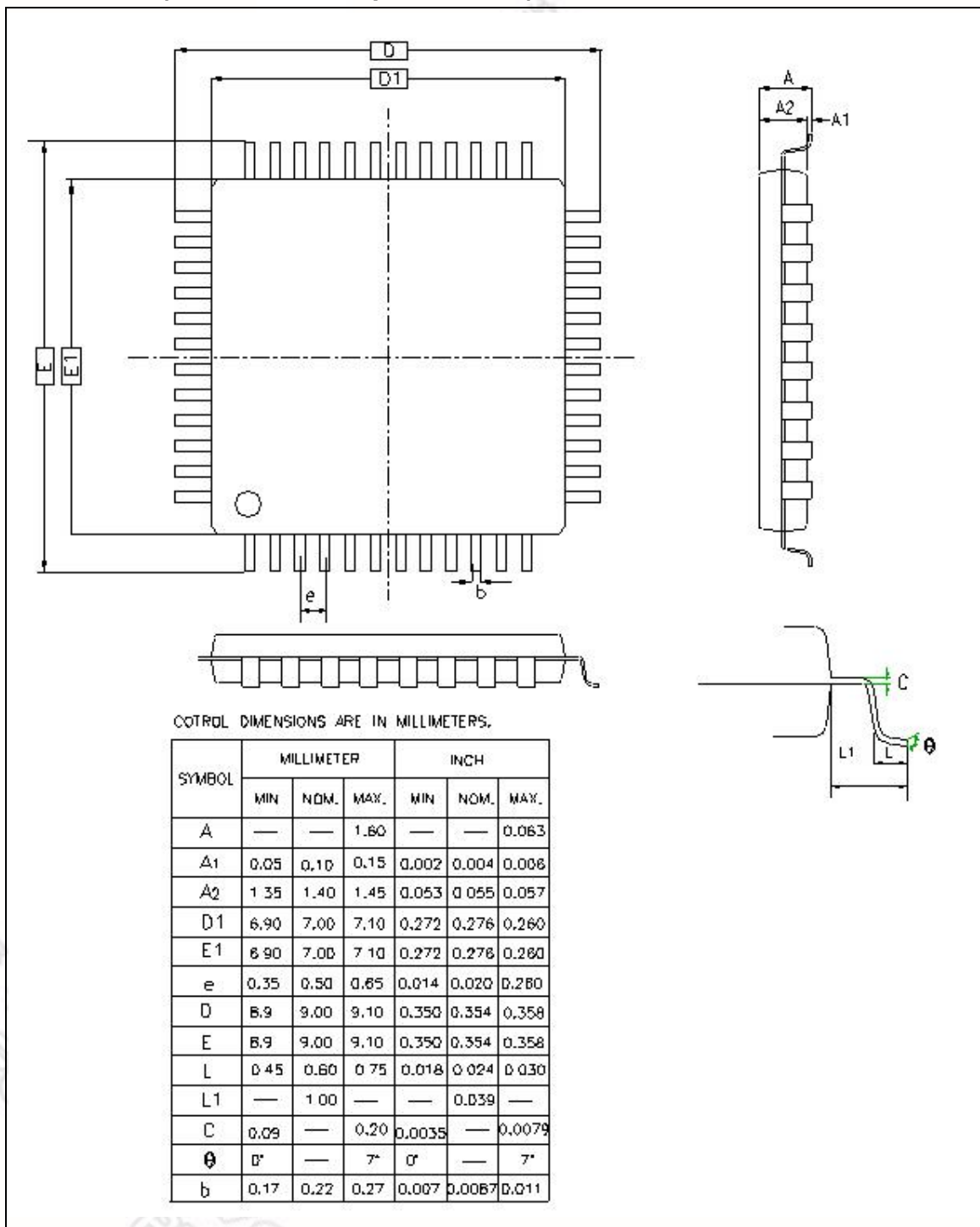
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	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	----	----	1.6
STAND OFF	A1	0.05	----	0.15
MOLD THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)	b	0.13	0.18	0.23
LEAD WIDTH	b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)	c	0.09	----	0.2
L/F THICKNESS	c1	0.09	----	0.16
BODY SIZE	X	D	9 BSC	
	Y	E	9 BSC	
	X	D1	7 BSC	
	Y	E1	7 BSC	
LEAD PITCH	e	0.4 BSC		
	L	0.45	0.6	0.75
FOOTPRINT	L1	1 REF		
	θ	0°	3.5°	7°
	θ1	0°	----	----
	θ2	11°	12°	13°
	θ3	11°	12°	13°
	R1	0.08	----	----
	R2	0.08	----	0.2
	S	0.2	----	----
PACKAGE EDGE TOLERANCE	aaa	0.2		
LEAD EDGE TOLERANCE	bbb	0.2		
COPLANARITY	ccc	0.08		
LEAD OFFSET	ddd	0.07		
MOLD FLATNESS	eee	0.05		



8.3 48L LQFP (7x7x1.4 mm footprint 2.0 mm)



9 REVISION HISTORY

Date	Revision	Description
2012.10.11	V1.00	Formal release

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