LMH6618 Single/LMH6619 Dual 130 MHz, 1.25 mA RRIO Operational Amplifiers

Check for Samples: LMH6618, LMH6619

FEATURES

- **V_S = 5V, R_L = 1 kΩ, T_A = 25°C and A_V = +1, Unless Otherwise Specified.**
- **Operating Voltage Range 2.7V to 11V**
- **Supply Current per Channel 1.25 mA**
- **Small Signal Bandwidth 130 MHz**
- **Input Offset Voltage (Limit at 25°C) ±0.75 mV**
- **Slew Rate 55 V/µs**
- **Settling Time to 0.1% 90 ns**
- **Settling Time to 0.01% 120 ns**
- **SFDR (f = 100 kHz, A_V = +1, V_{OUT} = 2 V_{PP}) 100 dBc**
- **0.1 dB Bandwidth (A_V = +2) 15 MHz**
- **Low Voltage Noise 10 nV/√Hz**
- **Industrial Temperature Grade −40°C to +125°C**
- **Rail-to-Rail Input and Output**

APPLICATIONS

- **ADC Driver**
- **DAC Buffer**
- **Active Filters**
- **High Speed Sensor Amplifier**
- **Current Sense Amplifier**
- **Portable Video**
- **STB, TV Video Amplifier**

DESCRIPTION

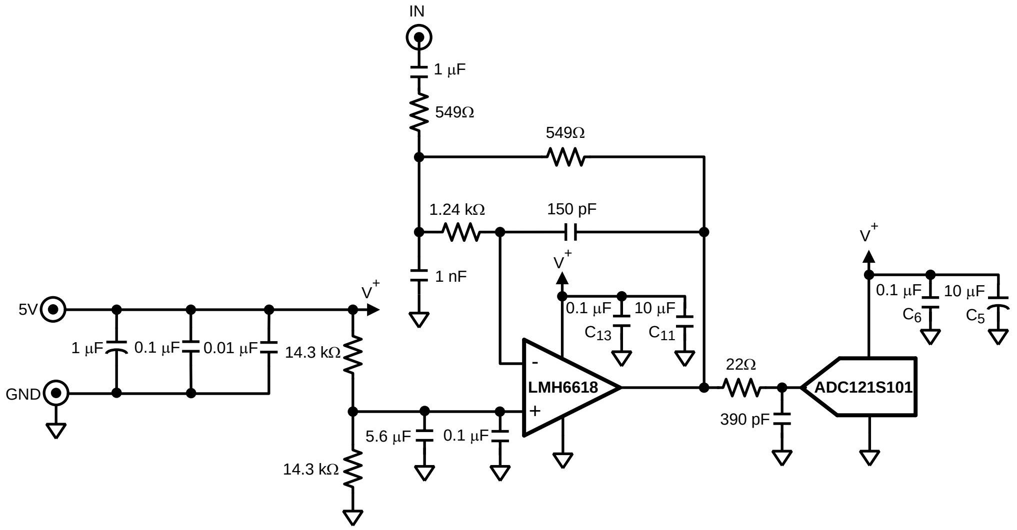
The LMH6618 (single, with shutdown) and LMH6619 (dual) are 130 MHz rail-to-rail input and output amplifiers designed for ease of use in a wide range of applications requiring high speed, low supply current, low noise, and the ability to drive complex ADC and video loads. The operating voltage range extends from 2.7V to 11V and the supply current is typically 1.25 mA per channel at 5V. The LMH6618 and LMH6619 are members of the PowerWise® family and have an exceptional power-to-performance ratio.

The amplifier's voltage feedback design topology provides balanced inputs and high open loop gain for ease of use and accuracy in applications such as active filter design. Offset voltage is typically 0.1 mV and settling time to 0.01% is 120 ns which combined with an 100 dBc SFDR at 100 kHz makes the part suitable for use as an input buffer for popular 8-bit, 10-bit, 12-bit and 14-bit mega-sample ADCs.

The input common mode range extends 200 mV beyond the supply rails. On a single 5V supply with a ground terminated 150Ω load the output swings to within 37 mV of the ground rail, while a mid-rail terminated 1 kΩ load will swing to 77 mV of either rail, providing true single supply operation and maximum signal dynamic range on low power rails. The amplifier output will source and sink 35 mA and drive up to 30 pF loads without the need for external compensation.

The LMH6618 has an active low disable pin which reduces the supply current to 72 µA and is offered in the space saving 6-Pin SOT package. The LMH6619 is offered in the 8-Pin SOIC package. The LMH6618 and LMH6619 are available with a −40°C to +125°C extended industrial temperature grade.

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS [(1)]

ESD Tolerance [(2)]	
Human Body Model	
For input pins only	2000V
For all other pins	2000V
Machine Model	200V
Supply Voltage ($V_S = V^+ – V^−$)	12V
Junction Temperature [(3)]	150°C max

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ θ_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

OPERATING RATINGS [(1)]

Supply Voltage ($V_S = V^+ – V^−$)	2.7V to 11V
Ambient Temperature Range [(2)]	−40°C to +125°C
Package Thermal Resistance ($θ_{JA}$)	
6-Pin SOT (DDC0006A)	231°C/W
8-Pin SOIC (D0008A)	160°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ θ_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

+3V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 3V, V^- = 0V, $\overline{\text{DISABLE}}$ = 3V, $V_{CM} = V_O = V^+/2$, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		120		MHz
		A_V = 2, −1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		56		
GBW	Gain Bandwidth (LMH6618)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	55	71		MHz
GBW	Gain Bandwidth (LMH6619)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	55	63		MHz
LSBW	−3 dB Bandwidth Large Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}		13		MHz
		A_V = 2, R_L = 150Ω, V_{OUT} = 2 V_{PP}		13		
Peak	Peaking	A_V = 1, C_L = 5 pF		1.5		dB
0.1 dBBW	0.1 dB Bandwidth	A_V = 2, V_{OUT} = 0.5 V_{PP} , $R_F = R_G$ = 825Ω		15		MHz
DG	Differential Gain	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.1		%
DP	Differential Phase	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.1		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, A_V = 1		36		ns
SR	Slew Rate	2V Step, A_V = 1	36	46		V/µs
$t_{s\_0.1}$	0.1% Settling Time	2V Step, A_V = −1		90		ns
$t_{s\_0.01}$	0.01% Settling Time	2V Step, A_V = −1		120		
Noise and Distortion Performance						
SFDR	Spurious Free Dynamic Range	f_C = 100 kHz, V_{OUT}= 2 V_{PP}, R_L = 1 kΩ		100		dBc
		f_C = 1 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		61		
		f_C = 5 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		47		
e_n	Input Voltage Noise Density	f = 100 kHz		10		nV//√Hz
i_n	Input Current Noise Density	f = 100 kHz		1		pA//√Hz
CT	Crosstalk (LMH6619)	f = 5 MHz, V_{IN} = 2 V_{PP}		80		dB
Input, DC Performance						
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V (pnp active) V_{CM} = 2.5V (npn active)		0.1	±0.75 **±1.3**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	(4)		0.8		µV/°C
I_B	Input Bias Current	V_{CM} = 0.5V (pnp active)		−1.4	**−2.6**	µA
		V_{CM} = 2.5V (npn active)		+1.0	**+1.8**	
I_{OS}	Input Offset Current			0.01	**±0.27**	µA
C_{IN}	Input Capacitance			1.5		pF
R_{IN}	Input Resistance			8		MΩ
CMVR	Common Mode Voltage Range	DC, CMRR ≥ 65 dB	−0.2		3.2	V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −0.1V to 1.4V	78	96		dB
		V_{CM} Stepped from 2.0V to 3.1V	81	107		
A_{OL}	Open Loop Voltage Gain	R_L = 1 kΩ to +2.7V or +0.3V	85	98		dB
		R_L = 150Ω to +2.6V or +0.4V	76	82		

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(1) Boldface limits apply to temperature range of −40°C to 125°C

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(4) Voltage average drift is determined by dividing the change in V_{OS} by temperature change.

+3V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 3V, V^- = 0V, $\overline{\text{DISABLE}}$ = 3V, $V_{CM} = V_O = V^+/2$, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes. [1]

Symbol	Parameter	Condition	Min [2]	Typ [3]	Max [2]	Units
Output DC Characteristics						
V_{OUT}	Output Voltage Swing High (LMH6618) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		50	56 **62**	mV from either rail
		R_L =150Ω to $V^+/2$		160	172 **198**	
	Output Voltage Swing Low (LMH6618) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		60	66 **74**	
		R_L = 150Ω to $V^+/2$		170	184 **217**	
		R_L = 150Ω to V^-		29	39 **43**	
	Output Voltage Swing High (LMH6619) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		50	56 **62**	mV from either rail
		R_L =150Ω to $V^+/2$		160	172 **198**	
	Output Voltage Swing Low (LMH6619) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		62	68 **76**	
		R_L =150Ω to $V^+/2$		175	189 **222**	
		R_L = 150Ω to V^-		34	44 **48**	
I_{OUT}	Linear Output Current	$V_{OUT} = V^+/2$ (5)	±25	±35		mA
R_{OUT}	Output Resistance	f = 1 MHz		0.17		Ω
Enable Pin Operation						
	Enable High Voltage Threshold	Enabled	2.0			V
	Enable Pin High Current	$V_{\overline{DISABLE}}$ = 3V		0.04		µA
	Enable Low Voltage Threshold	Disabled			1.0	V
	Enable Pin Low Current	$V_{\overline{DISABLE}}$ = 0V		1		µA
t_{on}	Turn-On Time			25		ns
t_{off}	Turn-Off Time			90		ns
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, V_{CM} = 0.5V, V_S = 2.7V to 11V	84	104		dB
I_S	Supply Current (LMH6618)	$R_L = \infty$		1.2	1.5 **1.7**	mA
	Supply Current (LMH6619) (per channel)	$R_L = \infty$		1.2	1.5 **1.75**	
I_{SD}	Disable Shutdown Current	$\overline{\text{DISABLE}}$ = 0V		59	85	µA

(5) Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as it may damage the part.

+5V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 5V, V^- = 0V, $\overline{\text{DISABLE}}$ = 5V, $V_{CM} = V_O = V^+/2$, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		130		MHz
		A_V = 2, −1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		53		
GBW	Gain Bandwidth (LMH6618)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	54	64		MHz
GBW	Gain Bandwidth (LMH6619)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	54	57		MHz
LSBW	−3 dB Bandwidth Large Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}		15		MHz
		A_V = 2, R_L = 150Ω, V_{OUT} = 2 V_{PP}		15		
Peak	Peaking	A_V = 1, C_L = 5 pF		0.5		dB
0.1 dBBW	0.1 dB Bandwidth	A_V = 2, V_{OUT} = 0.5 V_{PP}, $R_F = R_G$ = 1 kΩ		15		MHz
DG	Differential Gain	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.1		%
DP	Differential Phase	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.1		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, A_V = 1		30		ns
SR	Slew Rate	2V Step, A_V = 1	44	55		V/µs
$t_{s\_0.1}$	0.1% Settling Time	2V Step, A_V = −1		90		ns
$t_{s\_0.01}$	0.01% Settling Time	2V Step, A_V = −1		120		
Distortion and Noise Performance						
SFDR	Spurious Free Dynamic Range	f_C = 100 kHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		100		dBc
		f_C = 1 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		88		
		f_C = 5 MHz, V_O = 2 V_{PP}, R_L = 1 kΩ		61		
e_n	Input Voltage Noise Density	f = 100 kHz		10		nV//√Hz
i_n	Input Current Noise Density	f = 100 kHz		1		pA//√Hz
CT	Crosstalk (LMH6619)	f = 5 MHz, V_{IN} = 2 V_{PP}		80		dB
Input, DC Performance						
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V (pnp active) V_{CM} = 4.5V (npn active)		0.1	±0.75 **±1.3**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	(3)		0.8		µV/°C
I_B	Input Bias Current	V_{CM} = 0.5V (pnp active)		−1.5	**−2.4**	µA
		V_{CM} = 4.5V (npn active)		+1.0	**+1.9**	
I_{OS}	Input Offset Current			0.01	**±0.26**	µA
C_{IN}	Input Capacitance			1.5		pF
R_{IN}	Input Resistance			8		MΩ
CMVR	Common Mode Voltage Range	DC, CMRR ≥ 65 dB	−0.2		5.2	V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −0.1V to 3.4V	81	98		dB
		V_{CM} Stepped from 4.0V to 5.1V	84	108		
A_{OL}	Open Loop Voltage Gain	R_L = 1 kΩ to +4.6V or +0.4V	84	100		dB
		R_L = 150Ω to +4.5V or +0.5V	78	83		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Voltage average drift is determined by dividing the change in V_{OS} by temperature change.

+5V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 5V, V^- = 0V, $\overline{\text{DISABLE}}$ = 5V, V_{CM} = V_O = $V^+/2$, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
Output DC Characteristics						
V_{OUT}	Output Voltage Swing High (LMH6618) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		60	73 **82**	mV from either rail
		R_L = 150Ω to $V^+/2$		230	255 **295**	
	Output Voltage Swing Low (LMH6618) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		75	83 **96**	
		R_L = 150Ω to $V^+/2$		250	270 **321**	
		R_L = 150Ω to V^-		32	43 **45**	
	Output Voltage Swing High (LMH6619) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		60	73 **82**	mV from either rail
		R_L = 150Ω to $V^+/2$		230	255 **295**	
	Output Voltage Swing Low (LMH6619) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		77	85 **98**	
		R_L = 150Ω to $V^+/2$		255	275 **326**	
		R_L = 150Ω to V^-		37	48 **50**	
I_{OUT}	Linear Output Current	V_{OUT} = $V^+/2$ (4)	±25	±35		mA
R_{OUT}	Output Resistance	f = 1 MHz		0.17		Ω
Enable Pin Operation						
	Enable High Voltage Threshold	Enabled	3.0			V
	Enable Pin High Current	$V_{\overline{DISABLE}}$ = 5V		1.2		µA
	Enable Low Voltage Threshold	Disabled			2.0	V
	Enable Pin Low Current	$V_{\overline{DISABLE}}$ = 0V		2.5		µA
t_{on}	Turn-On Time			25		ns
t_{off}	Turn-Off Time			90		ns
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, V_{CM} = 0.5V, V_S = 2.7V to 11V	84	104		dB
I_S	Supply Current (LMH6618)	R_L = ∞		1.25	1.5 **1.7**	mA
	Supply Current (LMH6619) (per channel)	R_L = ∞		1.3	1.5 **1.75**	
I_{SD}	Disable Shutdown Current	$\overline{\text{DISABLE}}$ = 0V		72	105	µA

(4) Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as it may damage the part.

±5V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are guaranteed for $T_J = +25°C$, $V^+ = 5V$, $V^- = -5V$, $\overline{DISABLE} = 5V$, $V_{CM} = V_O = 0V$, $A_V = +1$ ($R_F = 0\Omega$), otherwise $R_F = 2\ k\Omega$ for $A_V \neq +1$, $R_L = 1\ k\Omega \ \|\ 5\ pF$. **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	$A_V = 1$, $R_L = 1\ k\Omega$, $V_{OUT} = 0.2\ V_{PP}$		140		MHz
		$A_V = 2, -1$, $R_L = 1\ k\Omega$, $V_{OUT} = 0.2\ V_{PP}$		53		
GBW	Gain Bandwidth (LMH6618)	$A_V = 10$, $R_F = 2\ k\Omega$, $R_G = 221\Omega$, $R_L = 1\ k\Omega$, $V_{OUT} = 0.2\ V_{PP}$	54	65		MHz
GBW	Gain Bandwidth (LMH6619)	$A_V = 10$, $R_F = 2\ k\Omega$, $R_G = 221\Omega$, $R_L = 1\ k\Omega$, $V_{OUT} = 0.2\ V_{PP}$	54	58		MHz
LSBW	−3 dB Bandwidth Large Signal	$A_V = 1$, $R_L = 1\ k\Omega$, $V_{OUT} = 2\ V_{PP}$		16		MHz
		$A_V = 2$, $R_L = 150\Omega$, $V_{OUT} = 2\ V_{PP}$		15		
Peak	Peaking	$A_V = 1$, $C_L = 5\ pF$		0.05		dB
0.1 dBBW	0.1 dB Bandwidth	$A_V = 2$, $V_{OUT} = 0.5\ V_{PP}$, $R_F = R_G = 1.21\ k\Omega$		15		MHz
DG	Differential Gain	$A_V = +2$, 4.43 MHz, $0.6V < V_{OUT} < 2V$, $R_L = 150\Omega$ to $V^+/2$		0.1		%
DP	Differential Phase	$A_V = +2$, 4.43 MHz, $0.6V < V_{OUT} < 2V$, $R_L = 150\Omega$ to $V^+/2$		0.1		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, $A_V = 1$		30		ns
SR	Slew Rate	2V Step, $A_V = 1$	45	57		V/μs
$t_{s\_0.1}$	0.1% Settling Time	2V Step, $A_V = -1$		90		ns
$t_{s\_0.01}$	0.01% Settling Time	2V Step, $A_V = -1$		120		
Noise and Distortion Performance						
SFDR	Spurious Free Dynamic Range	$f_C = 100\ kHz$, $V_{OUT} = 2\ V_{PP}$, $R_L = 1\ k\Omega$		100		dBc
		$f_C = 1\ MHz$, $V_{OUT} = 2\ V_{PP}$, $R_L = 1\ k\Omega$		88		
		$f_C = 5\ MHz$, $V_{OUT} = 2\ V_{PP}$, $R_L = 1\ k\Omega$		70		
e_n	Input Voltage Noise Density	f = 100 kHz		10		$nV/\sqrt{Hz}$
i_n	Input Current Noise Density	f = 100 kHz		1		$pA/\sqrt{Hz}$
CT	Crosstalk (LMH6619)	f = 5 MHz, $V_{IN} = 2\ V_{PP}$		80		dB
Input DC Performance						
V_{OS}	Input Offset Voltage	$V_{CM} = -4.5V$ (pnp active) $V_{CM} = 4.5V$ (npn active)		0.1	±0.75 **±1.3**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	(3)		0.9		μV/°C
I_B	Input Bias Current	$V_{CM} = -4.5V$ (pnp active)		−1.5	**−2.4**	μA
		$V_{CM} = 4.5V$ (npn active)		+1.0	**+1.9**	
I_{OS}	Input Offset Current			0.01	**±0.26**	μA
C_{IN}	Input Capacitance			1.5		pF
R_{IN}	Input Resistance			8		MΩ
CMVR	Common Mode Voltage Range	DC, CMRR ≥ 65 dB	−5.2		5.2	V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −5.1V to 3.4V	84	100		dB
		V_{CM} Stepped from 4.0V to 5.1V	83	108		
A_{OL}	Open Loop Voltage Gain	$R_L = 1\ k\Omega$ to +4.6V or −4.6V	86	95		dB
		$R_L = 150\Omega$ to +4.3V or −4.3V	79	84		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(3) Voltage average drift is determined by dividing the change in V_{OS} by temperature change.

±5V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 5V, V^- = −5V, $\overline{\text{DISABLE}}$ = 5V, V_{CM} = V_O = 0V, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
Output DC Characteristics						
V_{OUT}	Output Voltage Swing High (LMH6618) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to GND		100	111 **126**	mV from either rail
		R_L = 150Ω to GND		430	457 **526**	
	Output Voltage Swing Low (LMH6618) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to GND		110	121 **136**	
		R_L = 150Ω to GND		440	474 **559**	
		R_L = 150Ω to V^-		35	51 **52**	
	Output Voltage Swing High (LMH6619) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to GND		100	111 **126**	mV from either rail
		R_L = 150Ω to GND		430	457 **526**	
	Output Voltage Swing Low (LMH6619) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to GND		115	126 **141**	
		R_L = 150Ω to GND		450	484 **569**	
		R_L = 150Ω to V^-		45	61 **62**	
I_{OUT}	Linear Output Current	V_{OUT} = $V^+/2$ (4)	±25	±35		mA
R_{OUT}	Output Resistance	f = 1 MHz		0.17		Ω
Enable Pin Operation						
	Enable High Voltage Threshold	Enabled	0.5			V
	Enable Pin High Current	$V_{\overline{DISABLE}}$ = +5V		16		µA
	Enable Low Voltage Threshold	Disabled			−0.5	V
	Enable Pin Low Current	$V_{\overline{DISABLE}}$ = −5V		17		µA
t_{on}	Turn-On Time			25		ns
t_{off}	Turn-Off Time			90		ns
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, V_{CM} = −4.5V, V_S = 2.7V to 11V	84	104		dB
I_S	Supply Current (LMH6618)	R_L = ∞		1.35	1.6 **1.9**	mA
	Supply Current (LMH6619) (per channel)	R_L = ∞		1.45	1.65 **2.0**	
I_{SD}	Disable Shutdown Current	$\overline{\text{DISABLE}}$ = −5V		103	140	µA

(4) Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as it may damage the part.

Connection Diagram

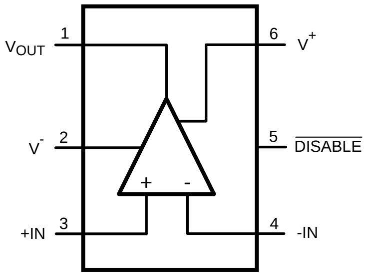

Figure 1. 6-Pin SOT – Top View
(See Package Number DDC0006A)

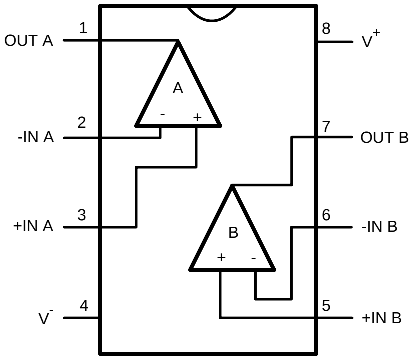

Figure 2. 8-Pin SOIC – Top View
(See Package Number D0008A)

TYPICAL PERFORMANCE CHARACTERISTICS

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, unless otherwise specified.

Closed Loop Frequency Response for Various Supplies

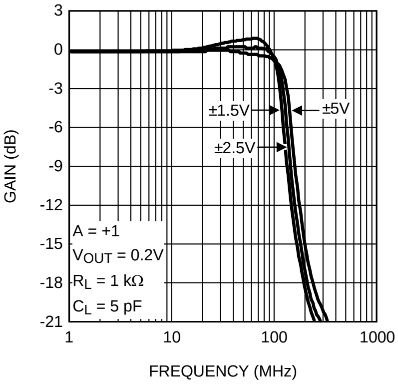

Figure 3.

Closed Loop Frequency Response for Various Supplies

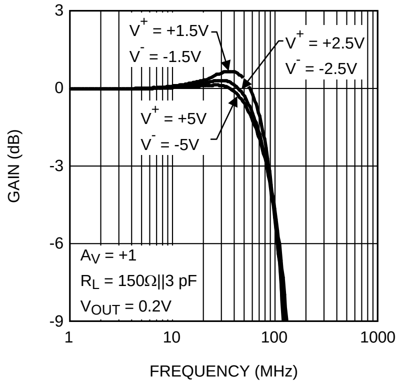

Figure 4.

Closed Loop Frequency Response for Various Supplies

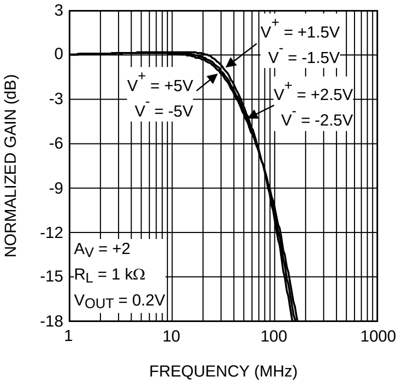

Figure 5.

Closed Loop Frequency Response for Various Supplies

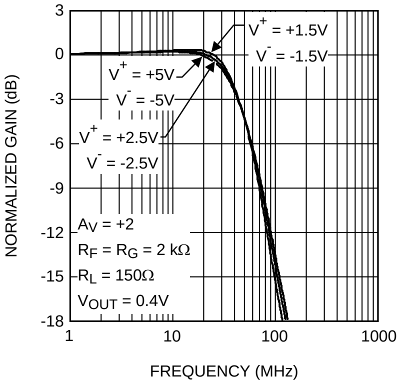

Figure 6.

Closed Loop Frequency Response for Various Temperatures

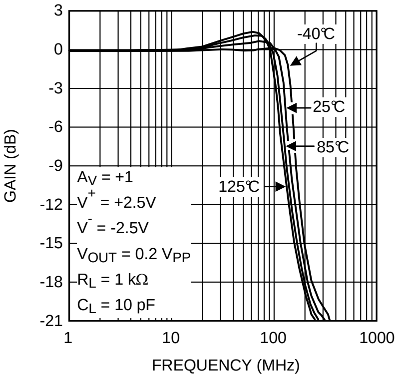

Figure 7.

Closed Loop Frequency Response for Various Temperatures

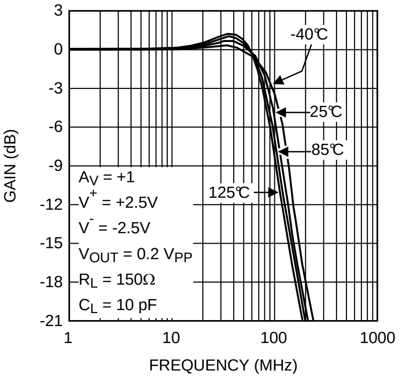

Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq$ +1, unless otherwise specified.

Closed Loop Gain vs. Frequency for Various Gains

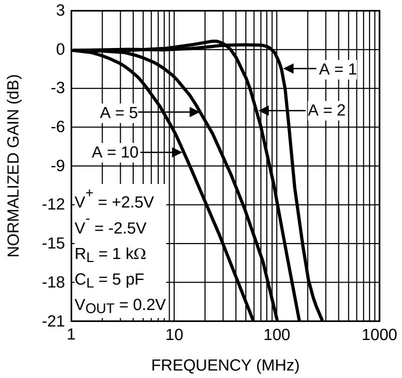

Figure 9.

Large Signal Frequency Response

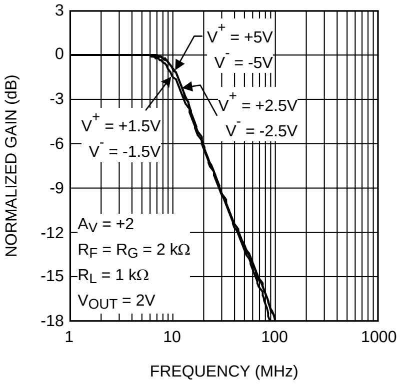

Figure 10.

±0.1 dB Gain Flatness for Various Supplies

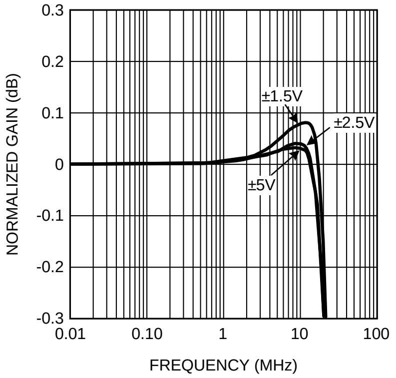

Figure 11.

Small Signal Frequency Response with Various Capacitive Load

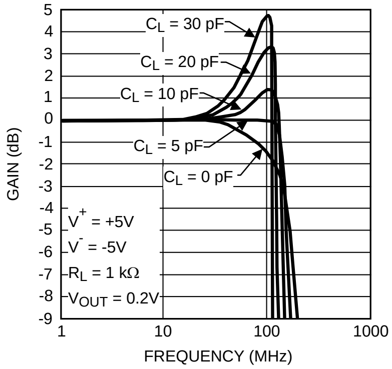

Figure 12.

Small Signal Frequency Response with Capacitive Load and Various R_{ISO}

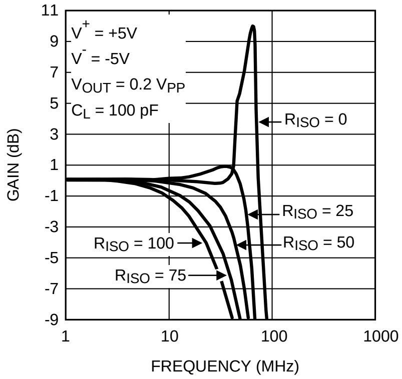

Figure 13.

HD2
vs.
Frequency and Supply Voltage

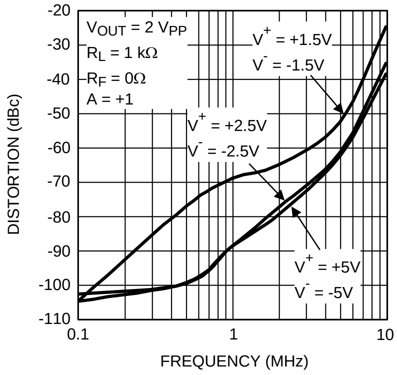

Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, unless otherwise specified.

HD3 vs. Frequency and Supply Voltage

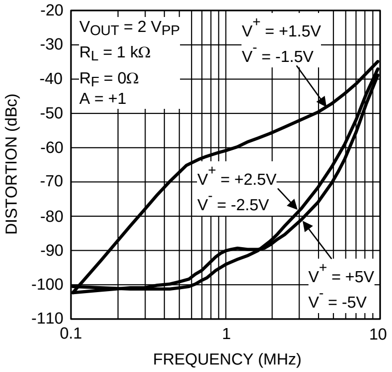

Figure 15.

HD2 and HD3 vs. Frequency and Load

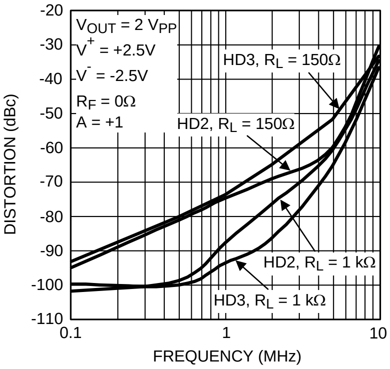

Figure 16.

HD2 and HD3 vs. Common Mode Voltage

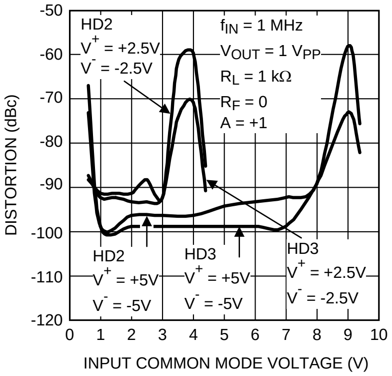

Figure 17.

HD2 and HD3 vs. Common Mode Voltage

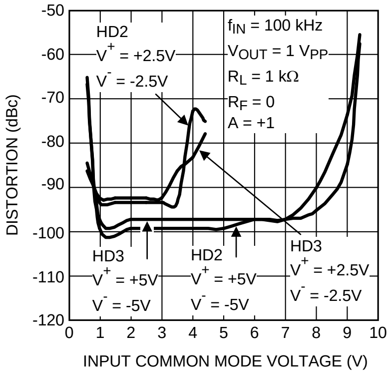

Figure 18.

HD2 vs. Frequency and Gain

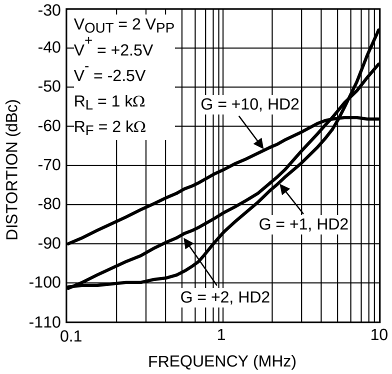

Figure 19.

HD3 vs. Frequency and Gain

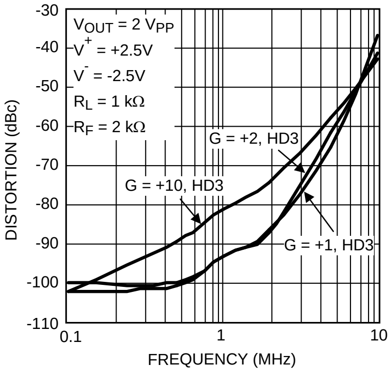

Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, unless otherwise specified.

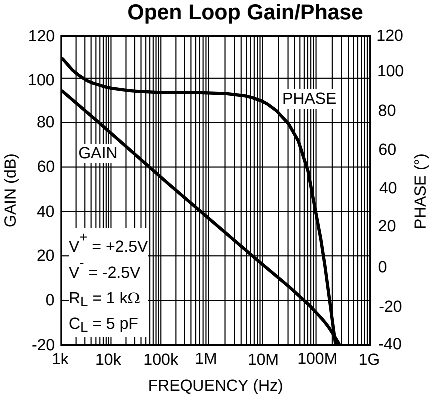
Open Loop Gain/Phase

Figure 21.

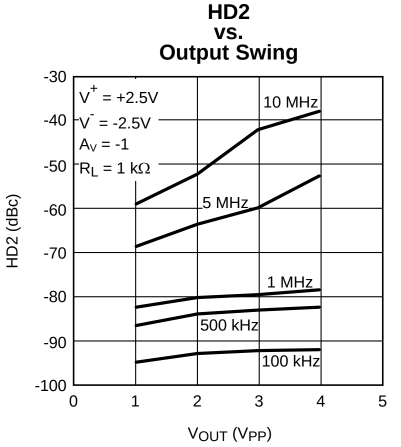
HD2 vs. Output Swing

Figure 22.

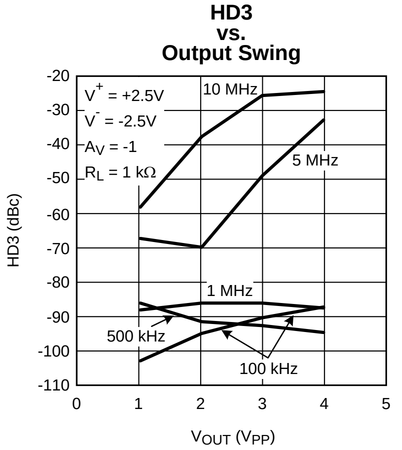
HD3 vs. Output Swing

Figure 23.

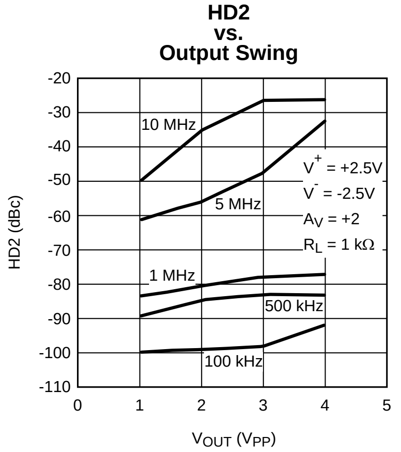
HD2 vs. Output Swing

Figure 24.

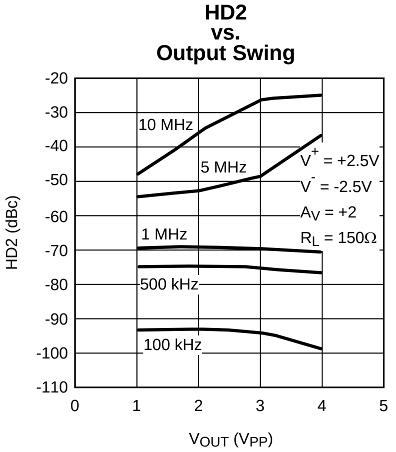
HD2 vs. Output Swing

Figure 25.

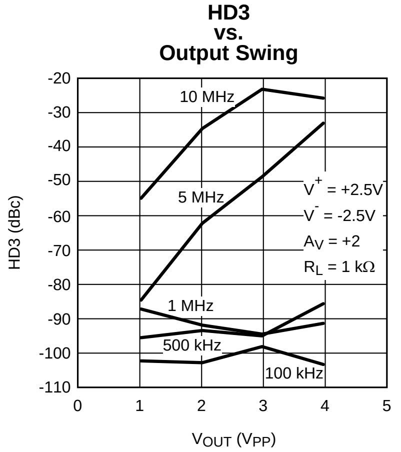
HD3 vs. Output Swing

Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, unless otherwise specified.

HD3 vs. Output Swing

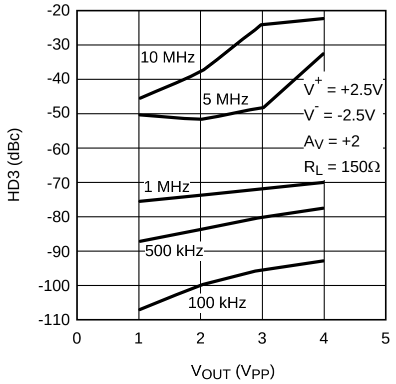

Figure 27.

THD vs. Output Swing

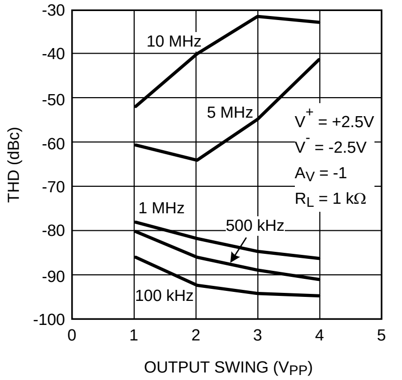

Figure 28.

Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)

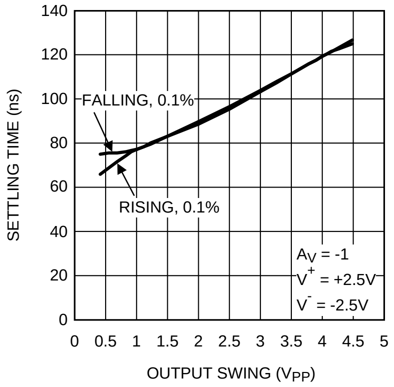

Figure 29.

Input Noise vs. Frequency

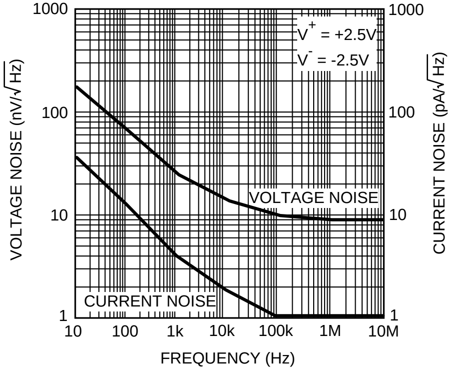

Figure 30.

V_{OS} vs. V_{OUT}

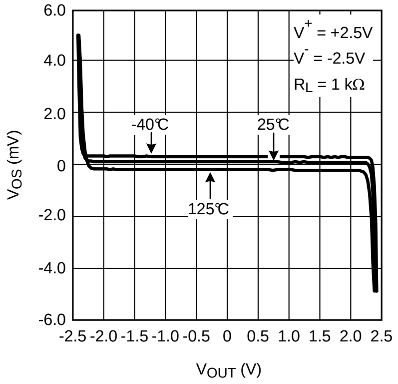

Figure 31.

V_{OS} vs. V_{OUT}

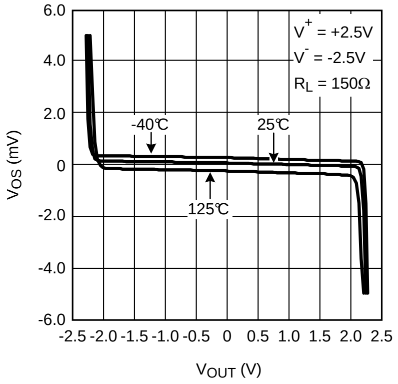

Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, unless otherwise specified.

V_{OS} vs. V_{CM}

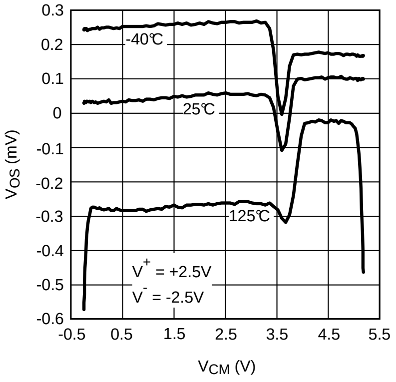

Figure 33.

V_{OS} vs. V_S (pnp)

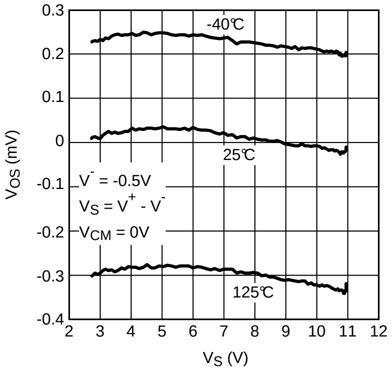

Figure 34.

V_{OS} vs. V_S (npn)

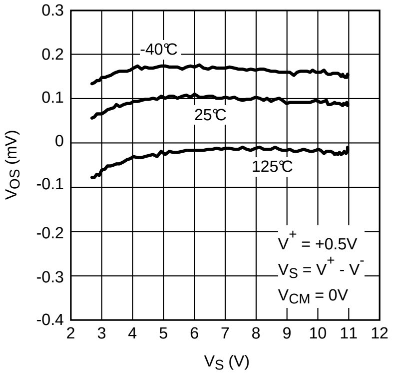

Figure 35.

V_{OS} vs. I_{OUT}

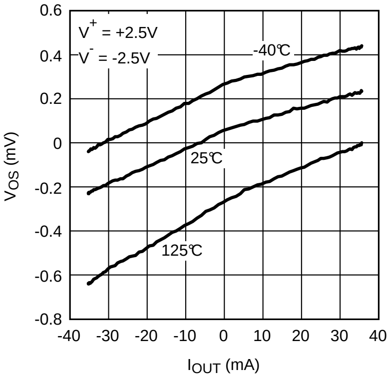

Figure 36.

V_{OS} Distribution (pnp and npn)

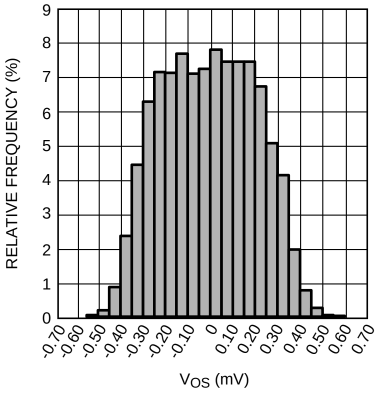

Figure 37.

I_B vs. V_S (pnp)

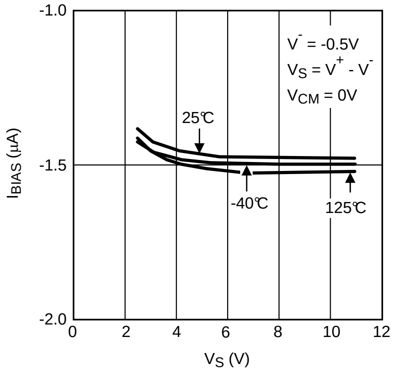

Figure 38.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, unless otherwise specified.

I_B vs. V_S (npn)

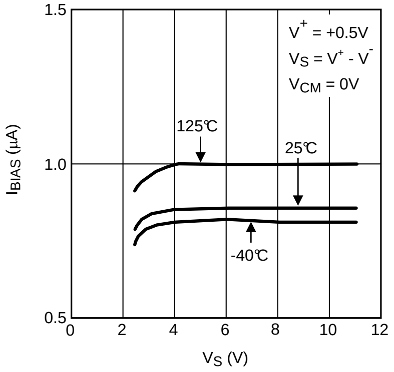

Figure 39.

I_S vs. V_S

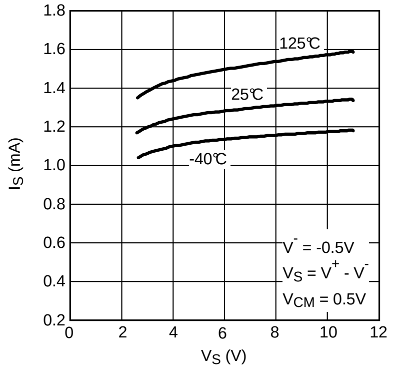

Figure 40.

V_{OUT} vs. V_S

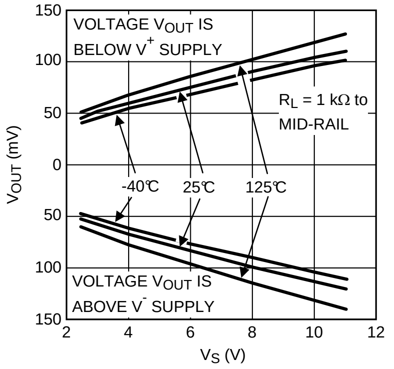

Figure 41.

V_{OUT} vs. V_S

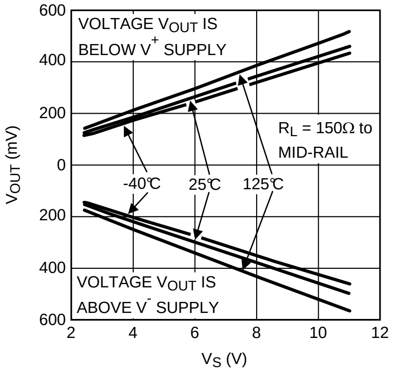

Figure 42.

V_{OUT} vs. V_S

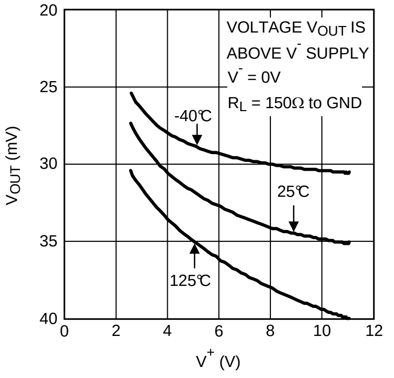

Figure 43.

Closed Loop Output Impedance vs. Frequency A_V = +1

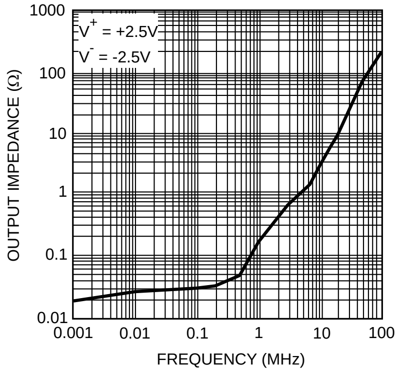

Figure 44.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = 25°C$, $A_V = +1$ ($R_F = 0\Omega$), otherwise $R_F = 2\ k\Omega$ for $A_V \neq +1$, unless otherwise specified.

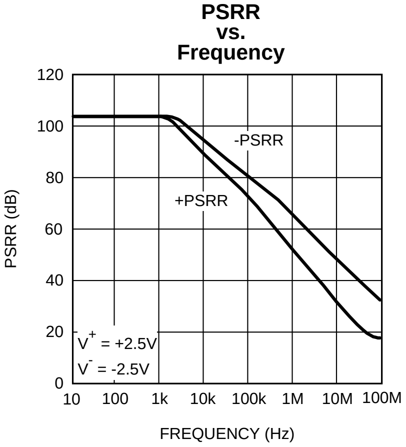

Figure 45.

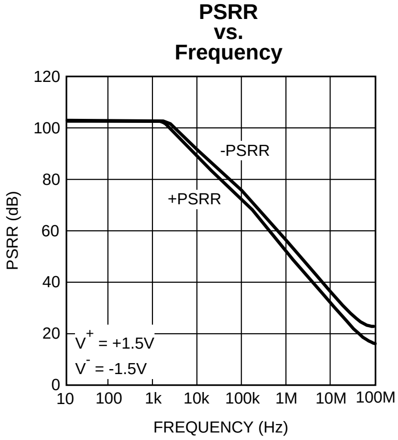

Figure 46.

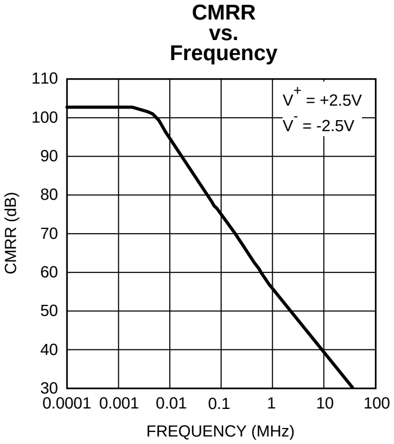

Figure 47.

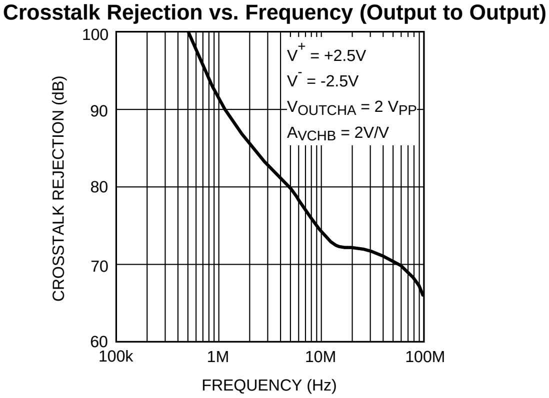

Figure 48.

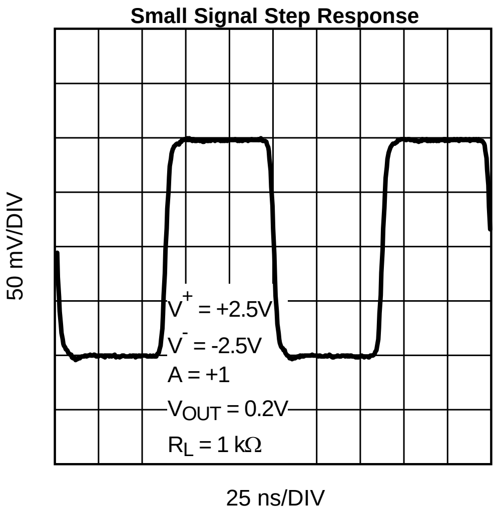

Figure 49.

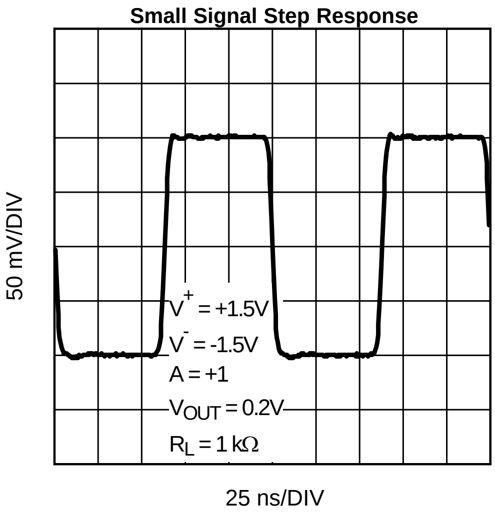

Figure 50.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq$ +1, unless otherwise specified.

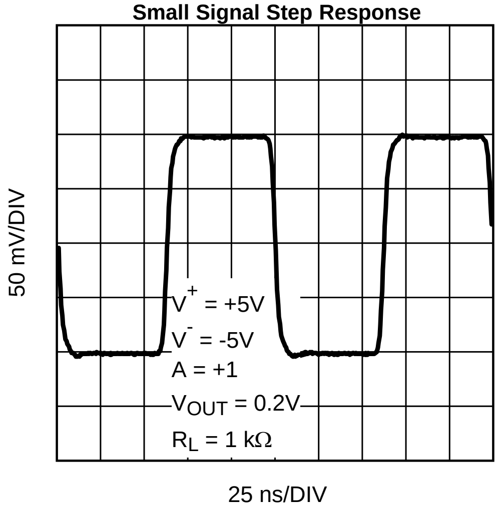

Figure 51.

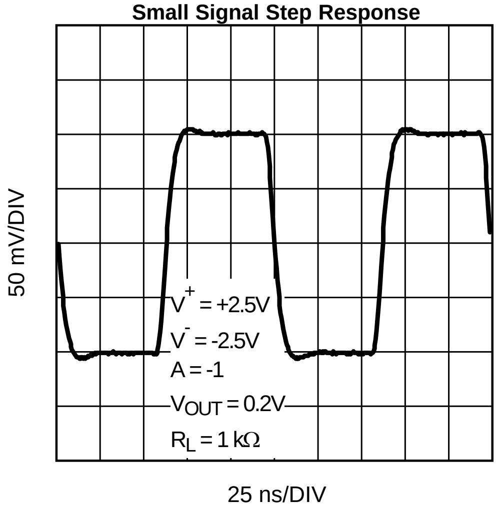

Figure 52.

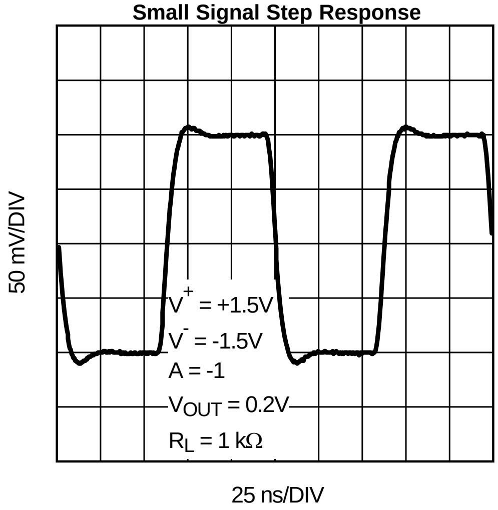

Figure 53.

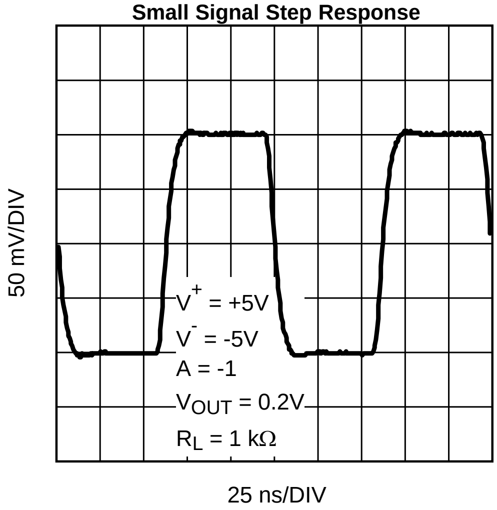

Figure 54.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, unless otherwise specified.

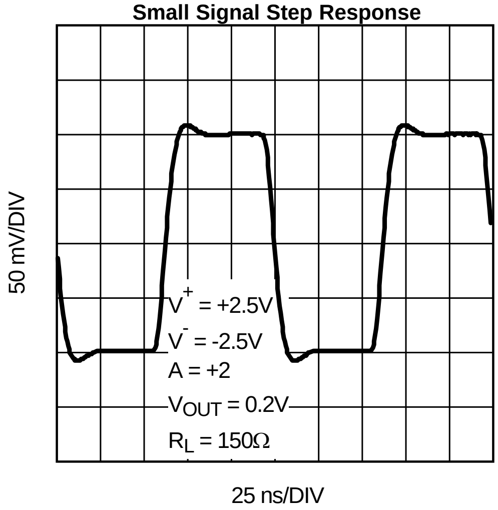
Small Signal Step Response

Figure 55.

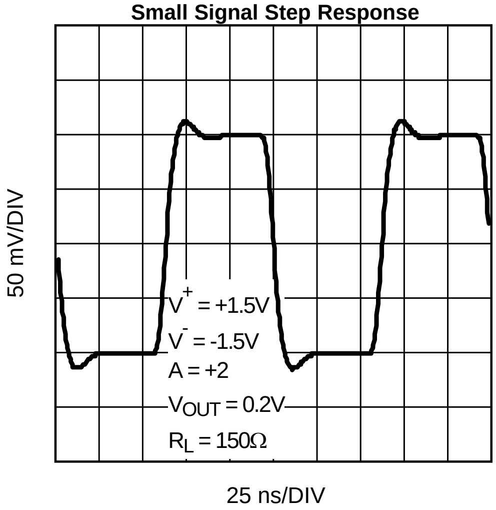
Small Signal Step Response

Figure 56.

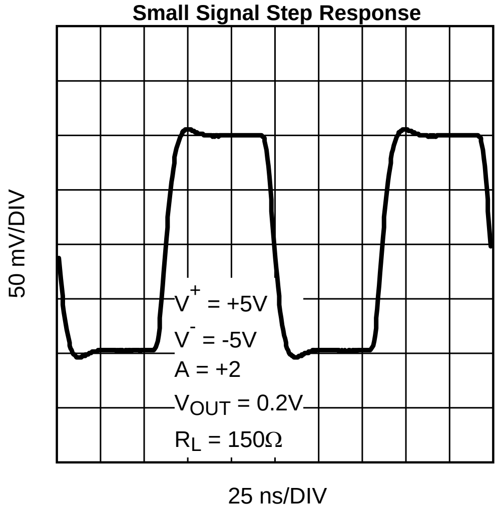
Small Signal Step Response

Figure 57.

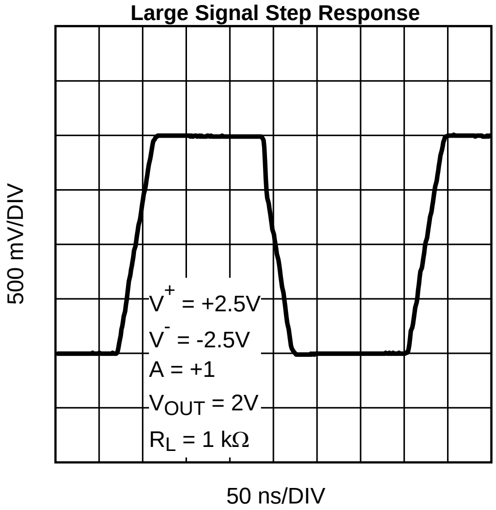
Large Signal Step Response

Figure 58.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = 25°C$, $A_V = +1$ ($R_F = 0\Omega$), otherwise $R_F = 2\ k\Omega$ for $A_V \neq +1$, unless otherwise specified.

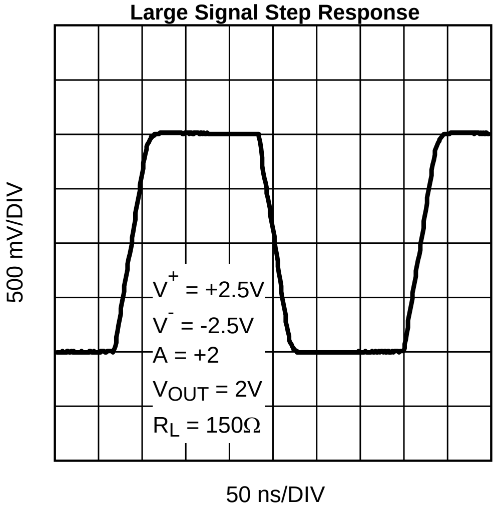

Figure 59.

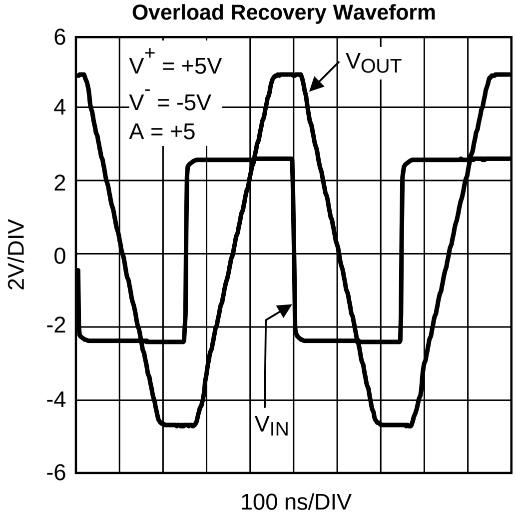

Figure 60.

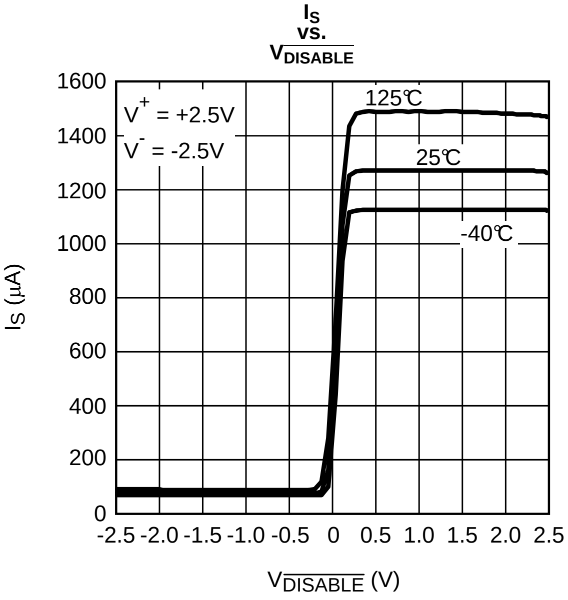

Figure 61.

APPLICATION INFORMATION

The LMH6618 and LMH6619 are based on TI's proprietary VIP10 dielectrically isolated bipolar process. This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8 GHz) even under low supply voltage (2.7V) and low bias current.
- Common emitter push-push output stage. This architecture allows the output to reach within millivolts of either supply rail.
- Consistent performance from any supply voltage (2.7V - 11V) with little variation with supply voltage for the most important specifications (e.g. BW, SR, I_{OUT}.)
- Significant power saving compared to competitive devices on the market with similar performance.

With 3V supplies and a common mode input voltage range that extends beyond either supply rail, the LMH6618 and LMH6619 are well suited to many low voltage/low power applications. Even with 3V supplies, the −3 dB BW (at A_V = +1) is typically 120 MHz.

The LMH6618 and LMH6619 are designed to avoid output phase reversal. With input over-drive, the output is kept near the supply rail (or as close to it as mandated by the closed loop gain setting and the input voltage). Figure 62 shows the input and output voltage when the input voltage significantly exceeds the supply voltages.

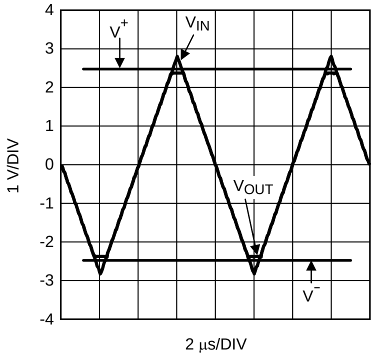

Figure 62. Input and Output Shown with CMVR Exceeded

If the input voltage range is exceeded by more than a diode drop beyond either rail, the internal ESD protection diodes will start to conduct. The current flow in these ESD diodes should be externally limited.

The LMH6618 can be shutdown by connecting the $\overline{\text{DISABLE}}$ pin to a voltage 0.5V below the supply midpoint which will reduce the supply current to typically less than 100 µA. The $\overline{\text{DISABLE}}$ pin is "active low" and should be connected through a resistor to V^+ for normal operation. Shutdown is guaranteed when the $\overline{\text{DISABLE}}$ pin is 0.5V below the supply midpoint at any operating supply voltage and temperature.

In the shutdown mode, essentially all internal device biasing is turned off in order to minimize supply current flow and the output goes into high impedance mode. During shutdown, the input stage has an equivalent circuit as shown in Figure 63.

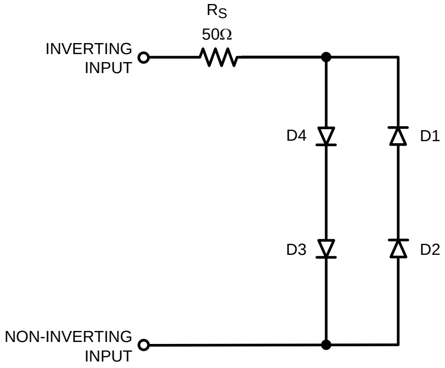

Figure 63. Input Equivalent Circuit During Shutdown

When the LMH6618 is shutdown, there may be current flow through the internal diodes shown, caused by input potential, if present. This current may flow through the external feedback resistor and result in an apparent output signal. In most shutdown applications the presence of this output is inconsequential. However, if the output is “forced” by another device, the other device will need to conduct the current described in order to maintain the output potential.

To keep the output at or near ground during shutdown when there is no other device to hold the output low, a switch using a transistor can be used to shunt the output to ground.

SINGLE CHANNEL ADC DRIVER

The low noise and wide bandwidth make the LMH6618 an excellent choice for driving a 12-bit ADC. Figure 64 shows the schematic of the LMH6618 driving an ADC121S101. The ADC121S101 is a single channel 12-bit ADC. The LMH6618 is set up in a 2nd order multiple-feedback configuration with a gain of −1. The −3 dB point is at 500 kHz and the −0.01 dB point is at 100 kHz. The 22Ω resistor and 390 pF capacitor form an antialiasing filter for the ADC121S101. The capacitor also stores and delivers charge to the switched capacitor input of the ADC. The capacitive load on the LMH6618 created by the 390 pF capacitor is decreased by the 22Ω resistor. Table 1 shows the performance data of the LMH6618 and the ADC121S101.

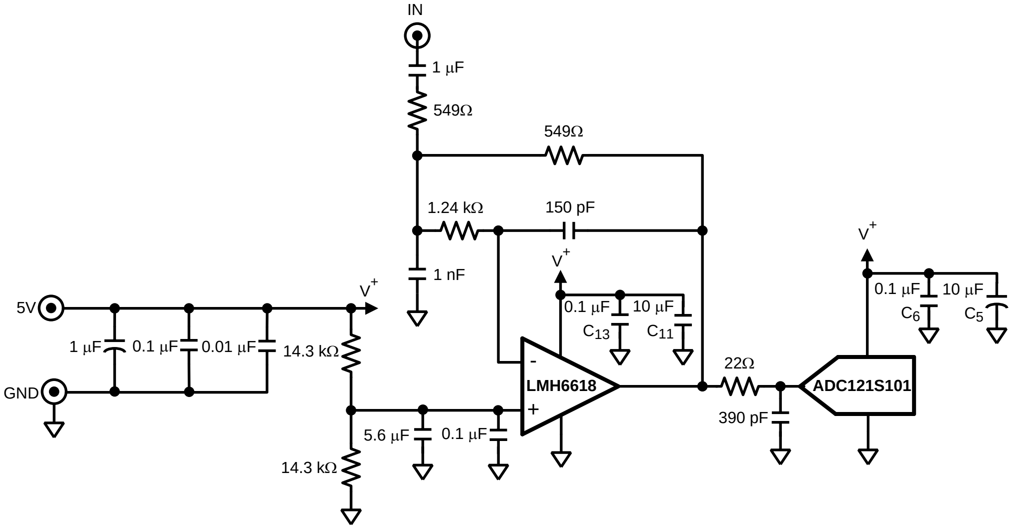

Figure 64. LMH6618 Driving an ADC121S101

Table 1. Performance Data for the LMH6618 Driving an ADC121S101

Parameter	Measured Value
Signal Frequency	100 kHz
Signal Amplitude	4.5V
SINAD	71.5 dB
SNR	71.87 dB
THD	−82.4 dB
SFDR	90.97 dB
ENOB	11.6 bits

When the op amp and the ADC are using the same supply, it is important that both devices are well bypassed. A 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor should be located as close as possible to each supply pin. A sample layout is shown in Figure 65. The 0.1 µF capacitors (C13 and C6) and the 10 µF capacitors (C11 and C5) are located very close to the supply pins of the LMH6618 and the ADC121S101.

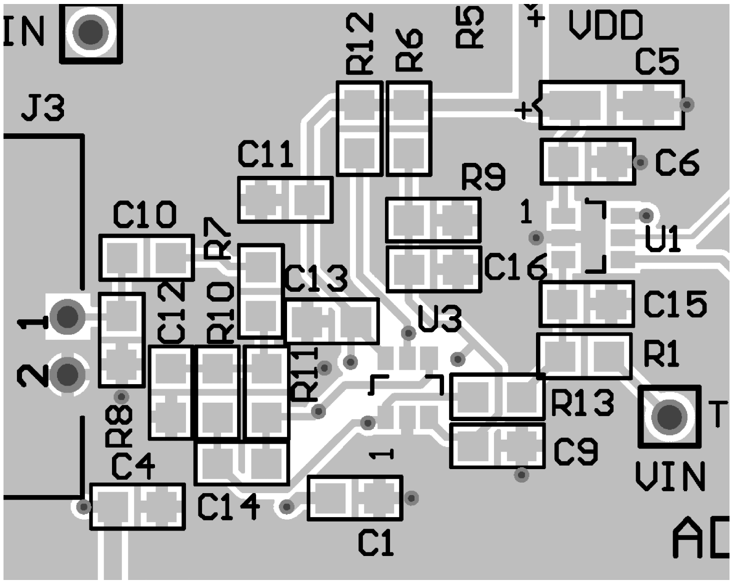

Figure 65. LMH6618 and ADC121S101 Layout

SINGLE TO DIFFERENTIAL ADC DRIVER

Figure 66 shows the LMH6619 used to drive a differential ADC with a single-ended input. The ADC121S625 is a fully differential 12-bit ADC. Table 2 shows the performance data of the LMH6619 and the ADC121S625.

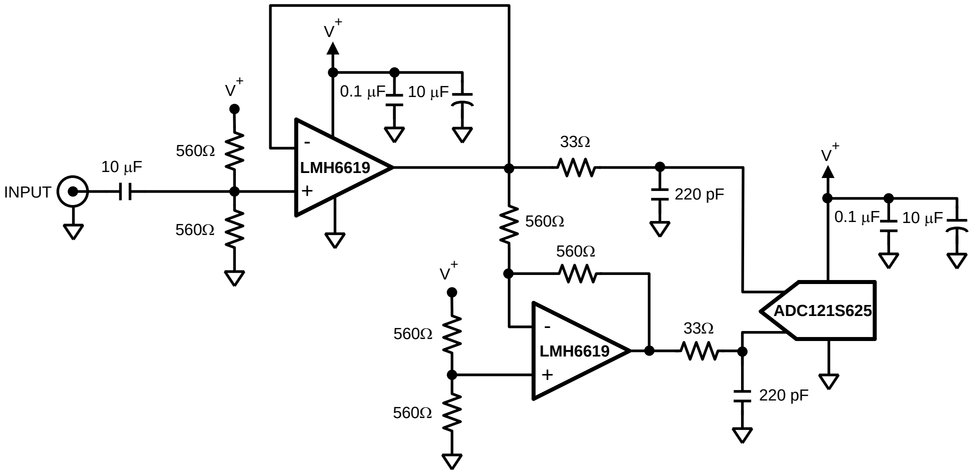

Figure 66. LMH6619 Driving an ADC121S625

Table 2. Performance Data for the LMH6619 Driving an ADC121S625

Parameter	Measured Value
Signal Frequency	10 kHz
Signal Amplitude	2.5V
SINAD	67.9 dB
SNR	68.29 dB
THD	−78.6 dB
SFDR	75.0 dB
ENOB	11.0 bits

DIFFERENTIAL ADC DRIVER

The circuit in Figure 64 can be used to drive both inputs of a differential ADC. Figure 67 shows the LMH6619 driving an ADC121S705. The ADC121S705 is a fully differential 12-bit ADC. Performance with this circuit is similar to the circuit in Figure 64.

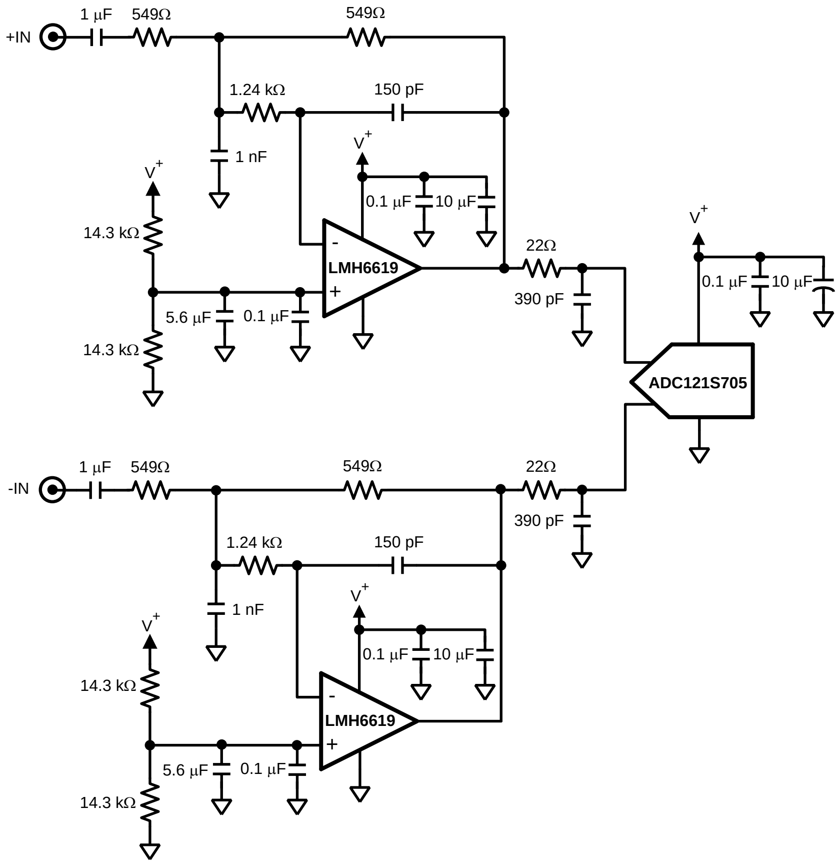

Figure 67. LMH6619 Driving an ADC121S705

DC LEVEL SHIFTING

Often a signal must be both amplified and level shifted while using a single supply for the op amp. The circuit in Figure 68 can do both of these tasks. The procedure for specifying the resistor values is as follows.

1. Determine the input voltage.
2. Calculate the input voltage midpoint, $V_{INMID} = V_{INMIN} + (V_{INMAX} – V_{INMIN})/2$.
3. Determine the output voltage needed.
4. Calculate the output voltage midpoint, $V_{OUTMID} = V_{OUTMIN} + (V_{OUTMAX} – V_{OUTMIN})/2$.
5. Calculate the gain needed, gain = $(V_{OUTMAX} – V_{OUTMIN})/(V_{INMAX} – V_{INMIN})$
6. Calculate the amount the voltage needs to be shifted from input to output, $\Delta V_{OUT} = V_{OUTMID}$ – gain x V_{INMID}.
7. Set the supply voltage to be used.
8. Calculate the noise gain, noise gain = gain + $\Delta V_{OUT}/V_S$.
9. Set R_F.
10. Calculate R_1, $R_1 = R_F$/gain.
11. Calculate R_2, $R_2 = R_F$/(noise gain-gain).
12. Calculate R_G, $R_G = R_F$/(noise gain – 1).

Check that both the V_{IN} and V_{OUT} are within the voltage ranges of the LMH6618.

The following example is for a V_{IN} of 0V to 1V with a V_{OUT} of 2V to 4V.

1. V_{IN} = 0V to 1V
2. V_{INMID} = 0V + (1V – 0V)/2 = 0.5V
3. V_{OUT} = 2V to 4V

4. V_{OUTMID} = 2V + (4V – 2V)/2 = 3V
5. Gain = (4V – 2V)/(1V – 0V) = 2
6. ΔV_{OUT} = 3V – 2 x 0.5V = 2
7. For the example the supply voltage will be +5V.
8. Noise gain = 2 + 2/5V = 2.4
9. R_F = 2 kΩ
10. R_1 = 2 kΩ/2 = 1 kΩ
11. R_2 = 2 kΩ/(2.4-2) = 5 kΩ
12. R_G = 2 kΩ/(2.4 – 1) = 1.43 kΩ

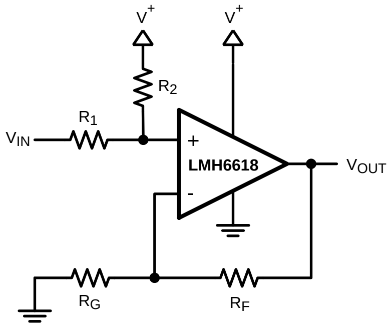

Figure 68. DC Level Shifting

4th ORDER MULTIPLE FEEDBACK LOW-PASS FILTER

Figure 69 shows the LMH6619 used as the amplifier in a multiple feedback low pass filter. This filter is set up to have a gain of +1 and a −3 dB point of 1 MHz. Values can be determined by using the WEBENCH® Active Filter Designer found at webench.ti.com.

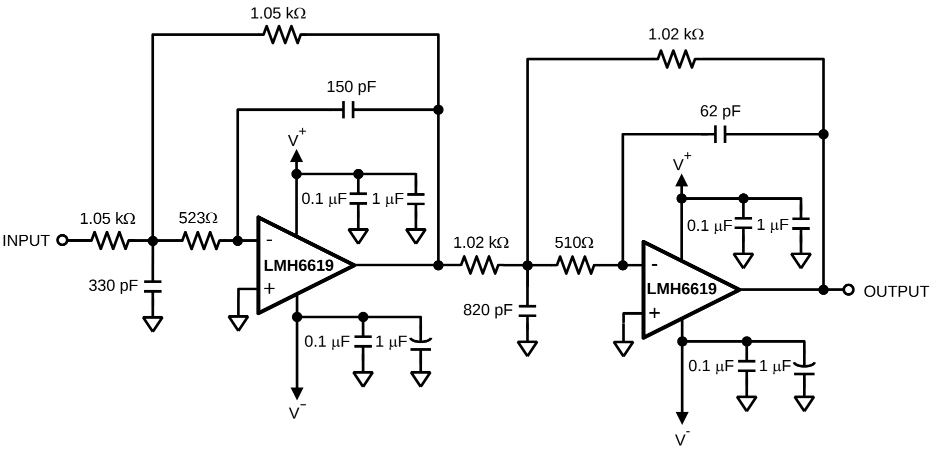

Figure 69. 4th Order Multiple Feedback Low-Pass Filter

CURRENT SENSE AMPLIFIER

With it's rail-to-rail input and output capability, low V_{OS}, and low I_B the LMH6618 is an ideal choice for a current sense amplifier application. Figure 70 shows the schematic of the LMH6618 set up in a low-side sense configuration which provides a conversion gain of 2V/A. Voltage error due to V_{OS} can be calculated to be V_{OS} x (1 + R_F/R_G) or 0.75 mV x 20.6 = 15.5 mV. Voltage error due to I_O is I_O x R_F or 0.26 µA x 1 kΩ = 0.26 mV. Hence total voltage error is 15.5 mV + 0.26 mV or 15.7 mV which translates into a current error of 15.7 mV/(2 V/A) = 7.9 mA.

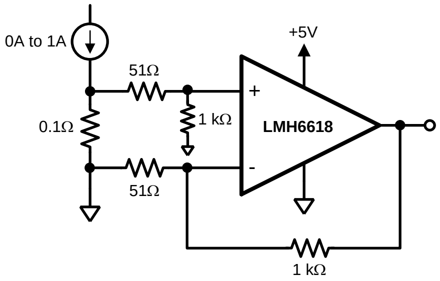

Figure 70. Current Sense Amplifier

TRANSIMPEDANCE AMPLIFIER

By definition, a photodiode produces either a current or voltage output from exposure to a light source. A Transimpedance Amplifier (TIA) is utilized to convert this low-level current to a usable voltage signal. The TIA often will need to be compensated to insure proper operation.

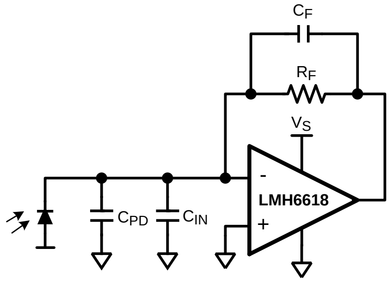

Figure 71. Photodiode Modeled with Capacitance Elements

Figure 71 shows the LMH6618 modeled with photodiode and the internal op amp capacitances. The LMH6618 allows circuit operation of a low intensity light due to its low input bias current by using larger values of gain (R_F). The total capacitance (C_T) on the inverting terminal of the op amp includes the photodiode capacitance (C_{PD}) and the input capacitance of the op amp (C_{IN}). This total capacitance (C_T) plays an important role in the stability of the circuit. The noise gain of this circuit determines the stability and is defined by:

$$NG = \frac{1 + sR_F\,(C_T + C_F)}{1 + sC_FR_F} \tag{1}$$

$$\text{Where, } f_Z \cong \frac{1}{2\pi R_F C_T} \text{ and } f_P = \frac{1}{2\pi R_F C_F} \tag{2}$$

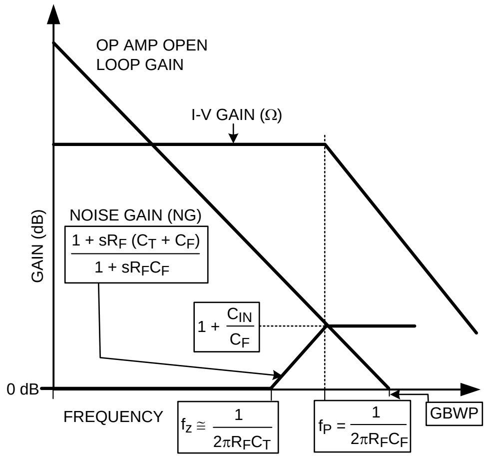

Figure 72. Bode Plot of Noise Gain Intersecting with Op Amp Open-Loop Gain

Figure 72 shows the bode plot of the noise gain intersecting the op amp open loop gain. With larger values of gain, C_T and R_F create a zero in the transfer function. At higher frequencies the circuit can become unstable due to excess phase shift around the loop.

A pole at f_P in the noise gain function is created by placing a feedback capacitor (C_F) across R_F. The noise gain slope is flattened by choosing an appropriate value of C_F for optimum performance.

Theoretical expressions for calculating the optimum value of C_F and the expected −3 dB bandwidth are:

$$C_F = \sqrt{\frac{C_T}{2\pi R_F (GBWP)}} \tag{3}$$

$$f_{-3\ dB} = \sqrt{\frac{GBWP}{2\pi R_F C_T}} \tag{4}$$

Equation 4 indicates that the −3 dB bandwidth of the TIA is inversely proportional to the feedback resistor. Therefore, if the bandwidth is important then the best approach would be to have a moderate transimpedance gain stage followed by a broadband voltage gain stage.

Table 3 shows the measurement results of the LMH6618 with different photodiodes having various capacitances (C_{PD}) and a feedback resistance (R_F) of 1 kΩ.

Table 3. TIA (Figure 1) Compensation and Performance Results

C_{PD}	C_T	$C_{F\ CAL}$	$C_{F\ USED}$	$f_{-3\ dB\ CAL}$	$f_{-3\ dB\ MEAS}$	Peaking
(pF)	(pF)	(pF)	(pF)	(MHz)	(MHz)	(dB)
22	24	7.7	5.6	23.7	20	0.9
47	49	10.9	10	16.6	15.2	0.8
100	102	15.8	15	11.5	10.8	0.9
222	224	23.4	18	7.81	8	2.9

Figure 73 shows the frequency response for the various photodiodes in Table 3.

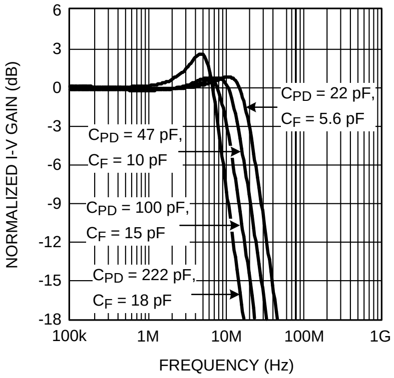

Figure 73. Frequency Response for Various Photodiode and Feedback Capacitors

When analyzing the noise at the output of the TIA, it is important to note that the various noise sources (i.e. op amp noise voltage, feedback resistor thermal noise, input noise current, photodiode noise current) do not all operate over the same frequency band. Therefore, when the noise at the output is calculated, this should be taken into account. The op amp noise voltage will be gained up in the region between the noise gain's zero and pole (f_Z and f_P in Figure 72). The higher the values of R_F and C_T, the sooner the noise gain peaking starts and therefore its contribution to the total output noise will be larger. It is obvious to note that it is advantageous to minimize C_{IN} by proper choice of op amp or by applying a reverse bias across the diode at the expense of excess dark current and noise.

DIFFERENTIAL CABLE DRIVER FOR NTSC VIDEO

The LMH6618 and LMH6619 can be used to drive an NTSC video signal on a twisted-pair cable. Figure 74 shows the schematic of a differential cable driver for NTSC video. This circuit can be used to transmit the signal from a camera over a twisted pair to a monitor or display located a distance. C_1 and C_2 are used to AC couple the video signal into the LMH6619. The two amplifiers of the LMH6619 are set to a gain of 2 to compensate for the 75Ω back termination resistors on the outputs. The LMH6618 is set to a gain of 1. Because of the DC bias the output of the LMH6618 is AC coupled. Most monitors and displays will accept AC coupled inputs.

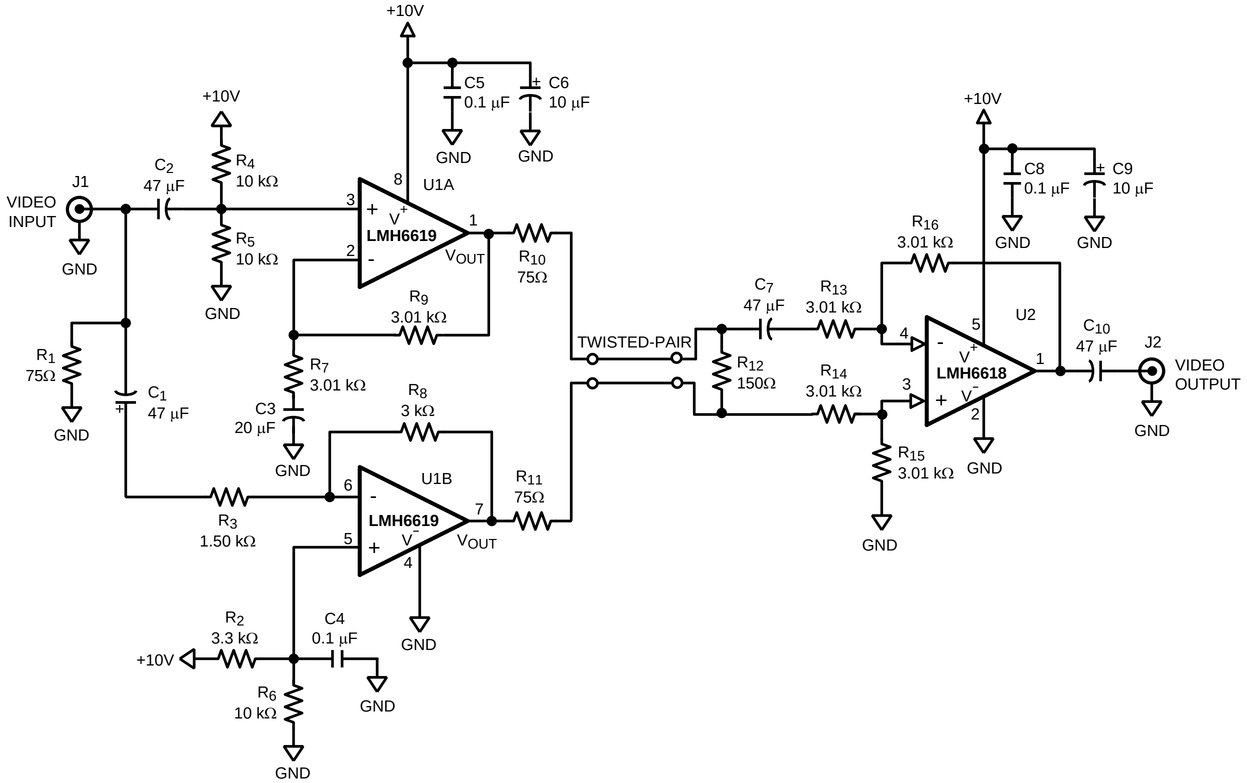

Figure 74. Differential Cable Driver

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6618MK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AE4A	Samples
LMH6618MKE/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AE4A	Samples
LMH6618MKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AE4A	Samples
LMH6619MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMH66 19MA	Samples
LMH6619MAE/NOPB	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMH66 19MA	Samples
LMH6619MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMH66 19MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMH6619 :

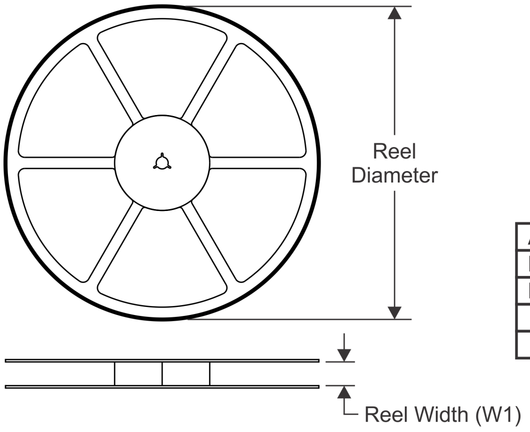
- Automotive: LMH6619-Q1

NOTE: Qualified Version Definitions:

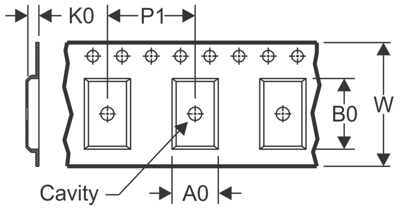
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

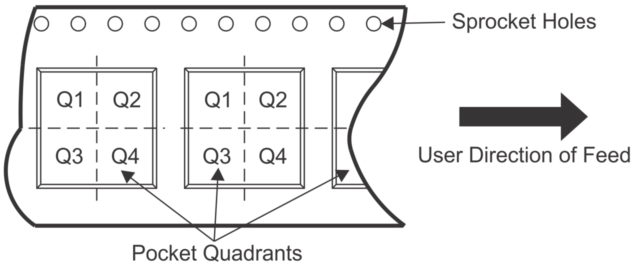


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

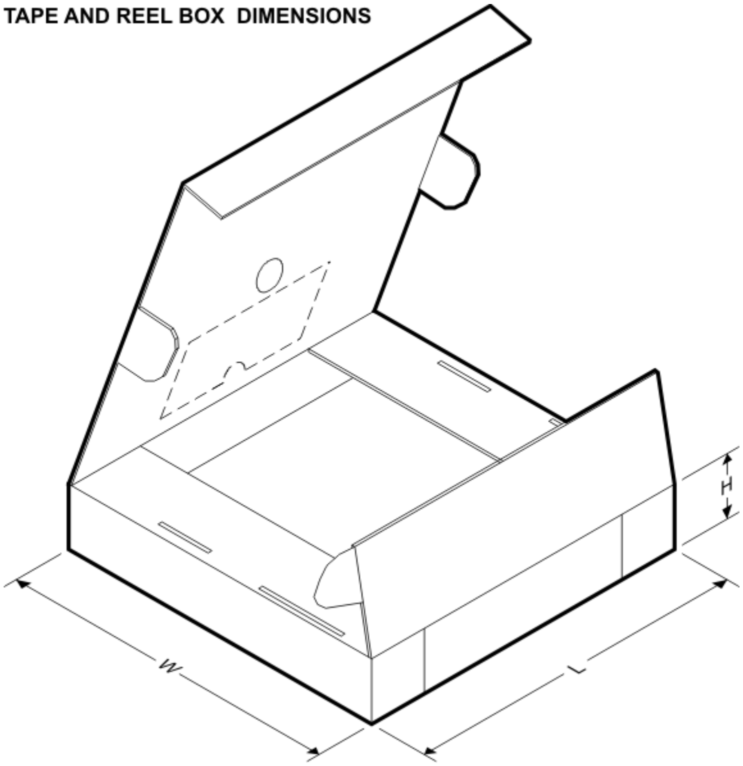
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6618MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6618MKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6618MKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6619MAE/NOPB	SOIC	D	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6619MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

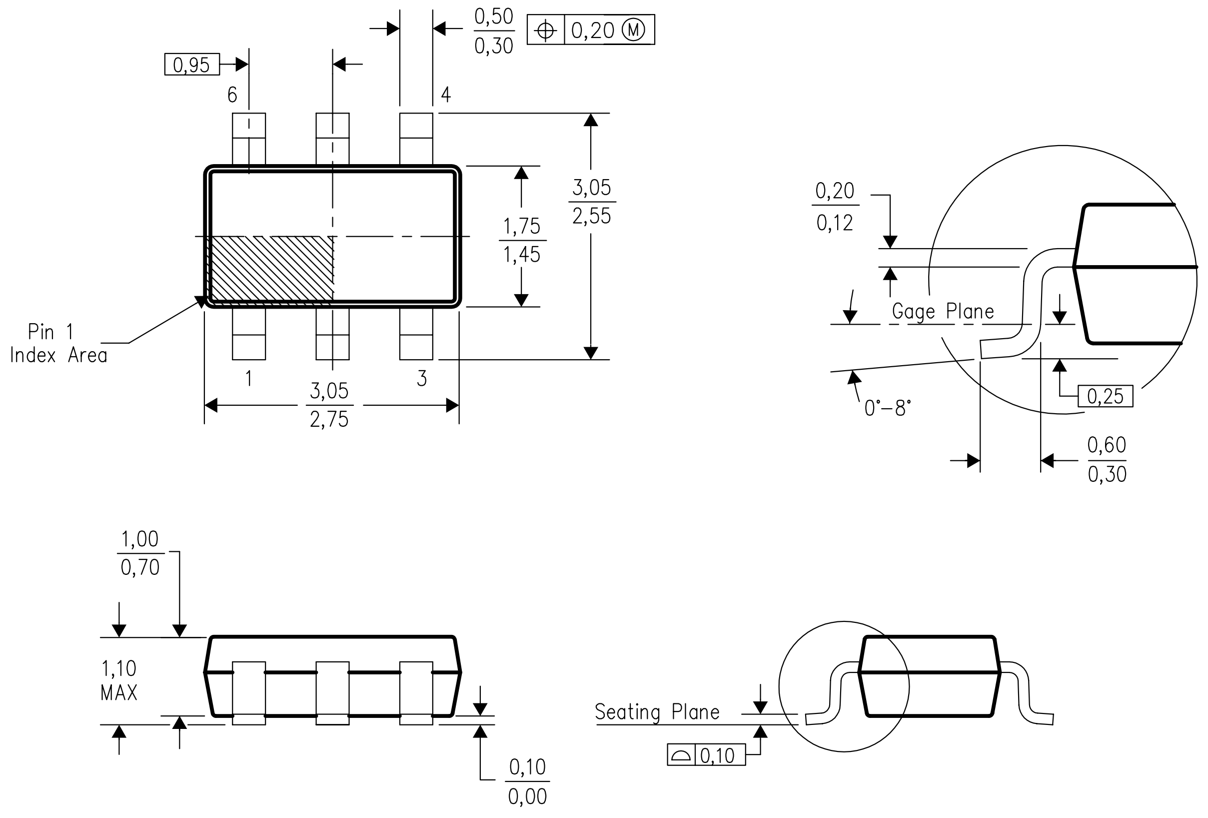
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6618MK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMH6618MKE/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMH6618MKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMH6619MAE/NOPB	SOIC	D	8	250	210.0	185.0	35.0
LMH6619MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

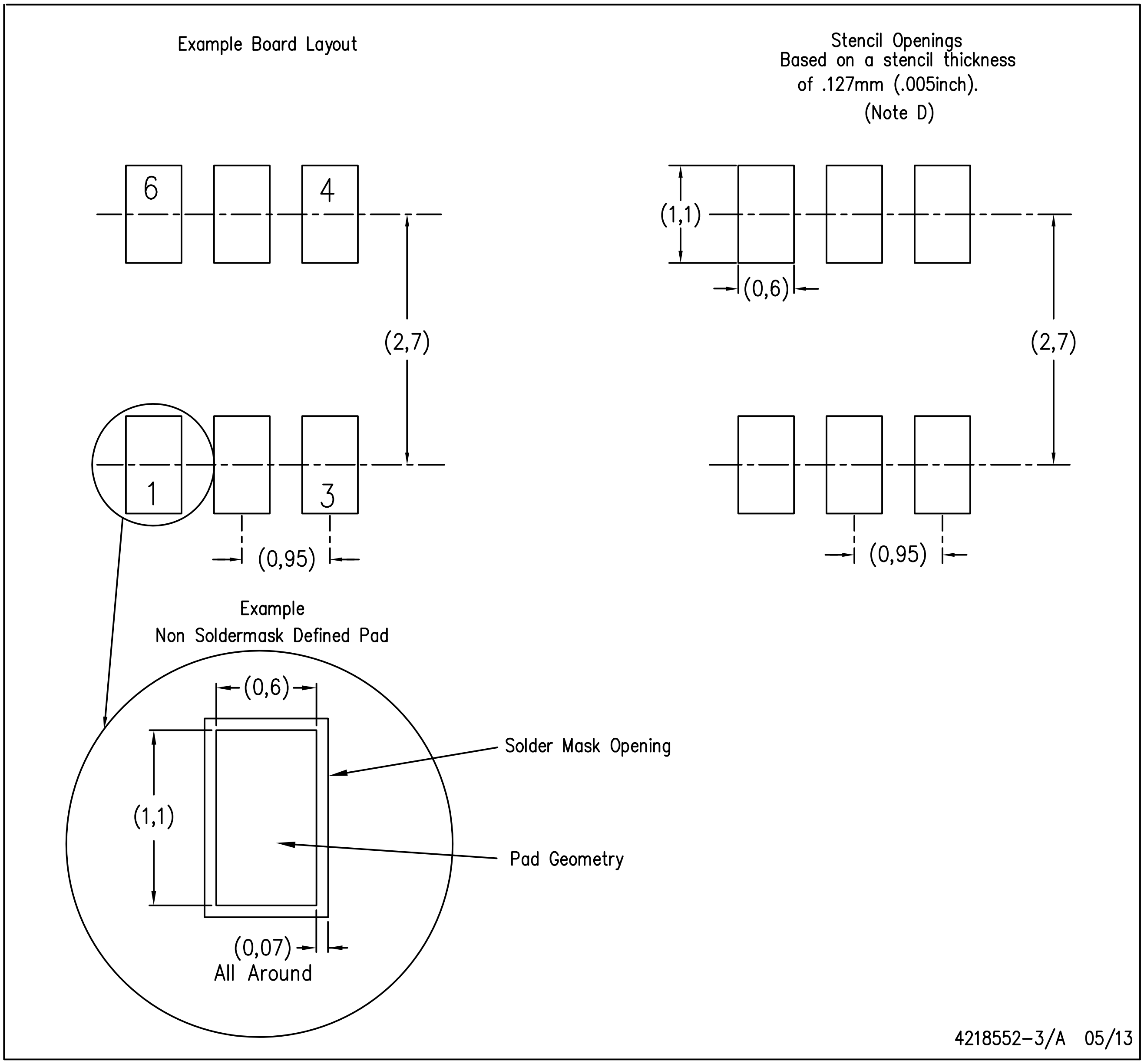
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–193 variation AA (6 pin).

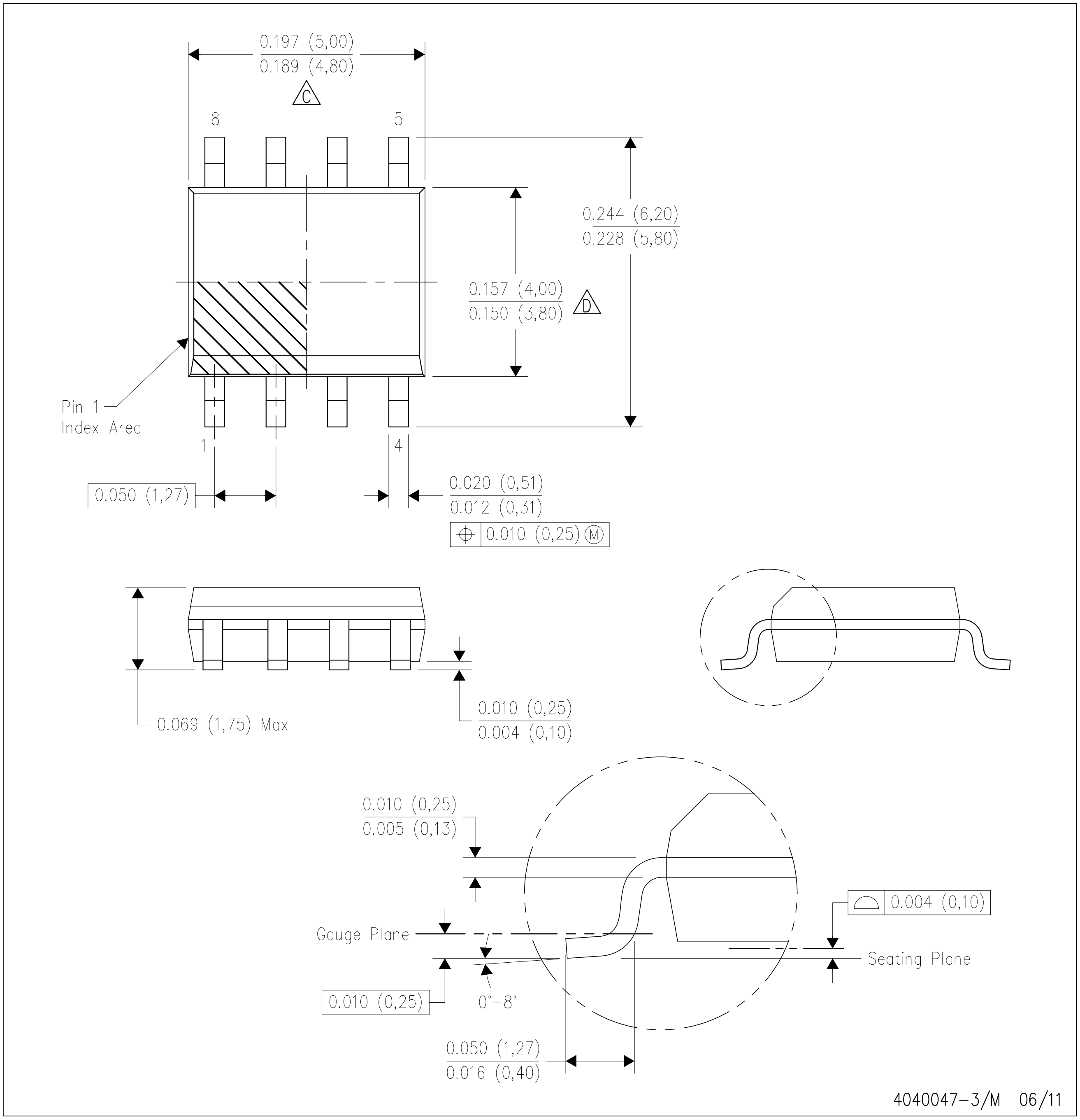
DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



4218552–3/A 05/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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