ELECTRONIC CIRCUIT

EG4002 Datasheet

PIR Controller

REV 1.0

Contents

EG4002 Datasheet V1.0

1. Features

- 8-Pin SOP8/DIP8 Packaging
- Minimal Peripheral Components Required
- Low Supply Current：45uA @VDD=3V and 75uA @VDD=5V
- Built-in 2-stage Operational Amplifier
- Built-in Fixed-gain 30x in 2nd Stage OP amp
- Built-in Window Comparator for Two Independent Voltage Monitors
- Built-in Internal Reference Voltages for OP amps and Comparators
- Provide Adjustable Turn on Delay Timer and Stable Timer
- Wider supply voltage:+3V～+6Vdc

2. General Description

The EG4002 IC is a PIR controller, using analog mixing digital designed by CMOS process, The EG4002 contains two operational amplifiers, window comparator, voltage reference, turn on delay timer and stable timer, and digital state controller, dedicated to Alarm system, Auto door system, and LED light controller etc.

The EG4002 is available in an 8-Pin SOP/DIP the necessary features to implement PIR control schemes with a minimal external parts count, which can reduce the material cost and save the PCB board space.

3. Applications

- PIR Alarm System
- Automatic Dryer
- PIR Sensor Door Bell
- PIR Light Controller
- LED Microwave Radar Light Controller
- Auto Door System

4. Device Information

4.1. Pin map

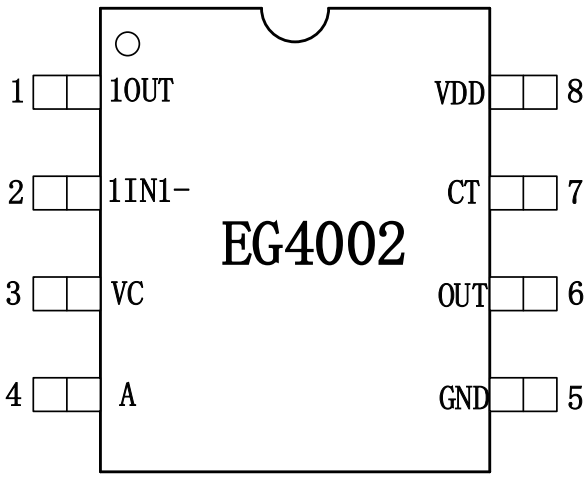


Figure 4.1 EG4002 pin map

4.2. Pin Functions

Designator	Name	I/O	Descriptions
1	1OUT	O	First stage OP amp output.
2	1IN-	I	First stage OP amp negative input.
3	VC	I	Enable/Disable trigger function for photo resistor input: ● Disable the sensor function when voltage of VC pin is lower than 0.2VDD, and OUT pin is always to low level ● Enable the sensor function when voltage of VC pin is higher than 0.2VDD.
4	A	I	Trigger mode selection for single trigger or auto trigger input: ● It's in auto trigger mode when voltage of A pin is higher than 0.7VDD. ● It's in single trigger mode when voltage of A pin is lower than 0.2VDD.
5	GND	I	Device ground reference.
6	OUT	O	Output, active high ● Sink current:10 mA max @VDD=3V and 25 mA max @VDD=5V ● Source current:10 mA max @VDD=3V and 25 mA max @VDD=5V
7	CT	I	Oscillator timing capacitor input
8	VDD	I	Supply voltage: +3V～+6Vdc.

5. Block Diagram

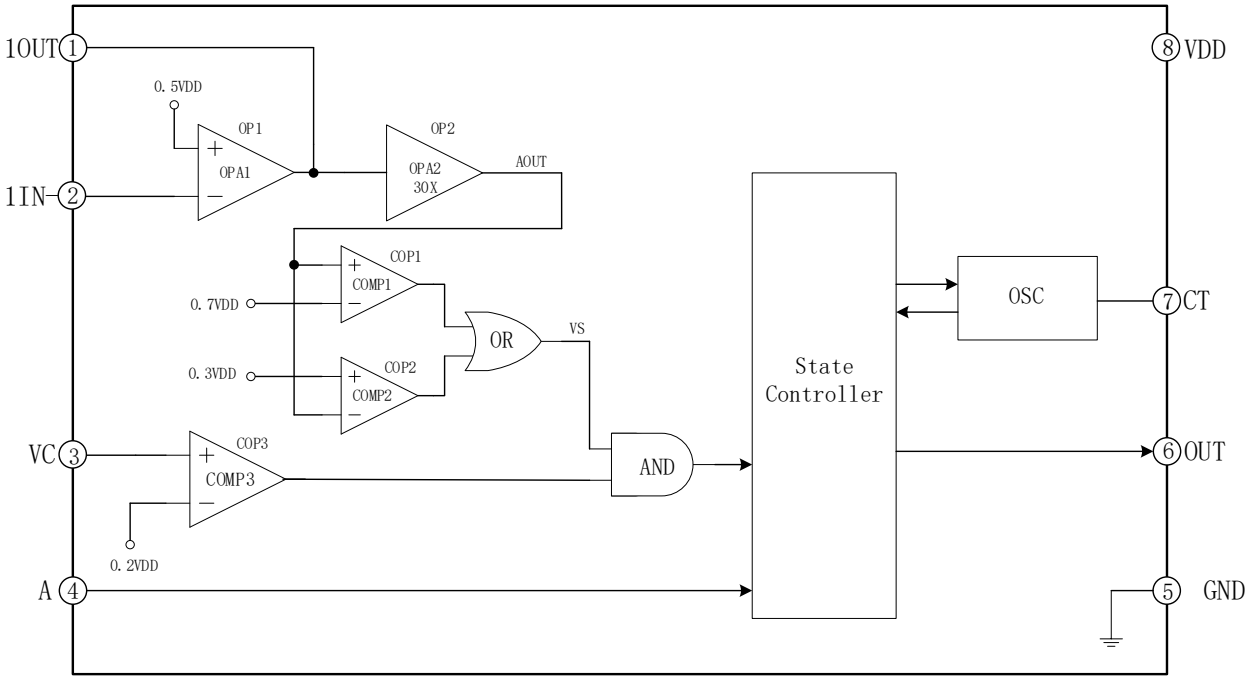


Figure 5.1EG4002 block diagram

6. Application Schematics

6.1 EG4002 Typical Application Schematic

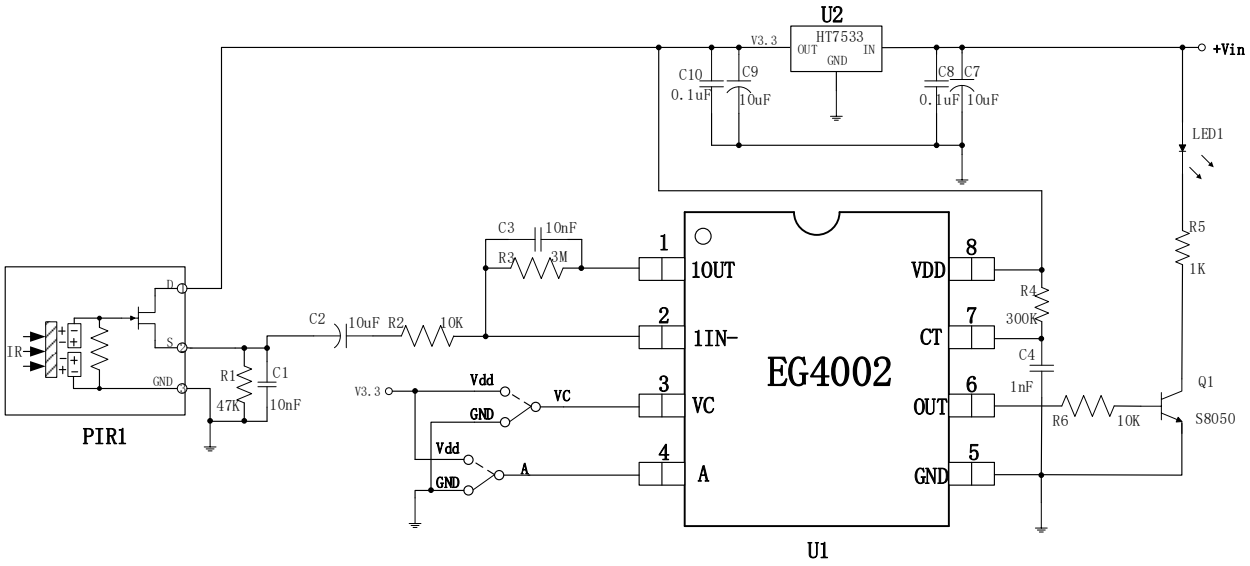


Figure 6.1a EG4002 typical application schematic

6.2 EG4002 Application Schematic to Drive Relay

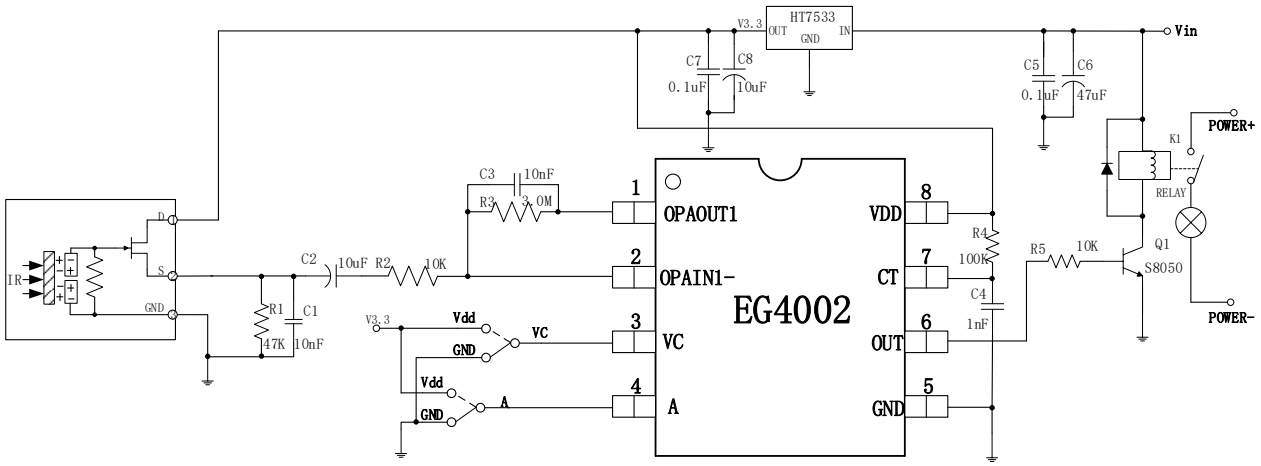


Figure 6.1b EG4002 application schematic to drive relay

6.3 EG4002 Application Schematic in Auto Trigger and CDS detector

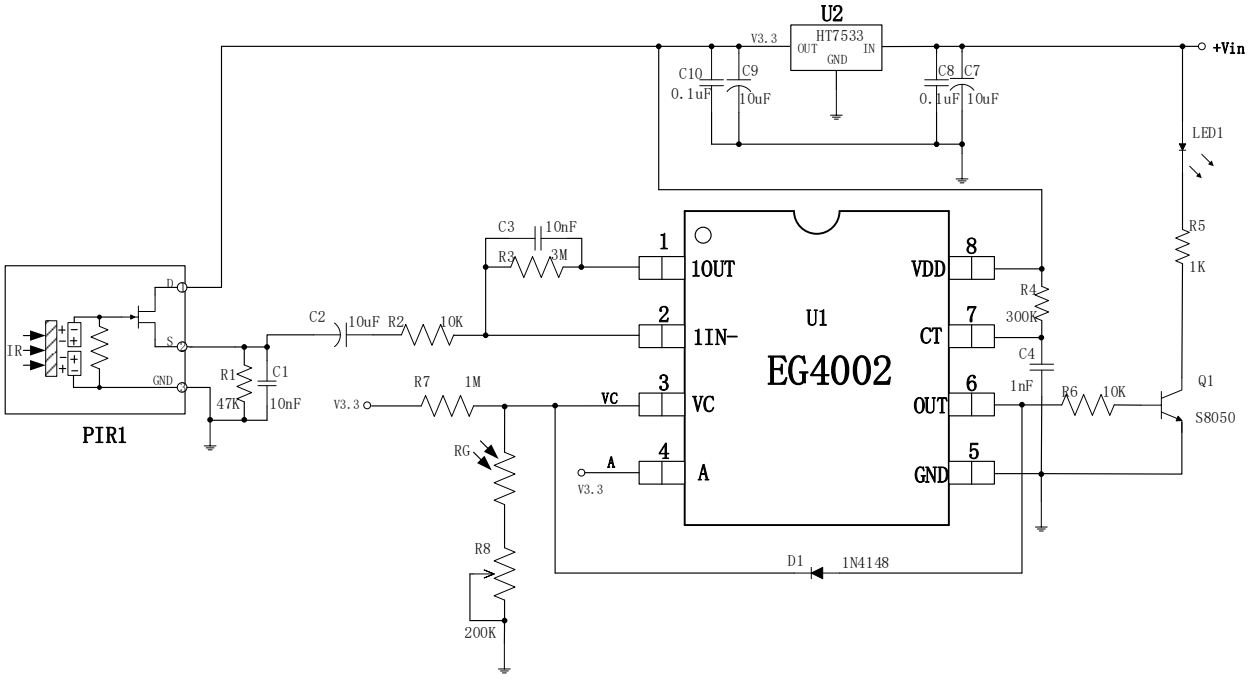


Figure 6.1c EG4002 application schematic in auto trigger and CDS detector

7. Electrical Characteristics

7.1 Absolute maximum ratings

TA=25℃ unless otherwise specified

Symbol	Ratings	Conditions	Min	Max	Unit
VDD	Supply voltage	Respect to the GND	-0.3	7	V
OUT	Output	Respect to the GND	-0.3	7	V
CT	Timing RC input	Respect to the GND	-0.3	7	V
A	Trigger mode selection	Respect to the GND	-0.3	7	V
VC	Enable/Disable Trigger	Respect to the GND	-0.3	7	V
1IN-	First stage OP amp negative input	Respect to the GND	-0.3	7	V
1OUT	First stage OP amp output	Respect to the GND	-0.3	7	V
TA	Ambient temperature	-	-45	85	℃
Tstr	Storage temperature	-	-65	125	℃
TL	Lead temperature	Soldering, T=10S	-	300	℃

Note：Exceeding extreme conditions may permanently damage the chip. EG4002's reliability may be affected running at the extreme conditions for a long time.

7.2 Recommended operating conditions

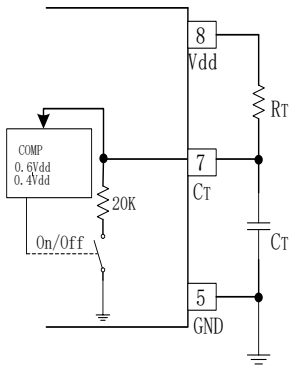
TA=25℃ unless otherwise specified

Symbol	Ratings	Conditions	Min	Typ	Max	Unit
VDD	Operating Range	-	3	-	6	V
Icc	Operating Supply Current	Vdd=5V	-	65	75	uA
		Vdd=3V	-	35	45	uA
Vos	Input Offset Voltage	Vdd=5V	-	2	5	mV
Ios	Input Offset Current	Vdd=5V	-	-	50	nA
Avo	Voltage Gain	Open loop	60	-	-	dB
V_{OPAH}	Output Voltage High for OP Amp	Vdd=5V, I_{LOAD}=5uA	4.5	4.85	-	V
V_{OPAL}	Output Voltage Low for OP Amp	Vdd=5V, I_{LOAD}=-5uA	-	-	0.1	V
V_{CH}	Enable Threshold for VC	Vdd=5V	1.0	-	-	V
		Vdd=3V	0.6	-	-	V
V_{CL}	Disable Threshold for VC	Vdd=5V	-	-	0.9	V
		Vdd=3V	-	-	0.5	V
V_{OH}	Output Voltage High for OUT	Vdd=5V, I_{LOAD}=10mA	4.5	4.6	-	V
		Vdd=3V, I_{LOAD}=5mA	2.5	2.6	-	V
V_{OL}	Output Voltage Low for OUT	Vdd=5V, I_{LOAD}=-10mA	-	0.3	0.5	V
		Vdd=3V, I_{LOAD}=-5mA	-	0.3	0.5	V
V_{AH}	Auto Trigger Mode for A	Vdd=5V	3.5	5	-	V
		Vdd=3V	2	3	-	V
V_{AL}	Single Trigger Mode for A	Vdd=5V	-	0	1	V
		Vdd=3V	-	0	0.5	V

8. Functional Description

8.1 Oscillator

The oscillator frequency is programmed by the values selected for the timing components RT and CT shown in Figure8.1a. The capacitor CT is charged from the VDD through resistor RT to approximately 0.6Vdd and discharged to 0.4Vdd by an internal 20KΩ pull-down resistor.



The approximately oscillator frequency is determined by: $Tosc=0.4R_TC_T\frac{RT}{RT-20K}$

(Here resistor unit is KΩ, capacitor is nF, Tosc is uS), and f=1/Tosc. For example, R_T=100K, C_T=1nF, Tosc=0.4*100*1*1.25=50uS, f=1/T=20KHz. When choosing the pull-up resistor RT, the resistance must be greater than 100K or more.

Figure 8.1a oscillator frequency setting

8.2 Turn on delay timer and Stable timer

The turn on delay timer of EG4002 is defined to Tx，stable timer is defined to Ti，the ratio-coefficient of Tx and Ti is defined to K，K= $\frac{Tx}{Ti}$. For adapt to more applications, the EG4002 has different K values, and the suffix in the EG4002 product model is distinguished, as shown in table 8.2.

Table 8.2

Model	Tx	Ti	K
EG4002A	100000xTosc	20000xTosc	5
EG4002B	100000xTosc	10000 xTosc	10
EG4002C	100000 xTosc	7000 xTosc	14
EG4002D	100000 xTosc	5000 xTosc	20
EG4002E	100000 xTosc	4000 xTosc	25
EG4002F	100000 x Tosc	3000 xTosc	33
EG4002G	100000 x Tosc	2000 xTosc	50

The turn on delay timer is used for setting up the timing of how long OUT pin is active, the timing time of Tx is equals to 100000 Tosc clock cycles, Tx time as shown in Figure8.2a.

The stable timer is used for trigger blocking after Tx time out, OUT pin is output low level during trigger blocking as shown in Figure8.2a, the timing time of Ti is shown in table 8.2.

The total timing time is T=Tx+Ti, for example using EG4002A,choosing Tosc=50uS, then Tx=100000*50uS=5S,Ti=20000*50uS=1S as table8.2, total timing time is T=6S。

When setting Tx is less than 15S, suggested the use of a K=5 of EG4002A product, which is to obtain better stable time for filter the load switching.

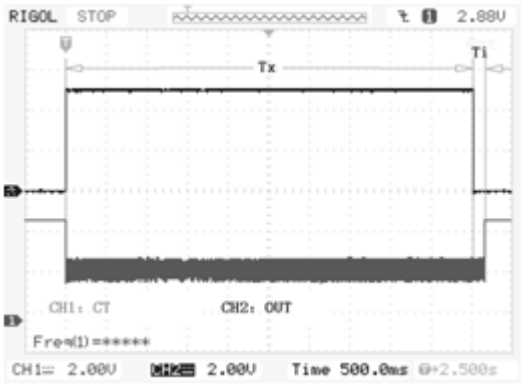
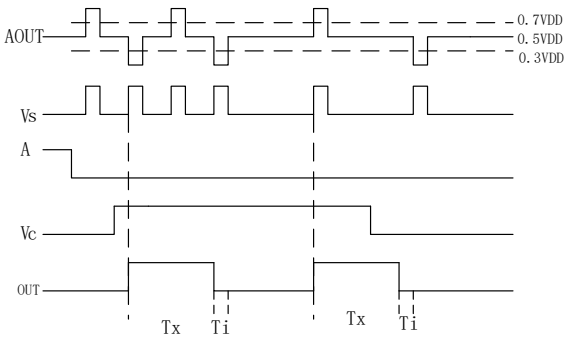


Figure 8.2a turn on delay timer Tx and stable timer Ti

8.3 Single Trigger and Auto Trigger on A pin

When A pin input is lower than 0.2VDD, EG4002 is working in single trigger mode. As Figure 8.3a, if Vc input is valid, the first rising edge of Vs will make the OUT to high level output, chip enters Tx delay timing and Ti blocking timing stage, in this Tx stage, the Vs signal will be invalid until Tx and Ti time out.

When A pin input is higher than 0.7VDD, EG4002 is working in auto trigger mode. As Figure 8.3b, if Vc input is valid, the first rising edge of Vs will make the OUT to high level output, chip enters Tx delay timing, in this Tx stage, the Tx delay time will be recount when Vs signal is trigged again, until Tx time out, chip enters Ti blocking time stage.



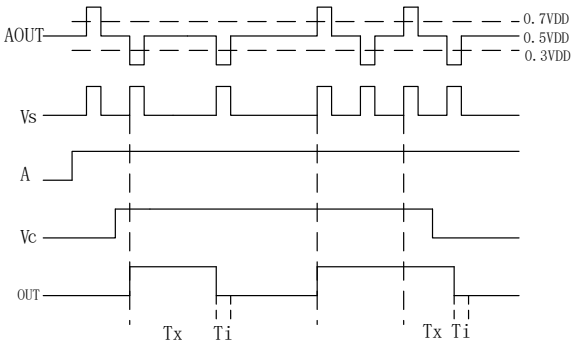


Figure 8.3a single trigger timing diagram Figure 8.3b auto trigger timing diagram

8.4 Enable/Disable Trigger Function on Vc pin

When Vc pin input is lower than 0.2VDD, EG4002 disable the PIR sensor function, and OUT pin is always to low level.

When Vc pin input is higher than 0.2VDD, EG4002 enable the PIR sensor function, OUT pin will be controlled by Vs trigger signal as shown in Figure8.3a and Figure8.3b.

A photo resistor can be applied to Vc pin for light and dark activated detector circuits.

8.5 OP amp Gain Setting

The gain of first stage OP amp is determined by R2 and R3, the second stage OP amp is fixed gain of 30 times, as shown in figure 8.5a, the total gain is A=A1 x A2. In figure8.5a configuration, the A1=R3/R2=(3*10^6)/(10*10^3)=300,A2=30, A=A1 x A2=300 x30=9000.By adjusting the gain, the PIR distance of detection can be changed. Here C2 is DC-blocking capacitor.

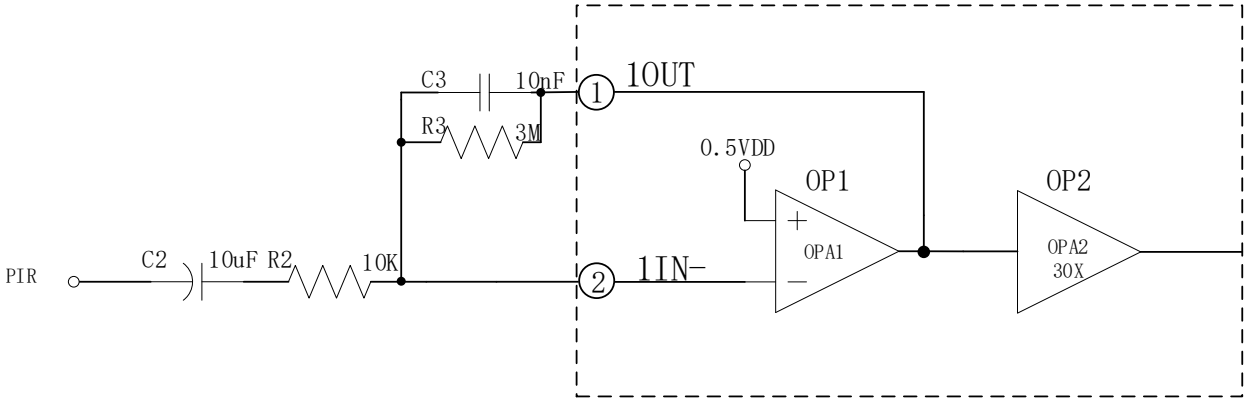
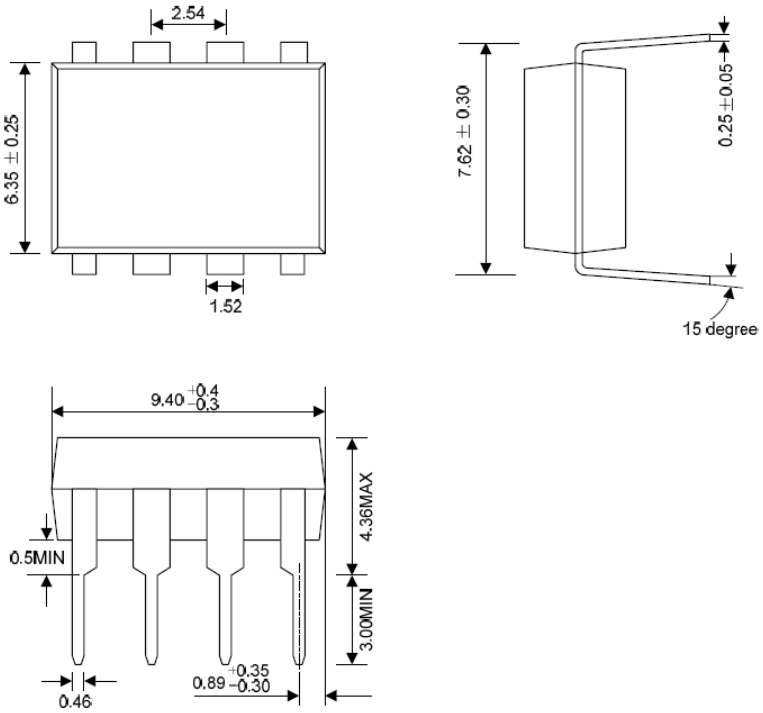


Figure 8.5a EG4002 OP amp gain setting

9. Package Information

9.1 DIP8 Dimension



9.2 SOP8 Dimension