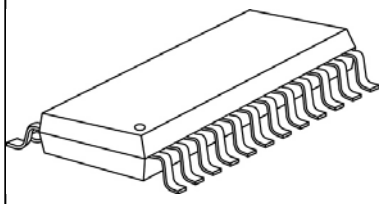
16-Channel Constant Current LED Sink Driver with Compulsory Open-circuit Detection and Current Gain

Features

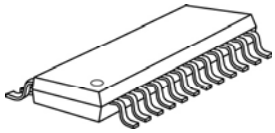
- 16 constant-current output channels
  Constant output current range: 3~45mA
  - 3-45mA @ 5V supply voltage
  - 3-30mA @ 3.3V supply voltage
- Compulsory LED open-circuit detection
  - Open-circuit LEDs can be detected
  - Full panel, data independent
  - Flicker-free error detection
- 64-step programmable current gain: from 12.5% to 200%
- Excellent output current accuracy,
  - Between channels: <±1.5% (typ.), and
  - Between ICs: <±3% (typ.)
- Fast response of output current
  - Min. output pulse width of $\overline{OE}$: 20ns
- Staggered delay of output, preventing from current surge
- 30MHz clock frequency
- Schmitt trigger input

Small Outline Package



GF: SOP24L-300-1.00

Shrink SOP



GP: SSOP24L-150-0.64

Product Description

MBI5034 is an enhanced 16-channel constant current LED sink driver with smart error detection and output current gain. MBI5034 succeeds MBI5026 and also exploits **PrecisionDrive™** technology to enhance the output characteristics. Furthermore, MBI5034 adopts **Share-I-O™** technology to be backward compatible with MBI5026, MBI5036 and MBI5039 in pin definition and has the functionality for compulsory LED open-circuit detection and current gain control in LED display systems.

MBI5034 contains a 16-bit shift register and a 16-bit output latch, which convert serial input data into parallel output format. At MBI5034 output stages, sixteen regulated current ports are designed to provide uniform and constant current sinks with small skew between ports for driving LEDs within a wide range of forward voltage (V_F) variations. Users may adjust the output current from 3mA to 45mA with an external resistor R_{ext}, which provides users flexibility in controlling the light intensity of LEDs. MBI5034 guarantees to endure maximum 17V at the output ports. Besides, the high clock frequency, up to 30MHz, also satisfies the system requirements of high volume data transmission.

With the open-circuit detection, MBI5034 can detect individual LED open-circuit error without extra components. Once the dedicated command is issued, all of the output ports will be turned on with small current. Since the turn-on duration and current are so small, the flicker will not be sensed by human eyes and the image quality will not be impacted. All of the channels are detected no matter the input data is zero or one.

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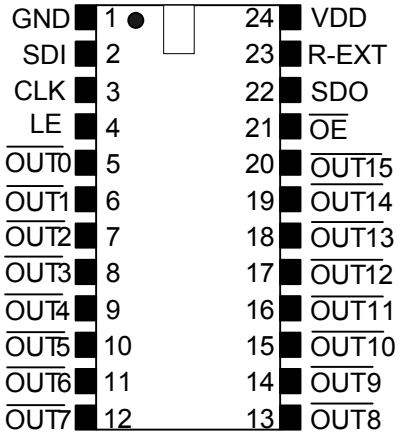
In addition, MBI5034 also allows users to adjust the output current level by setting a programmable configuration code. The code is sent into MBI5034 via the pin SDI. The falling edge of LE would latch the code in the shift register into a built-in 16-bit configuration register, instead of the output latch. The gain code would affect the voltage at the terminal R-EXT and control the output current regulator. The output current can be adjusted finely by a gain ranging from 12.5% to 200% in 64 steps.

With the **Share-I-O™** technique, MBI5034 could be a drop-in replacement of predecessors. The printed circuit board originally designed for MBI5026/36/39 may be also applied to MBI5034 only that the controllers have to be upgraded and $\overline{OE}$ needs to be controllable.

Pin Configuration

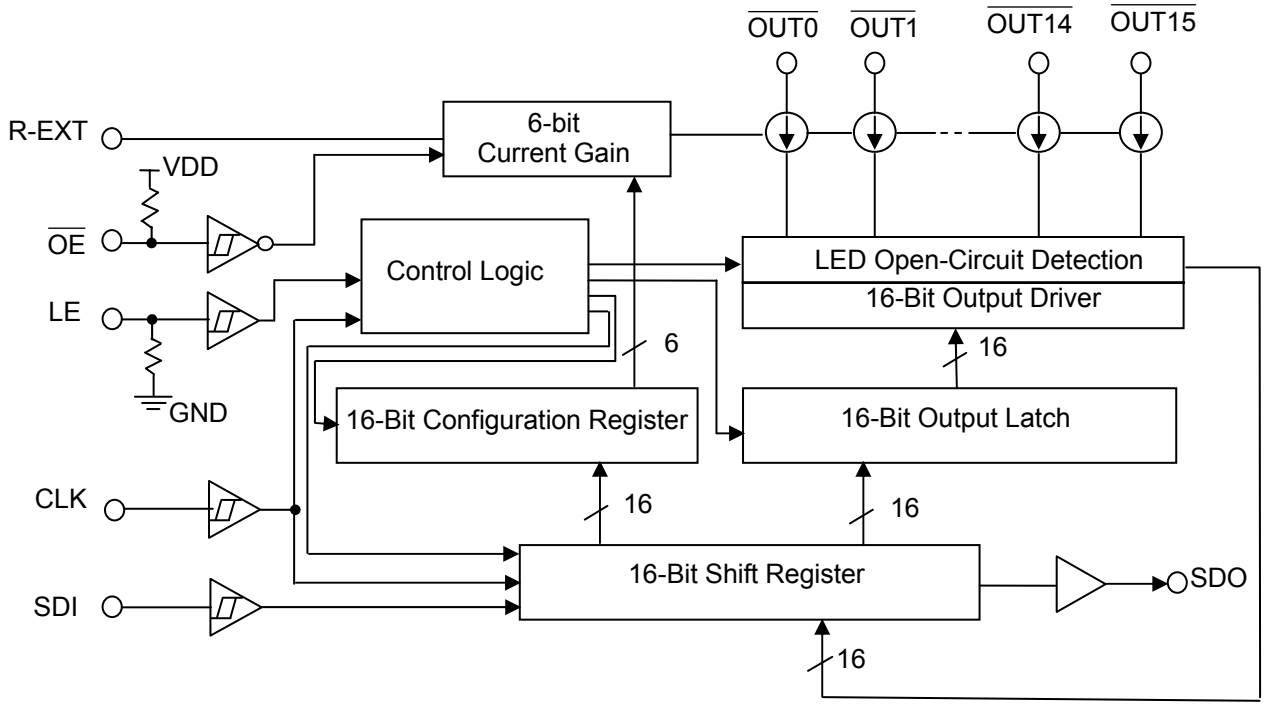


MBI5034GF/GP
Top View

Terminal Description

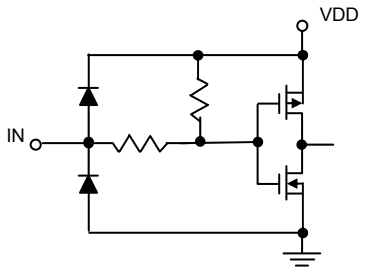
Pin Name	Function
GND	Ground terminal for control logic and current sinks
SDI	Serial-data input to the shift register
CLK	Clock input terminal used to shift data on rising edge and carry command information when LE is asserted.
LE	Data strobe terminal and asserting command with adequate CLK pulses
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
$\overline{OE}$	Enable output drivers to sink current. Internal pulled-high. When its level is low (active), the output drivers are enabled; when high, all output drivers are turned OFF (blank). The signal is used for error detection. Please refer to error detection sections for further details.
SDO	Serial-data output to the SDI of the following driver IC
R-EXT	Input terminal used for connecting an external resistor in order to set up the current level of all output ports
VDD	3.3/5V supply voltage terminal

Block Diagram

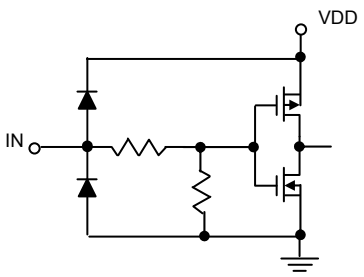


Equivalent Circuits of Inputs and Outputs

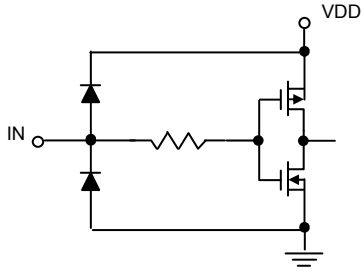
$\overline{OE}$ terminal



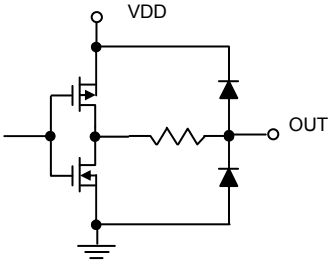
LE terminal



CLK, SDI terminal



SDO terminal



Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7.0	V
Input Pin Voltage (SDI, $\overline{OE}$, LE, CLK)		V_{IN}	-0.4 to VDD+0.4	V
Sustaining Voltage at SDO Pin		V_{OUT}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at $\overline{OUTn}$ Pins		V_{DS}	-0.5~+17	V
Output Current ($\overline{OUT0}$ ~ $\overline{OUT15}$)		I_{OUT}	+45	mA
GND Terminal Current		I_{GND}	+720	mA
Power Dissipation (On 4 Layer PCB, Ta=25°C)*	GF Type	P_D	1.83	W
	GP Type		1.76	
Thermal Resistance (On 4 Layer PCB, Ta=25°C)*	GF Type	$R_{th(j-a)}$	68.44	°C/W
	GP Type		71.18	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	HBM (MIL-STD-883G Method 3015.7, Human Body Mode)	HBM	Class 3A (4000V~7999V)	-
	MM (JEDEC EIA/JESD22-A115, Machine Mode)	MM	Class B (200V~399V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested operation temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V; Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		3	-	45	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V and channel off		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=25mA V_{DS}=1.0V	R_{ext}=560Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=25mA V_{DS}=1.0V	R_{ext}=560Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=560Ω@25mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±0.5	±1.0	% / V
LED Open-Circuit Detection Threshold Voltage**		$V_{OD,TH}$	-		-	0.35	-	V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		250	450	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off,		-	2.5	5	mA
		I_{DD}(off) 2	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off,		-	6.0	10	
	"On"	I_{DD}(on) 1	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=On,		-	6.5	12	

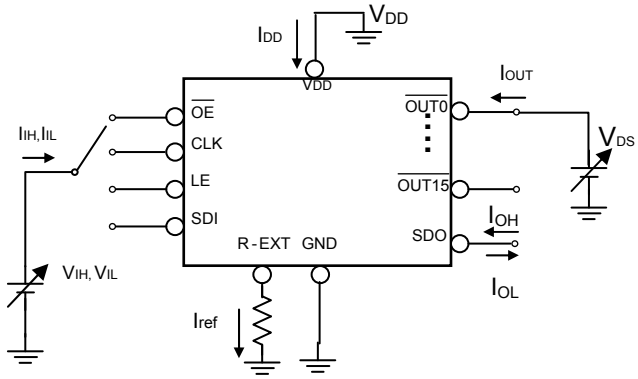
*One channel on.
**LED open-circuit detection threshold voltage ($V_{OD,TH}$) is a configurable voltage.

Electrical Characteristics (V_{DD}=3.3V; Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		3	-	30	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V and channel off		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=25mA V_{DS}=1.0V	R_{ext}=560Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=25mA V_{DS}=1.0V	R_{ext}=560Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=560Ω@25mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±0.5	±1.0	% / V
LED Open-Circuit Detection Threshold Voltage**		$V_{OD,TH}$	-		-	0.35	-	V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		250	450	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off,		-	2.0	4.5	mA
		I_{DD}(off) 2	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off,		-	5.5	10	
	"On"	I_{DD}(on) 1	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=On,		-	6.0	12	

*One channel on.
**LED open circuit detection threshold voltage ($V_{OD,TH}$) is a configurable voltage.

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}=5.0V; Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time (“L” to “H”)	LE-SDO	t_{pLH0}	V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω R_L=162Ω C_L=10pF I_{OUT}=20mA C_1=100nF C_2=22μF C_{SDO}=10pF	-	25	35	ns
	CLK-SDO	t_{pLH1}		-	25	30	ns
	LE-$\overline{OUT0}$	t_{pLH2}		-	25		ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}		-	25		ns
	$\overline{OE}$ -SDO	t_{pLH4}		-	-	40	ns
Propagation Delay Time (“H” to “L”)	LE-SDO	t_{pHL0}		-	25	35	ns
	CLK-SDO	t_{pHL1}		-	25	30	ns
	LE-$\overline{OUT0}$	t_{pHL2}		-	25		ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL3}		-	25		ns
	$\overline{OE}$ -SDO	t_{pHL4}		-	-	40	ns
Staggered Delay of Output*	Output Group 1~ Output Group 2	t_{stag1}		-	10	-	ns
	Output Group 1~ Output Group 3	t_{stag2}		-	20	-	ns
	Output Group 1~ Output Group 4	t_{stag3}		-	30	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		15	-	-	ns
	LE	$t_{w(L)}$		15	-	-	ns
Data Clock Frequency		F_{CLK}		-	-	30	MHz
Hold Time for LE		$t_{h(L)}$		10	-	-	ns
Setup Time for LE		$t_{su(L)}$		10	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
Maximum CLK Rise Time**		t_r		-	-	500	ns
Maximum CLK Fall Time**		t_f		-	-	500	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$t_{f,SDO}$		-	10	-	ns
Output Rise Time of Output Ports		t_{or}		10	15		ns
Output Fall Time of Output Ports		t_{of}		10	15	-	ns
Compulsory Error Detection Operation Time***		t_{ERR-C}		600	650	700	ns
$\overline{OE}$ Pulse Width****		$t_{w(OE)}$			20	-	ns
Output On-time Error*****		t_{ON_ERR}	On/off latch data=all “1” , 20 ns $\overline{OE}$ low level one -shot pulse input	0	5	12	ns

* Output group 1~4 can refer to “Stagger Delay of Output” Section for detailed information.

** If t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded drivers.

*** The detection time of compulsory error detection is 600ns. However, it takes extra operation time to enter or exit the error detection mode. The specifications here list the total operation time for detection. Please refer to the section of principle of operation for details.

**** $\overline{OE}$ =t_{or}+t_{of}.

*****Output pulse width= $\overline{OE}$ + t_{ON_ERR}. Users should set the appropriate $\overline{OE}$ pulse width based on the required uniformity of $\overline{OE}$ gray scale.

Switching Characteristics (V_{DD}=3.3V; Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time (“L” to “H”)	LE-SDO	t_{pLH0}	V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω R_L=162Ω C_L=10pF I_{OUT}=20mA C_1=100nF C_2=22μF C_{SDO}=10pF	-	35	45	ns
	CLK-SDO	t_{pLH1}		-	30	35	ns
	LE-$\overline{OUT0}$	t_{pLH2}			30		ns
	$\overline{OE}$-$\overline{OUT0}$	t_{pLH3}		-	30		ns
	$\overline{OE}$-SDI	t_{pLH4}		-	-	55	ns
Propagation Delay Time (“H” to “L”)	LE-SDO	t_{pHL0}		-	35	45	ns
	CLK-SDO	t_{pHL1}		-	30	35	ns
	LE-$\overline{OUT0}$	t_{pHL2}		-	30		ns
	$\overline{OE}$-$\overline{OUT0}$	t_{pHL3}		-	30		ns
	$\overline{OE}$-SDI	t_{pHL4}		-	-	55	ns
Staggered Delay of Output*	Output Group 1~ Output Group 2	t_{stag1}		-	10	-	ns
	Output Group 1~ Output Group 3	t_{stag2}		-	20	-	ns
	Output Group 1~ Output Group 4	t_{stag3}		-	30	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		25	-	-	ns
	LE	$t_{w(L)}$		15	-	-	ns
Data Clock Frequency		F_{CLK}		-	-	20	MHz
Hold Time for LE		$t_{h(L)}$		10	-	-	ns
Setup Time for LE		$t_{su(L)}$		10	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
Maximum CLK Rise Time**		t_r		-	-	500	ns
Maximum CLK Fall Time**		t_f		-	-	500	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$t_{f,SDO}$		-	10	-	ns
Output Rise Time of Output Ports		t_{or}		15	20		ns
Output Fall Time of Output Ports		t_{of}		15	20	-	ns
Compulsory Error Detection Operation Time***		t_{ERR-C}		600	650	700	ns
$\overline{OE}$ Pulse Width****		$t_{w(OE)}$			30	-	ns
Output On-time Error*****		t_{ON_ERR}	On/off latch data=all “1” , 30 ns $\overline{OE}$ low level one -shot pulse input	0	10	16	ns

* Output group 1~4 can refer to “Stagger Delay of Output” Section for detailed information.

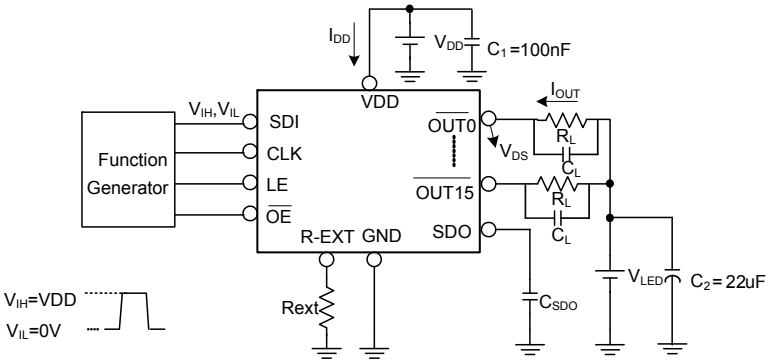
**If t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded drivers.

***The detection time of compulsory error detection is 600ns. However, it takes extra operation time to enter or exit the error detection mode. The specifications here list the total operation time for detection. Please refer to the section of principle of operation for details.

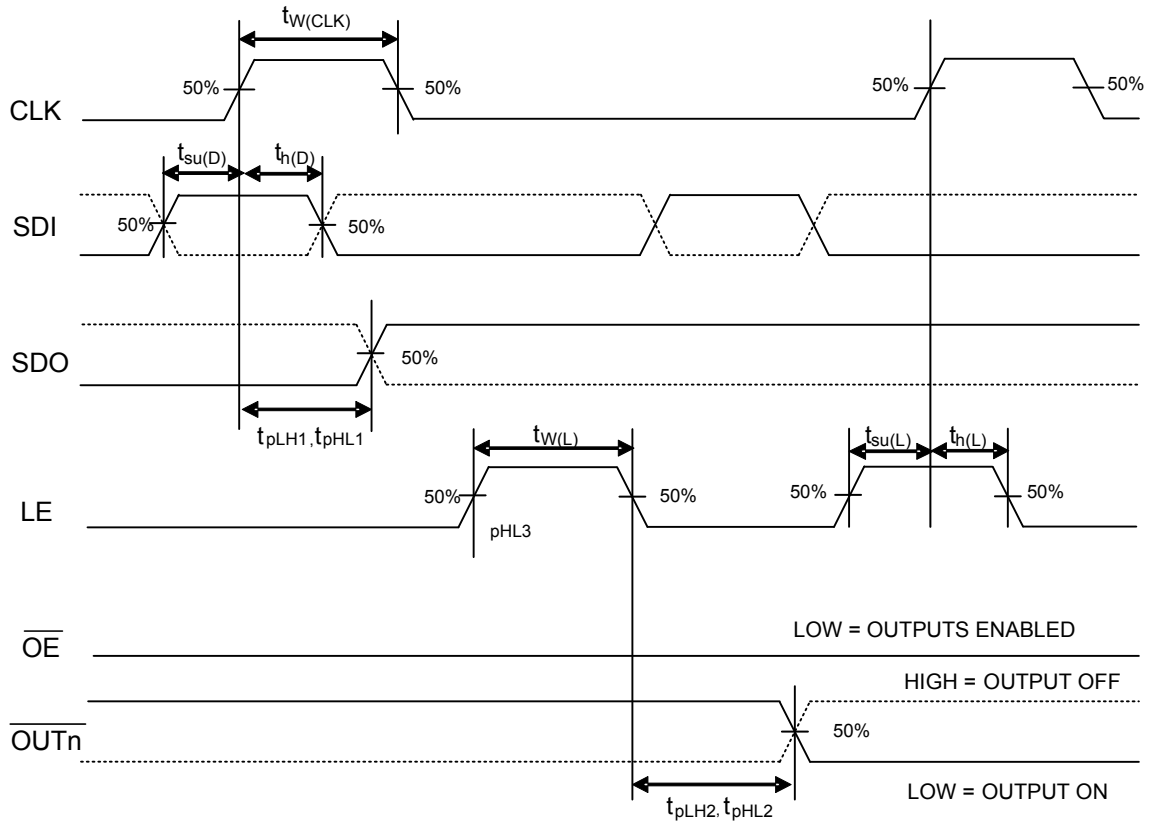
**** $\overline{OE}$ =t_{or}+t_{of}.

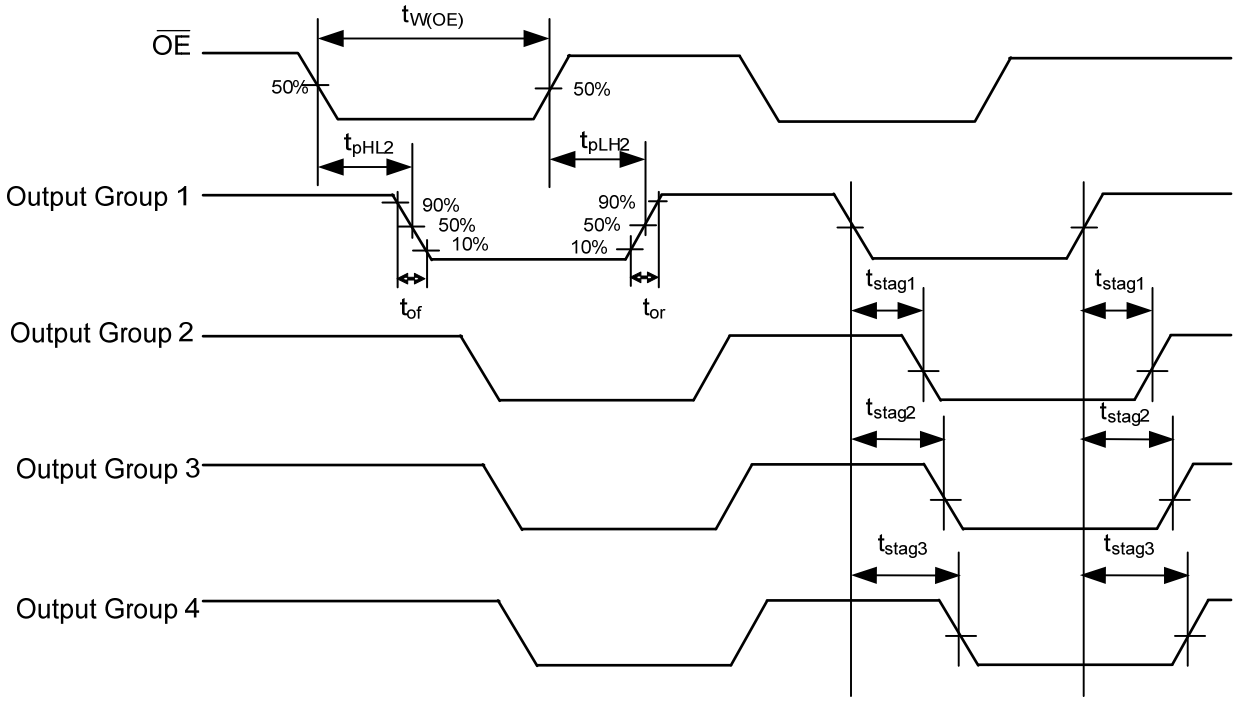
*****Output pulse width= $\overline{OE}$ + t_{ON_ERR}. Users should set the appropriate $\overline{OE}$ pulse width based on the required uniformity of $\overline{OE}$ gray scale.

Test Circuit for Switching Characteristics

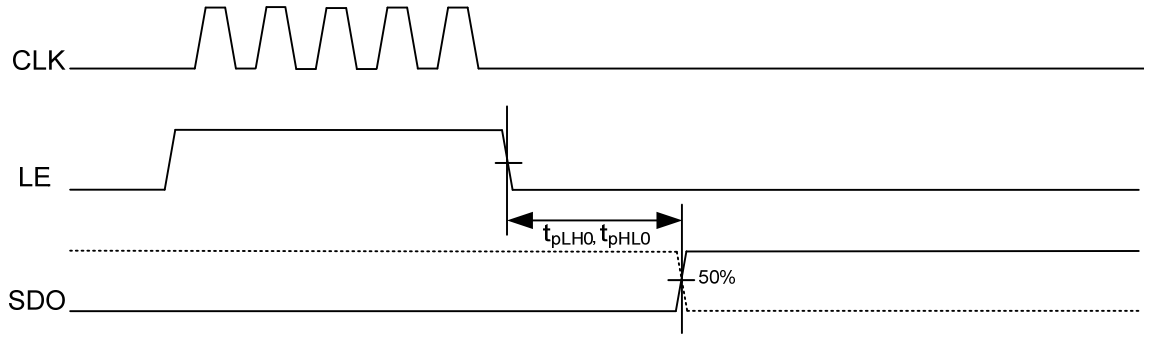


Timing Waveform

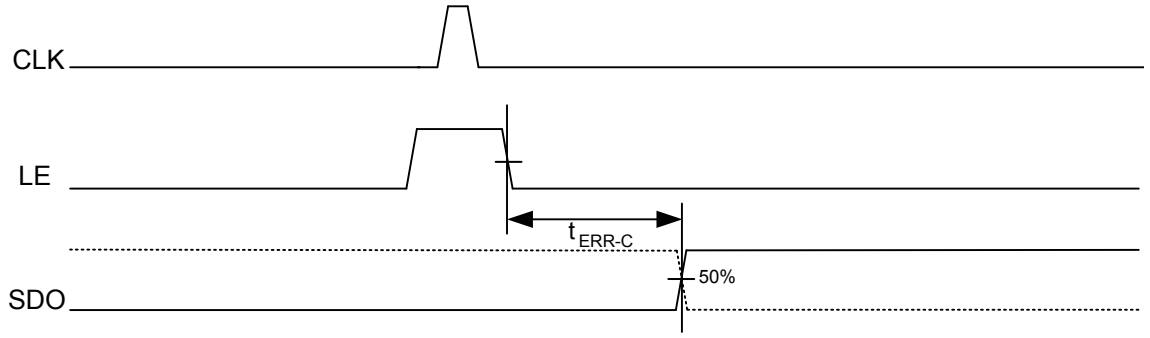




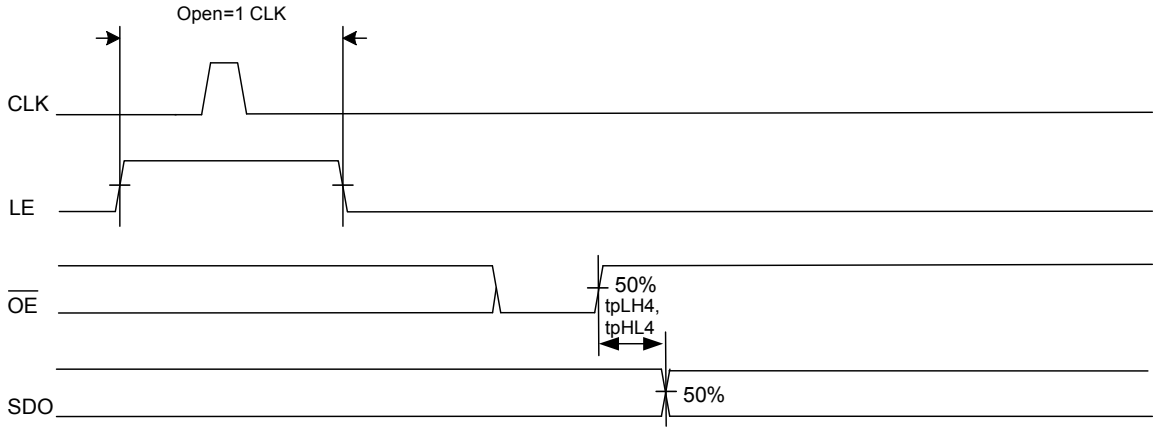
Read Configuration Register



Compulsory Open-Circuit Error Report



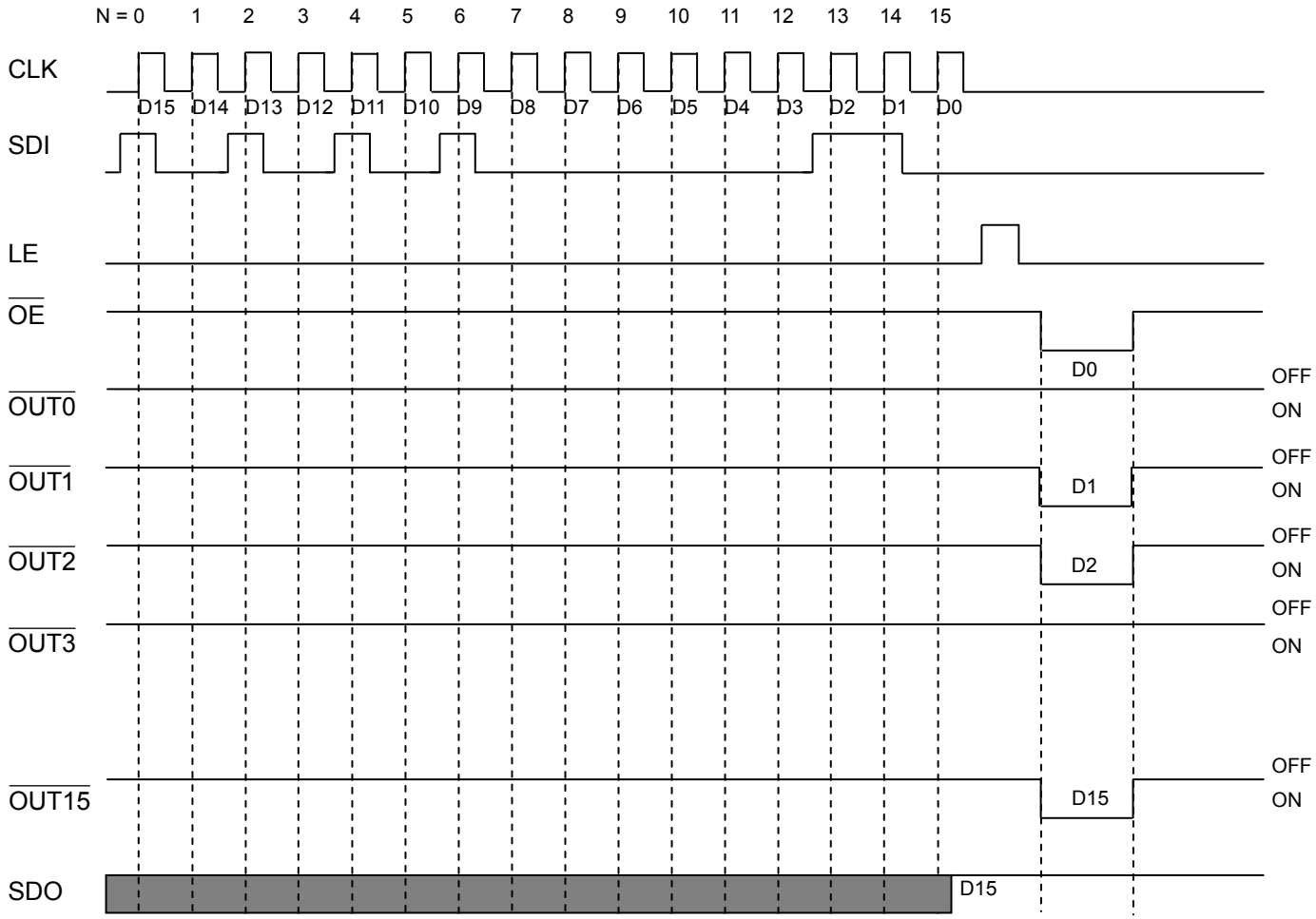
Error Detection Time Decided by $\overline{OE}$



Control the Output Ports

The data is shifted from the SDI to the 16-bits shift registers. When both the LE is asserted and no CLK toggles when LE is high, the data in the shift register is latched to the output latch. This is so-called “series-in parallel out” mechanism.

When the $\overline{OE}$ is low and the data in the output latch is “1”, the output channel will be turned on and the current will sink into the output port. If LEDs are connected to the output port with adequate power source, the LEDs will be lit up with the pre-set current.



Definition of Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	0	0	1	0	1	6'b101011					

Default setting of configuration register is 16'h716B

Bit	Definition	Value	Function
F, E	Reserved	01 (Default)	Reserved. Please set 01.
D~C	Error detection time	00	Reserved. Not for use.
		01	Reserved. Not for use.
		10	The detection time is between the falling edge of LE and rising edge of $\overline{OE}$
		11 (Default)	The detection time is default value (<700ns)
B, A	Reserved	00(Default)	Reserved. Please set 00.
9~6	Configuration register check bits	0101	Write in configuration register. Please set 0101 or data cannot be updated to the configuration register.
5~0	Current gain	000000 ~ 111111	6'b101011 (Default): allow 64-step programmable current gain from 12.5 % to 200%

Control Command

	Signals Combination	Description
Command Name	**Number of CLK Rising Edge when LE is asserted**	**The Action After a Falling Edge of LE**
Latch data	0	Latch the serial data to the output latch.
Compulsory open-circuit detection	1	Issue "open-circuit error detection" once. The data latching will not occur.
Write configuration	4	Serial data are transferred to the "configuration register"
Read configuration	5	"Configuration register" is shifted out to SDO.
No Action	2, 3, > 5	No action. Please do not use it.

Data Output From SDO

Command	SDO after a falling edge of LE
Latch data	Serial data input ; the data had latched into output buffer
Compulsory open-circuit detection	Error code of Compulsory open-circuit detection. After the falling edge of LE, it needs to wait t_{ERR-C}*.
Write configuration register	Serial data input ; the data had latched into configuration register
Read configuration register	Shift out data from configuration register

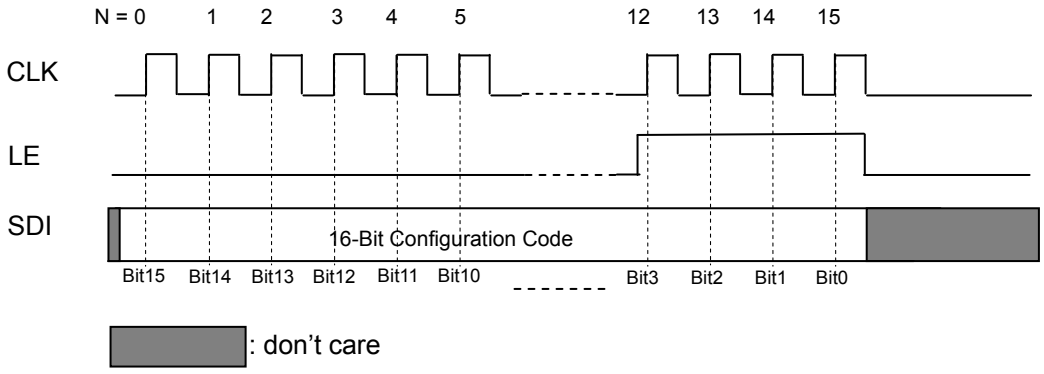
*See section of "Principle of Operation" for detailed timing diagram.

Error Code

Result	Error flag for corresponding bit in the shift register
Open-circuit error is detected in the channel	0
No open-circuit error is detected in the channel (Or detection is suppressed)	1

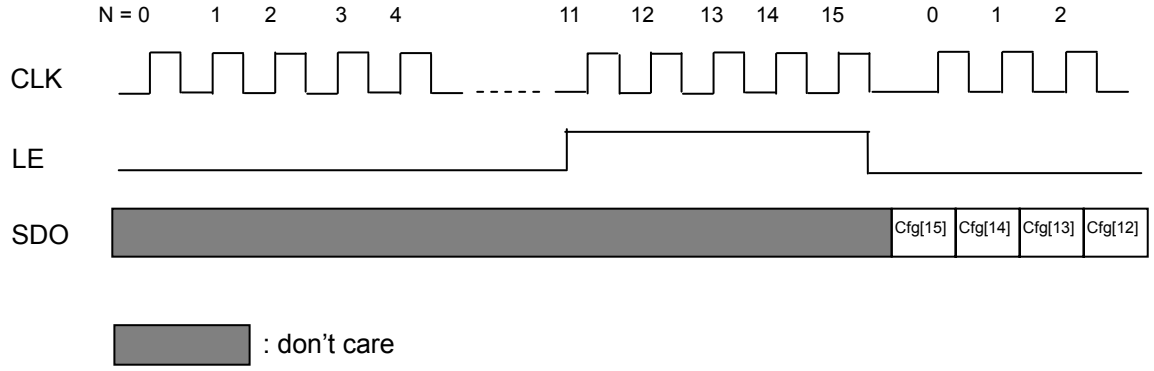
If the condition of valid error detection does not matched, the detection is suppressed. Please refer to section of "Principle of Operation" for the condition of valid error detection.

Writing Configuration Register



After entering the writing configuration mode, the system controller sends a 16-bit configuration register setting which must include check bits (bit9~bit6=0101) to the 16-bit shift register through the SDI pin. Then the falling edge of LE will transfer the contents in the shift register to a 16-bit configuration register rather than the 16-bit output latch. If the check bits are not equal to "0101", the data will not be updated to the configuration register.

Reading Configuration Register



If users want to know the current setting of the configuration register, user could send the "read configuration" command, i.e. LE contains 5 CLKs rising edge. The MSB(CF[15]) of the configuration register will be shifted out first).

Principle of Operation

Compulsory Error Detection

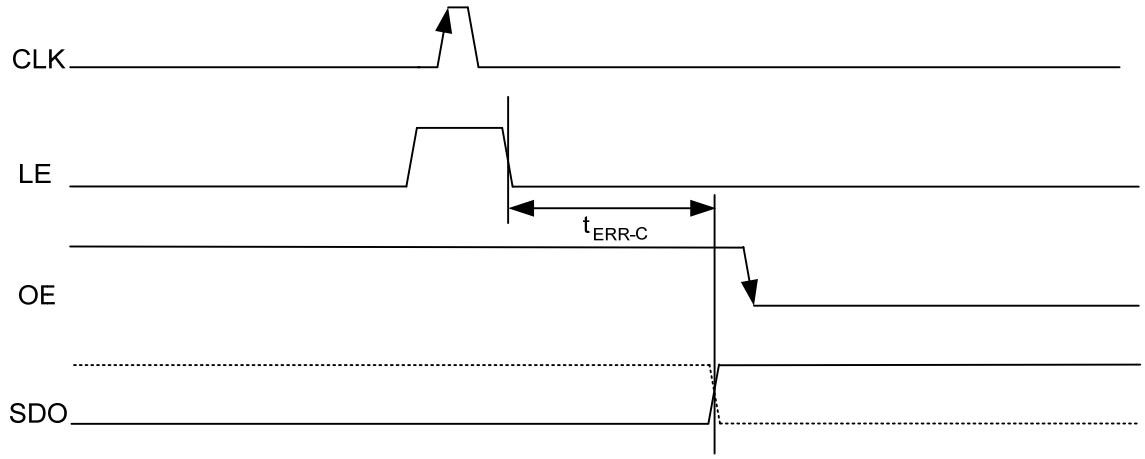
Compulsory error detection is “silent error detection”, also named as “dark” or “blind” error detection. No matter the data is 1 or 0, the output will be turned on in a short time in the compulsory error detection mode. The turn-on time and current are too short and small to influence the quality of video and image. Therefore, the human eyes cannot perceive the detection. According to the issued “control commands”, if an LED is open-circuit, the error code will be “0” and shifted out through SDO once only.

Compulsory Open-Circuit Detection

The principle of MBI5034 LED open-circuit detection is based on the fact that the LED loading status is judged by comparing the effective voltage value (V_{DS}) of each output port with the target voltage ($V_{OD,TH}$ = 0.35V). Thus, after the command of “compulsory open-circuit detection”, the output ports of MBI5034 will be turned on in a short time. Then, the error status saved in the built-in register will be shifted out through SDO pin bit by bit while receiving the new data simultaneously.

BIT[D:C]=11

The open-circuit detection time is a default value. The MBI5034 starts the error detection and then loads error result to shift register after 700ns at the falling edge of LE.



1. Condition of valid error detection: (1) falling edge of LE and (2) $\overline{OE}$ =high during t_{ERR-C}

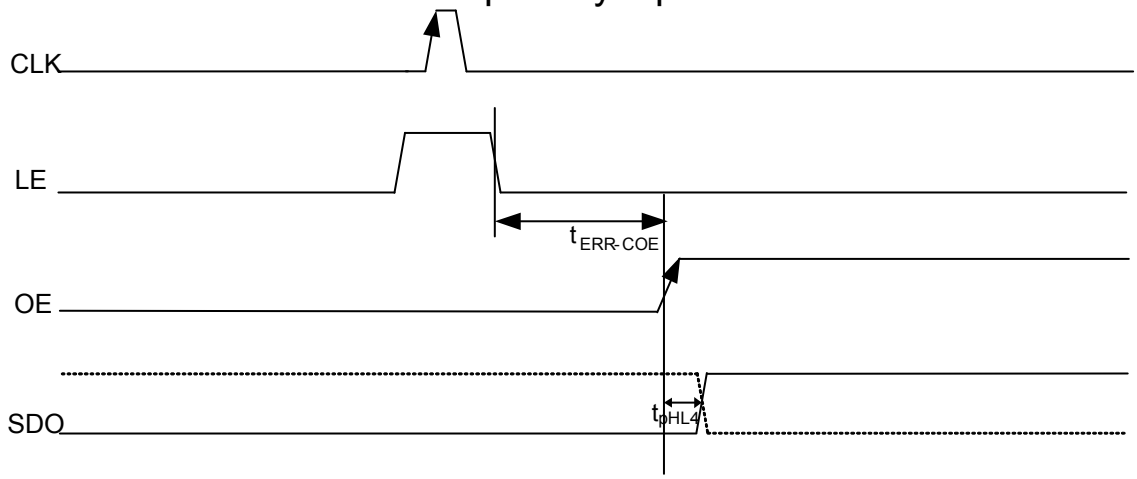
Note: If the above condition is not matched, the error detection is suppressed and error codes remain “1”.

2. At the falling edge of LE, all output channels are turned on by small current.

3. The MBI5034 starts the error detection and then loads error result to shift register after t_{ERR-C} duration.

BIT[D:C]=10

The manual setting of open-circuit detection time($t_{ERR-COE}$) is between the falling edge of LE and the rising edge of $\overline{OE}$. The error status will be shifted out to shift register. This setting is for high parasitic impedance. Users can set the detection time to overcome parasitic impedance.



1. Condition of valid error detection:(1) falling edge of LE (2) $\overline{OE}$ =low during $t_{ERR-COE}$

Note: If the above condition is not matched, the error detection is suppressed and error codes remain “1”.

2. At the falling edge of LE, all output channels are turned on by small current.

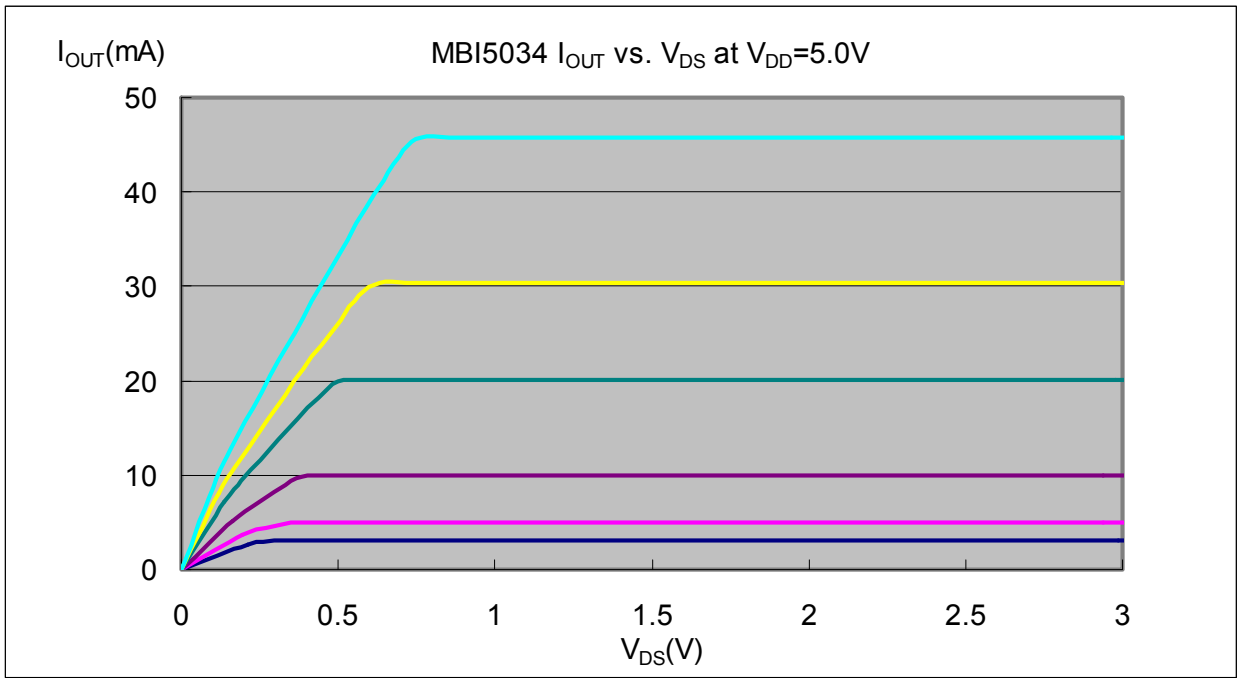
3. The MBI5034 starts the error detection and then loads error result to shift register after $t_{ERR-COE}$ duration.

Constant Current

In LED display applications, MBI5034 provides nearly no current variations from channel to channel and from IC to IC. This can be achieved by:

1) While $I_{OUT} \leqq 45mA$, $V_{DD}=5V$, the maximum current skew between channels is less than ±1.5% (typical) and that between ICs is less than ±3.0% (typical).

2) In addition, the characteristics curve of output stage in the saturation region is flat and users can refer to the charts as shown below. Thus, the output current keeps constant regardless of the variations of LED forward voltages (V_F). The output current level in the saturation region is defined as output target current $I_{out,target}$.



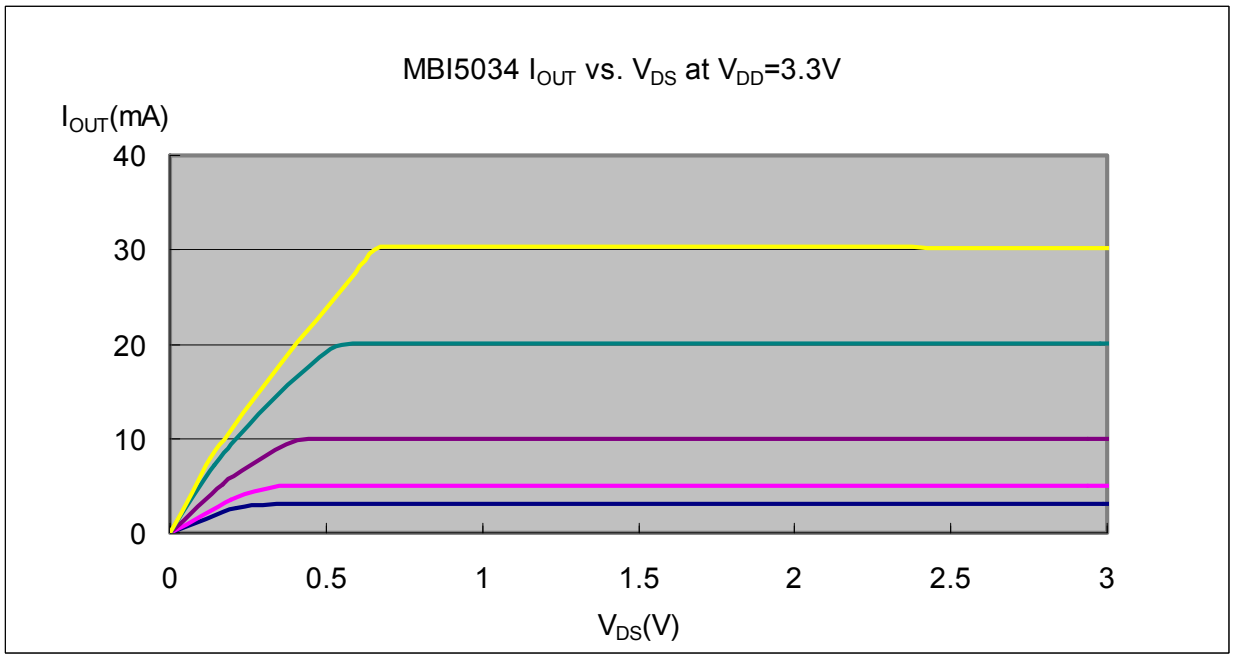
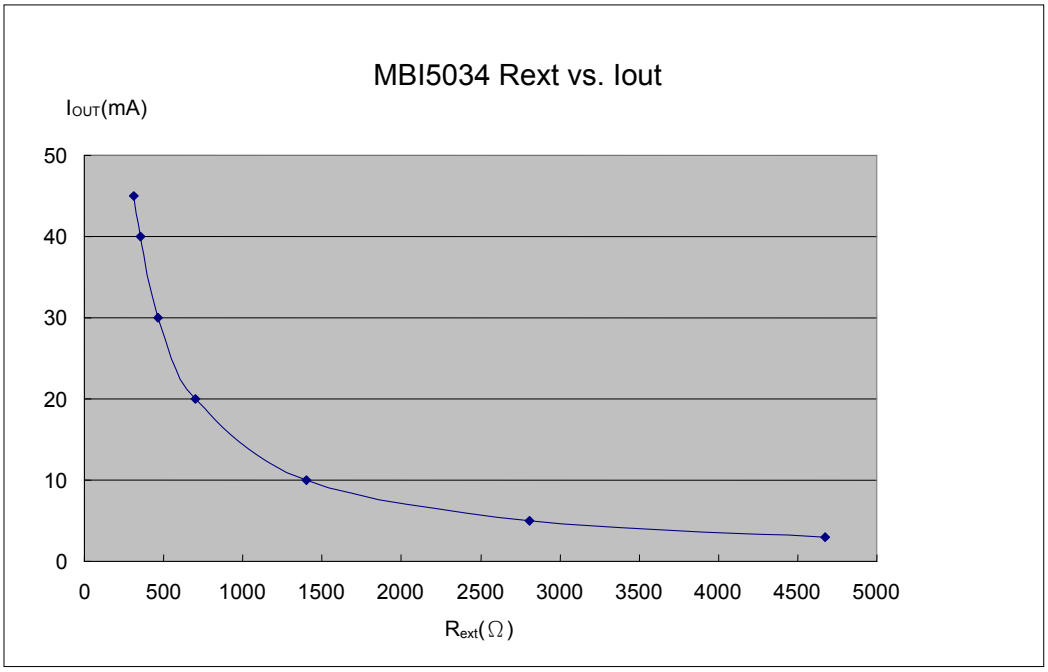


Figure 3

Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.



MBI5034 R_{ext} vs. I_{OUT}

Also, the output current can be calculated from the equation:

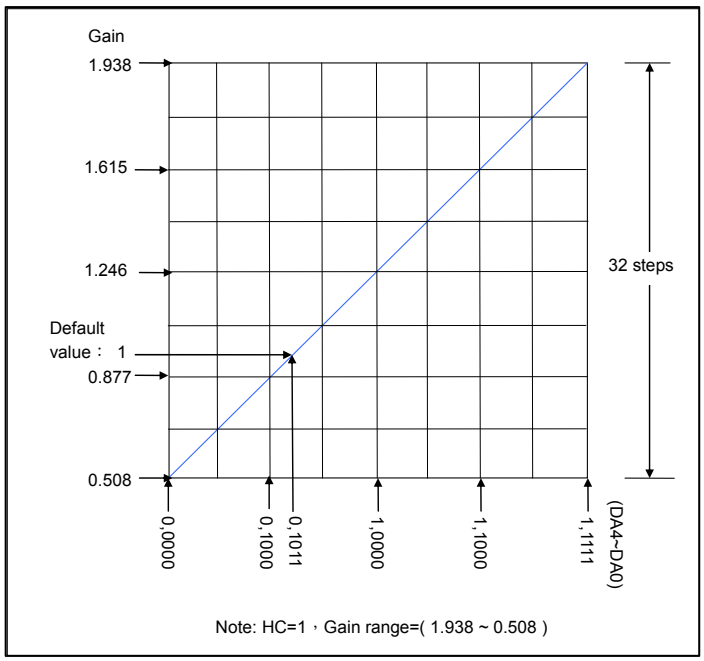
$V_{R\text{-}EXT}$=0.61Volt x G x H; $I_{OUT}=V_{R\text{-}EXT}/(R_{ext}$ x H)x23.0

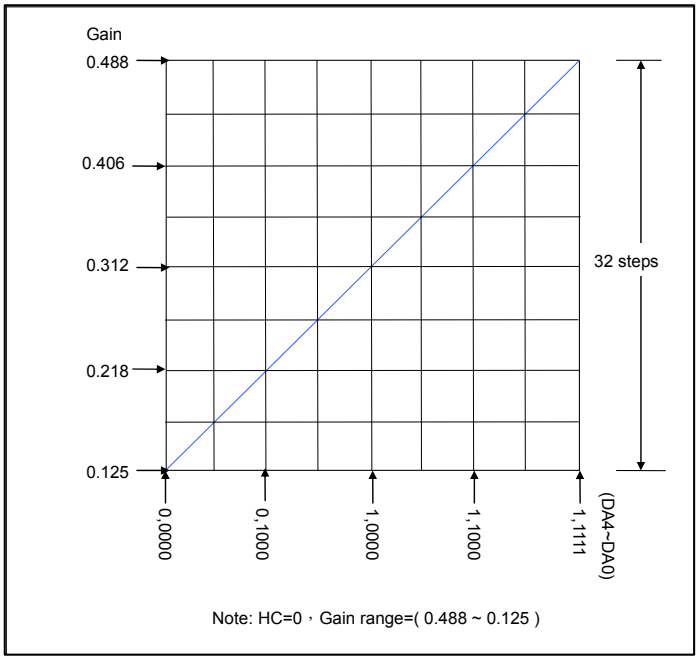
HC=1=>H=1 (Please refers to Current Gain Adjustment section on P19. for “HC” description)

HC=0=>H=4

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit 5 to bit 0 of the configuration register. The default value of G is 1. For your information, the output current is about 20mA when R_{ext}=700Ω and 42.5mA when R_{ext}=330Ω if G is set to default value 1. The formula and the setting for G are described in the next section.

Current Gain Adjustment





The 6 bits (bit 5~bit 0) of the configuration register set the gain of output current. As total 6-bit in number, i.e., ranged from 6'b000000 to 6'b111111, these bits allow the user to set the output current gain up to 64 steps. These bits can be further defined inside configuration register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	HC	DA4	DA3	DA2	DA1	DA0

1. Bit 5 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 4 to bit 0 are DA4~DA0.

The relationship between these bits and current gain (G) is:

HC=1, D=(65xG-33)/3

HC=0, D=(256xG-32)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D=DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 5-bit mantissa DA4~DA0.

For example,

HC=1, G=1.246, D=(65x1.246-33)/3=16

the D in binary form would be:

$D=16=1x2^4+0x2^3+0x2^2+0x2^1+0x2^0$

The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b110000.

Staggered Delay of Output

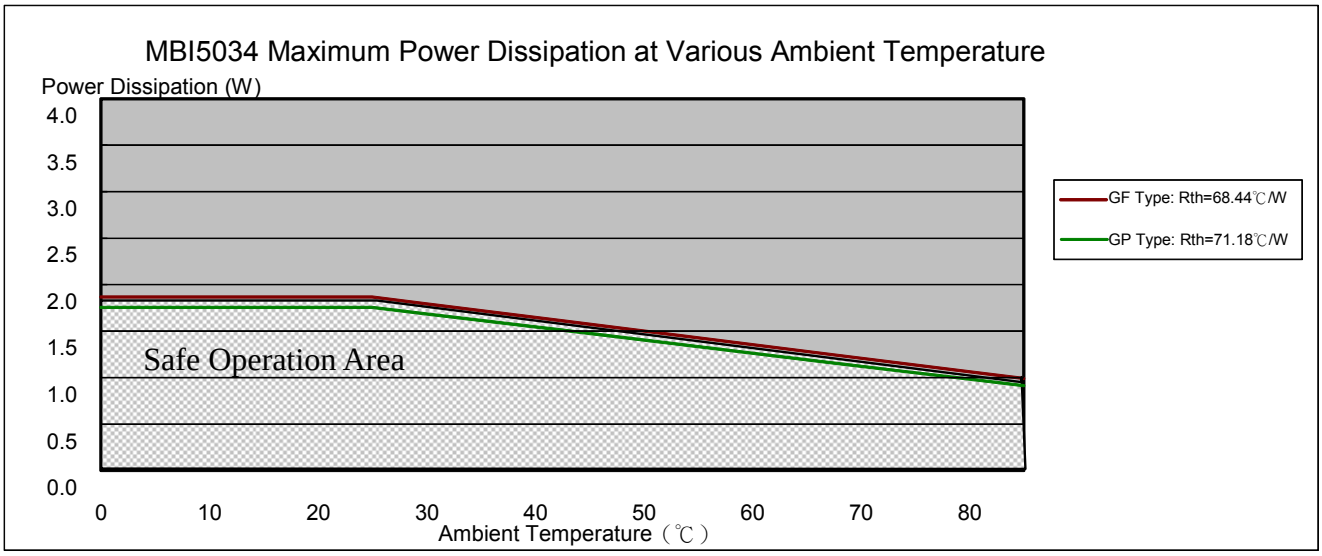
MBI5034 has a built-in delay circuit to perform delay mechanism. Among output ports exist a graduated 10ns delay time among 4 groups as shown in below chart by which the output ports will be turned on at a different time so that the instant current from the power line will be lowered.

Output Group	Output Channel	Output Channel	Output Channel	Output Channel
Output Group 1	$\overline{OUT0}$	$\overline{OUT4}$	$\overline{OUT9}$	$\overline{OUT13}$
Output Group 2	$\overline{OUT2}$	$\overline{OUT6}$	$\overline{OUT11}$	$\overline{OUT15}$
Output Group 3	$\overline{OUT1}$	$\overline{OUT5}$	$\overline{OUT8}$	$\overline{OUT12}$
Output Group 4	$\overline{OUT3}$	$\overline{OUT7}$	$\overline{OUT10}$	$\overline{OUT14}$

Package Power Dissipation (P_D)

The allowable maximum package heat dissipation is determined as $P_{D(max)}=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act) \leqq P_{D(max)}$, the allowable maximum output current as a function of duty cycle is: $I_{OUT} =\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

The maximum power dissipation, $P_{D(max)}=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.

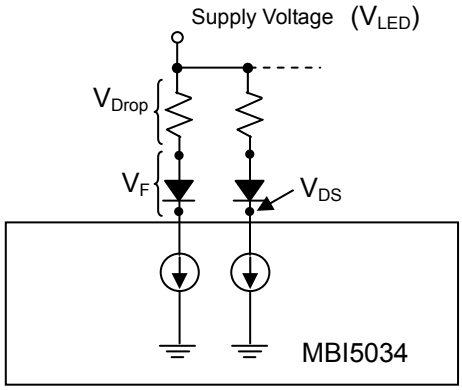


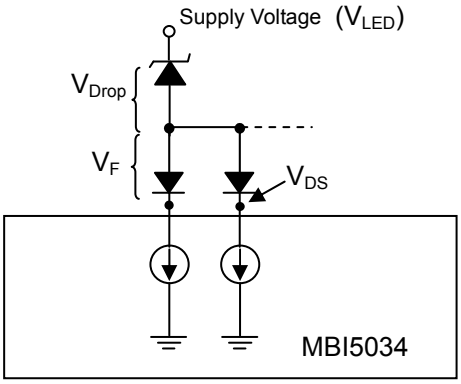
Load Supply Voltage (V_{LED})

MBI5034 is designed to operate with V_{DS} ranging from 0.4V to 1.0V, considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)}>P_{D(max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer (V_{DROP}).

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resisters or zener diode can be used in the applications as shown in the following figures.



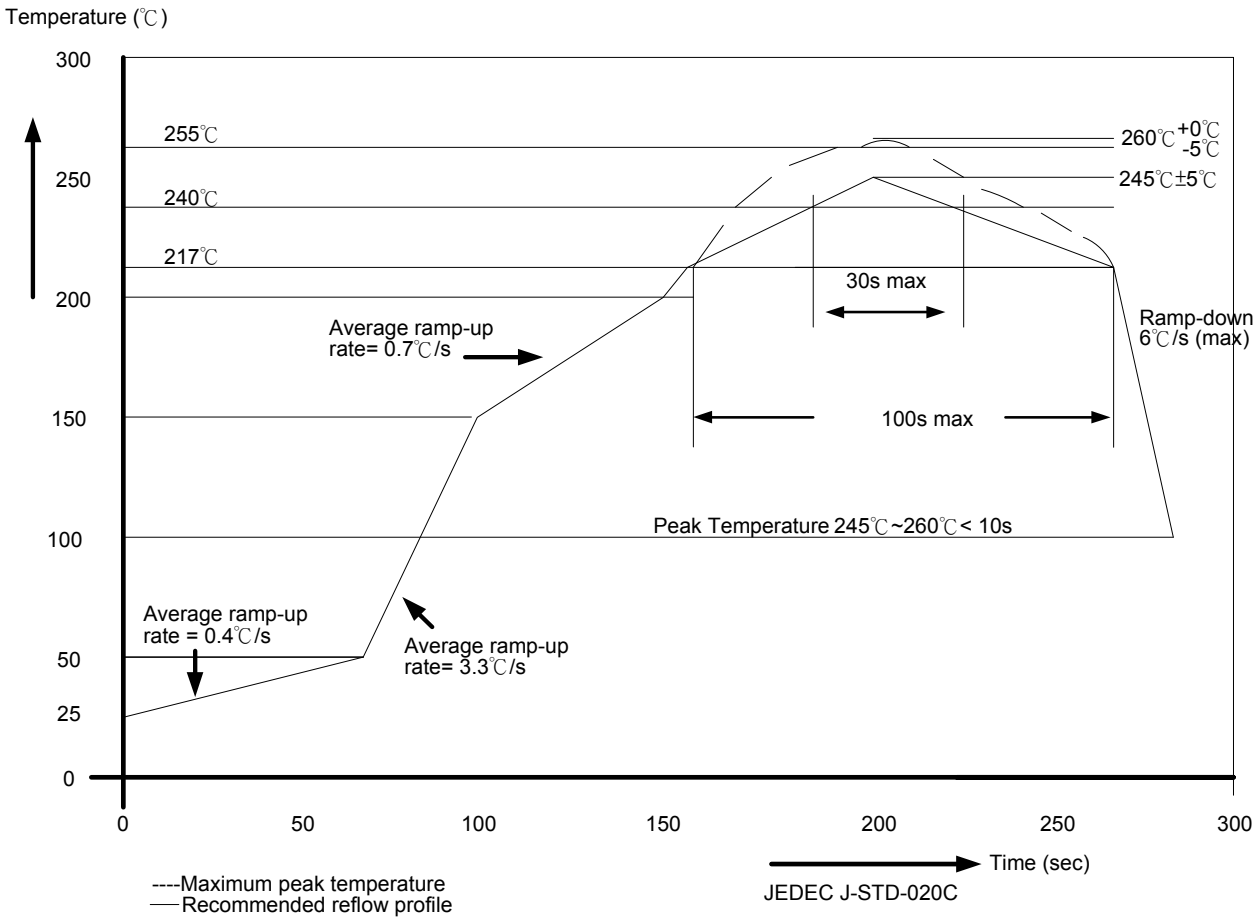


Switching Noise Reduction

LED driver ICs are frequently used in switch-mode applications which always behave with switching noise due to parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

Soldering Process of "Pb-free & Green" Package Plating*

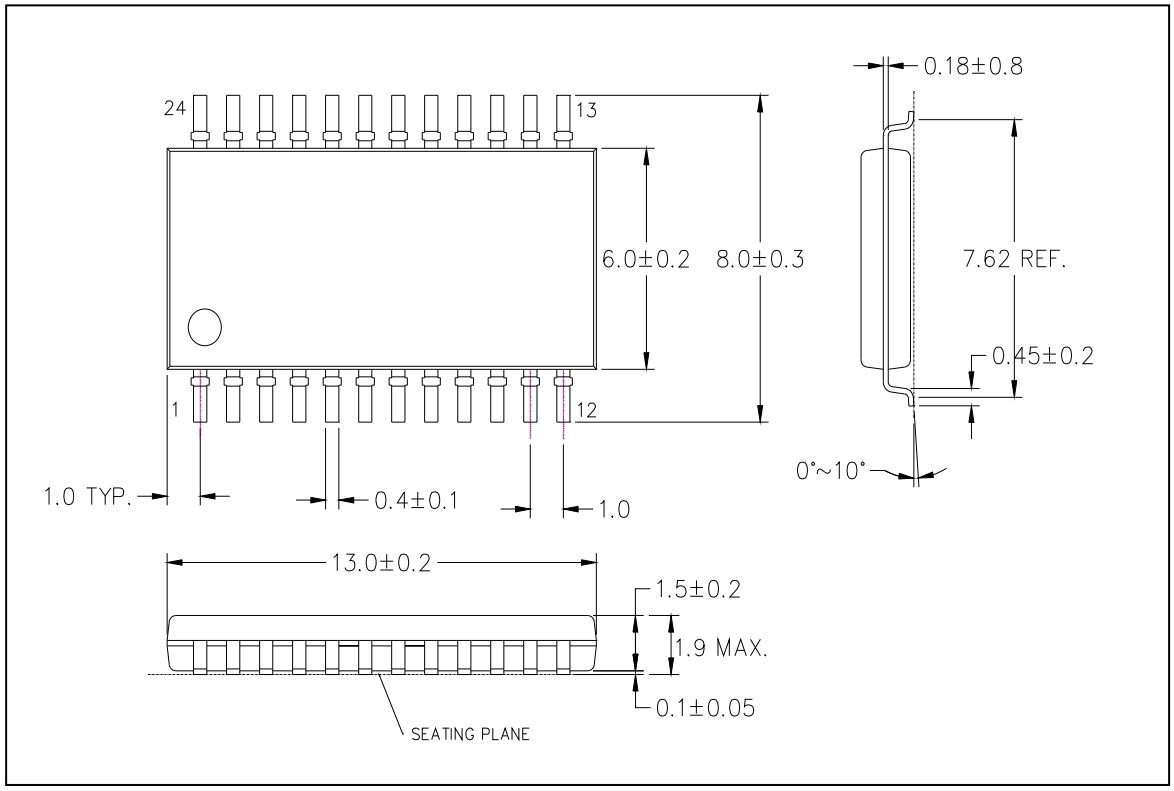
Macroblock has defined " Pb-Free & Green " to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to standard 215ºC to 240ºC reflow processes which adopt tin/lead (SnPb) solder paste. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.



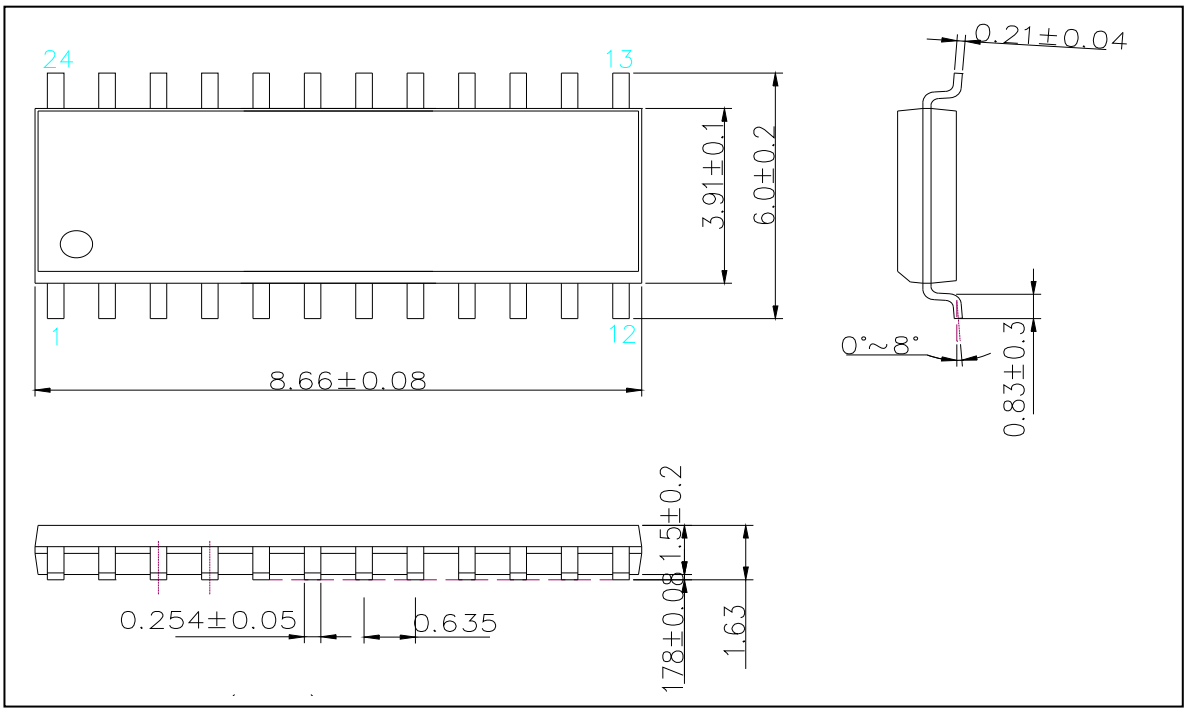
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



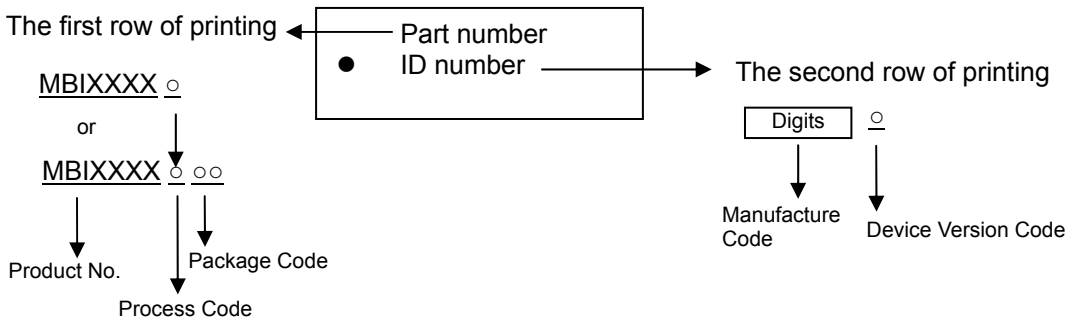
MBI5034GF Outline Drawing



MBI5034GP Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top-mark Information



Product Revision History

Datasheet version	Device version code
VA.00	A

Product Ordering Information

Part Number	**RoHS Compliant Package Type**	**Weight (g)**
MBI5034GF-A	SOP24L-300-1.00	0.28
MBI5034GP-A	SSOP24L-150-0.64	0.11

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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