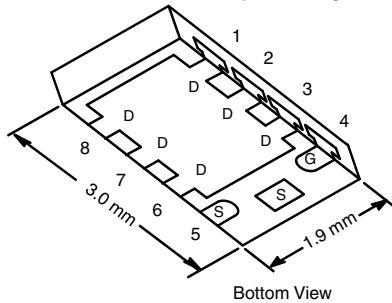


## P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) (Max.)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
- 20	0.0096 at V <sub>GS</sub> = - 4.5 V	- 25	43 nC
	0.0132 at V <sub>GS</sub> = - 2.5 V	- 25	
	0.0220 at V <sub>GS</sub> = - 1.8 V	- 7	

**PowerPAK ChipFET Single**


**Ordering Information:**  
Si5415AEDU-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

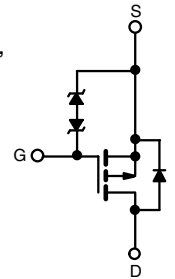
- TrenchFET® Power MOSFET
- Thermally Enhanced PowerPAK® ChipFET Package
  - Small Footprint Area
  - Low On-Resistance
- 100 % R<sub>g</sub> and UIS Tested
- Typical ESD Protection: 5500 V (HBM)
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

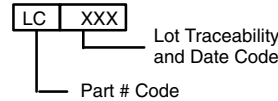
### APPLICATIONS

- Portable Devices such as Smart Phones, Tablet PCs and Mobile Computing
  - Battery Switch
  - Load Switch
  - Power Management



P-Channel MOSFET

Marking Code



### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	- 20	V
Gate-Source Voltage	V <sub>GS</sub>	± 8	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 25 <sup>a</sup>
		T <sub>C</sub> = 70 °C	- 25 <sup>a</sup>
		T <sub>A</sub> = 25 °C	- 15 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	- 12 <sup>b, c</sup>
Pulsed Drain Current (t = 100 μs)	I <sub>DM</sub>	- 70	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	- 2.6 <sup>b, c</sup>
Single Avalanche Current	I <sub>AS</sub>	- 15	mJ
Single Avalanche Energy	E <sub>AS</sub>	11	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	31
		T <sub>C</sub> = 70 °C	20
		T <sub>A</sub> = 25 °C	3.1 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	2 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	34	40	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	3	4	

#### Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 90 °C/W.



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-11		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 2$	$\mu\text{A}$
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			$\pm 0.2$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-10			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		0.0081	0.0096	$\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -5\text{ A}$		0.0110	0.0132	
		$V_{GS} = -1.8\text{ V}, I_D = -2\text{ A}$		0.0170	0.0220	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		47		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4300		pF
Output Capacitance	$C_{oss}$			445		
Reverse Transfer Capacitance	$C_{rss}$			400		
Total Gate Charge	$Q_g$	$V_{DS} = -10\text{ V}, V_{GS} = -8\text{ V}, I_D = -14\text{ A}$		80	120	nC
				43	65	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -14\text{ A}$		7		
Gate-Drain Charge	$Q_{gd}$			11.4		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.6	3.3	6.6	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		30	60	ns
Rise Time	$t_r$			45	90	
Turn-Off Delay Time	$t_{d(off)}$			75	150	
Fall Time	$t_f$			25	50	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$		12	25	
Rise Time	$t_r$			5	10	
Turn-Off Delay Time	$t_{d(off)}$			80	160	
Fall Time	$t_f$			20	40	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			-25	A
Pulse Diode Forward Current ( $t = 100\text{ }\mu\text{s}$ )	$I_{SM}$				-70	
Body Diode Voltage	$V_{SD}$	$I_S = -10\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		35	70	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			21	40	nC
Reverse Recovery Fall Time	$t_a$			20		ns
Reverse Recovery Rise Time	$t_b$			15		

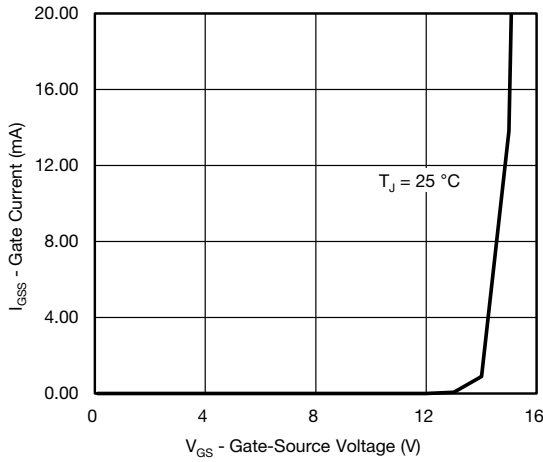
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

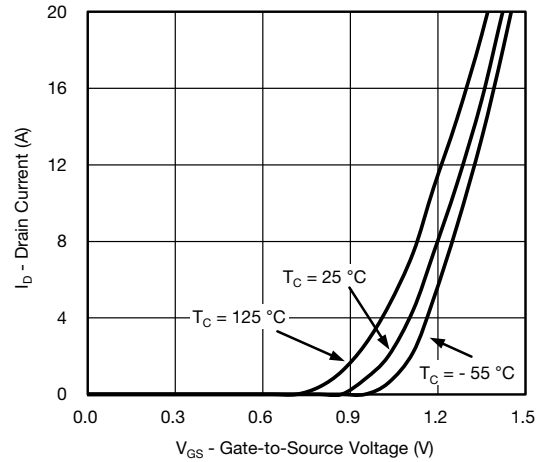
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



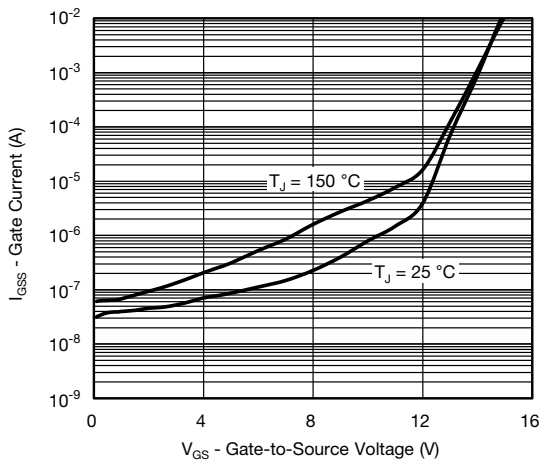
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



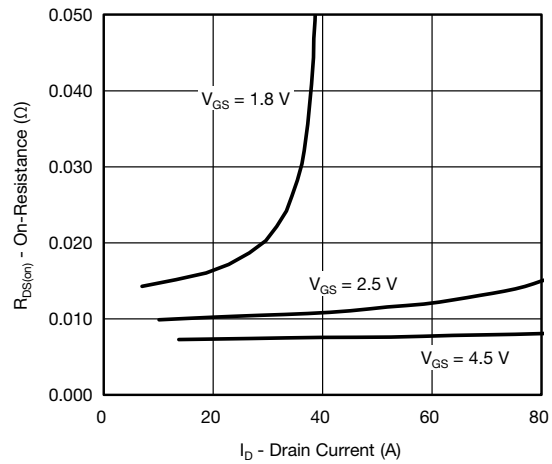
Gate Current vs. Gate-Source Voltage



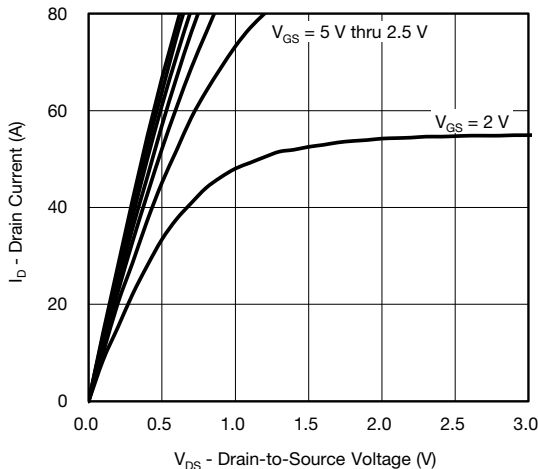
Transfer Characteristics



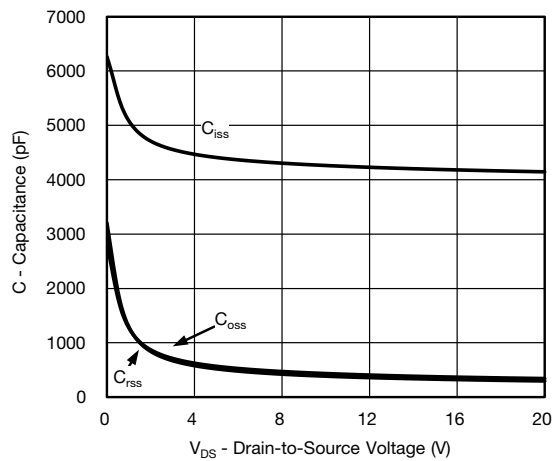
Gate Current vs. Gate-Source Voltage



On-Resistance vs. Drain Current and Gate Voltage

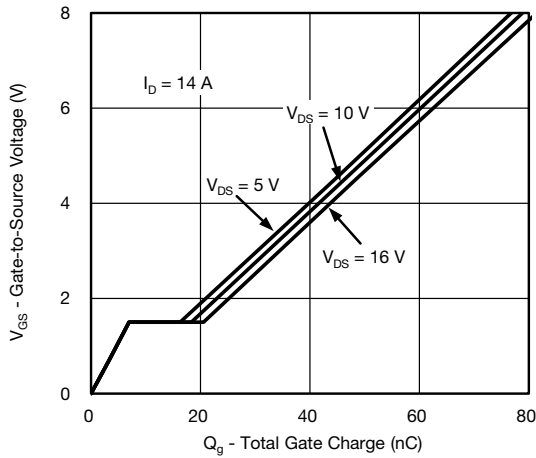


Output Characteristics

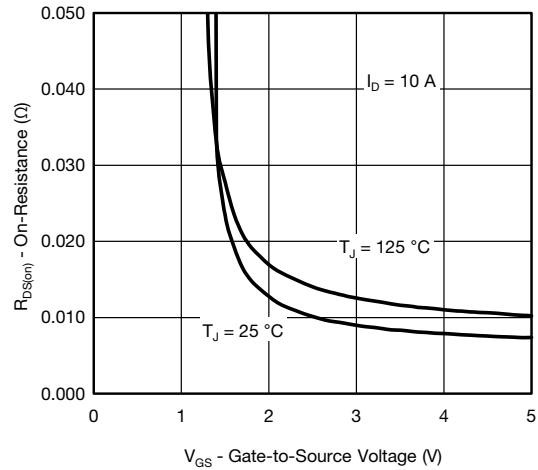


Capacitance

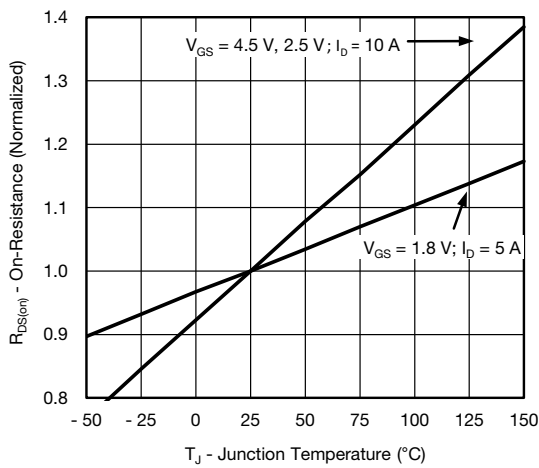
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



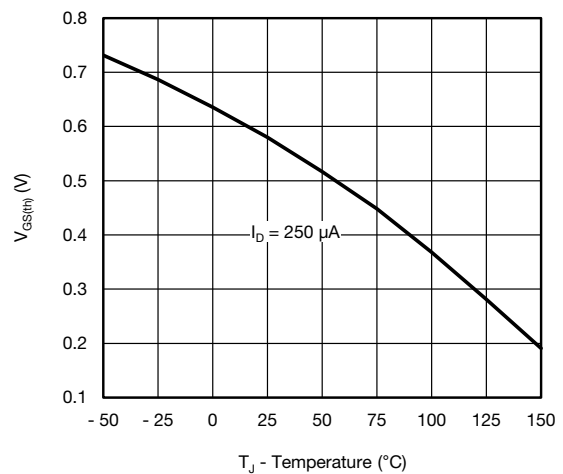
**Gate Charge**



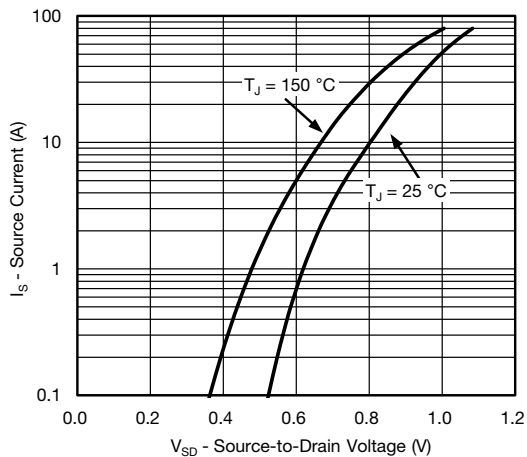
**On-Resistance vs. Gate-to-Source Voltage**



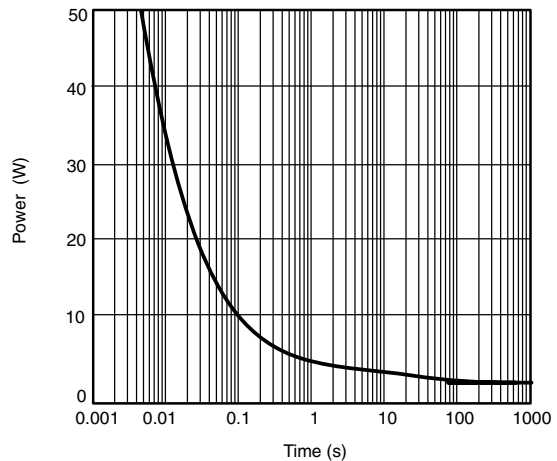
**On-Resistance vs. Junction Temperature**



**Threshold Voltage**



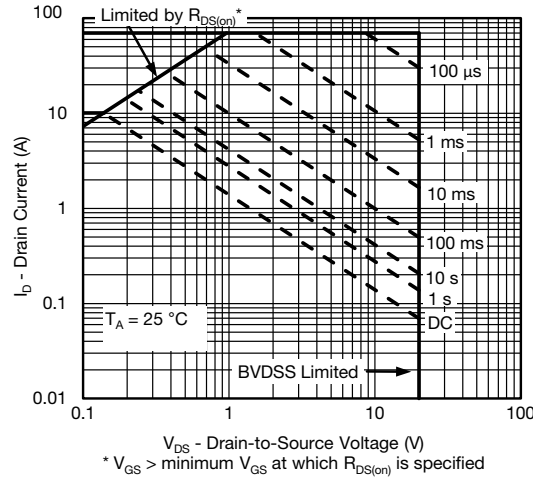
**Source-Drain Diode Forward Voltage**



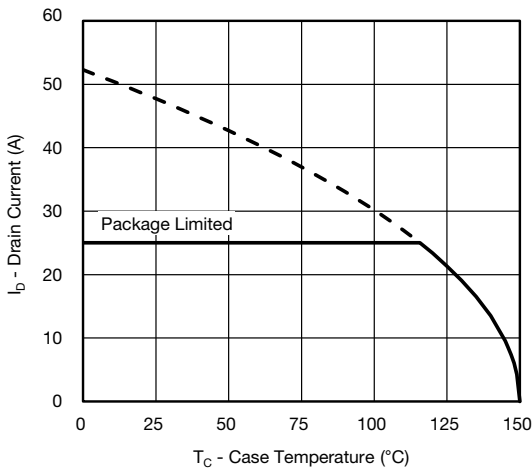
**Single Pulse Power, Junction-to-Ambient**



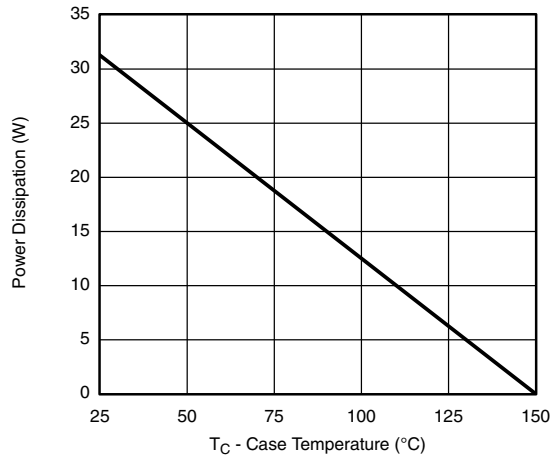
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating\*

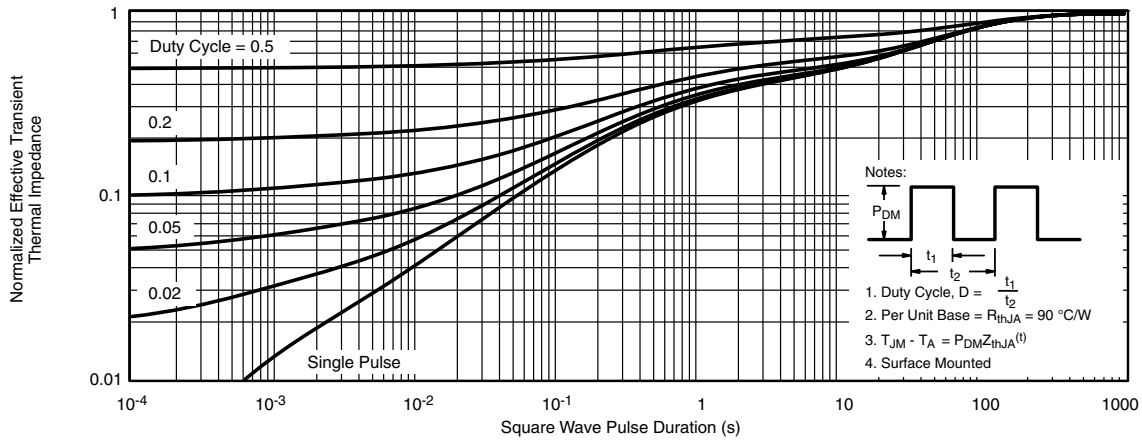


Power Derating

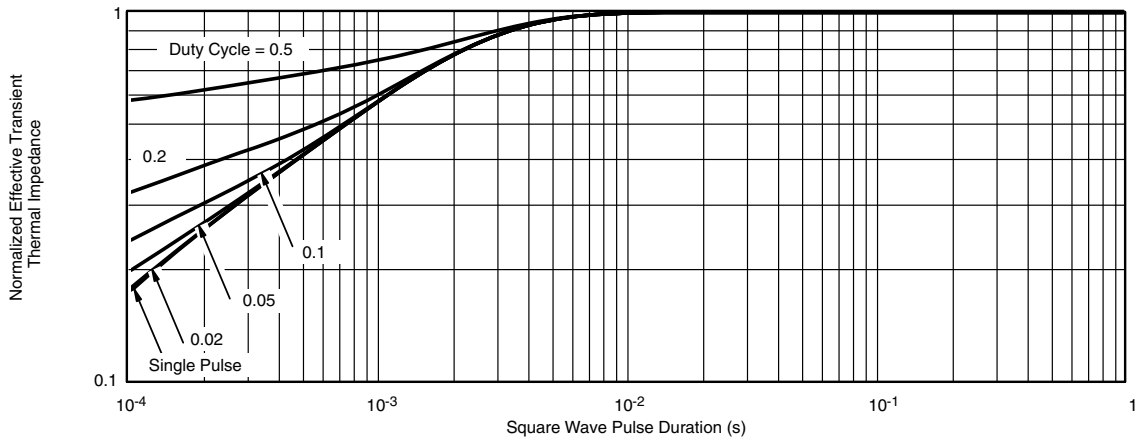
\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150\text{ }^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



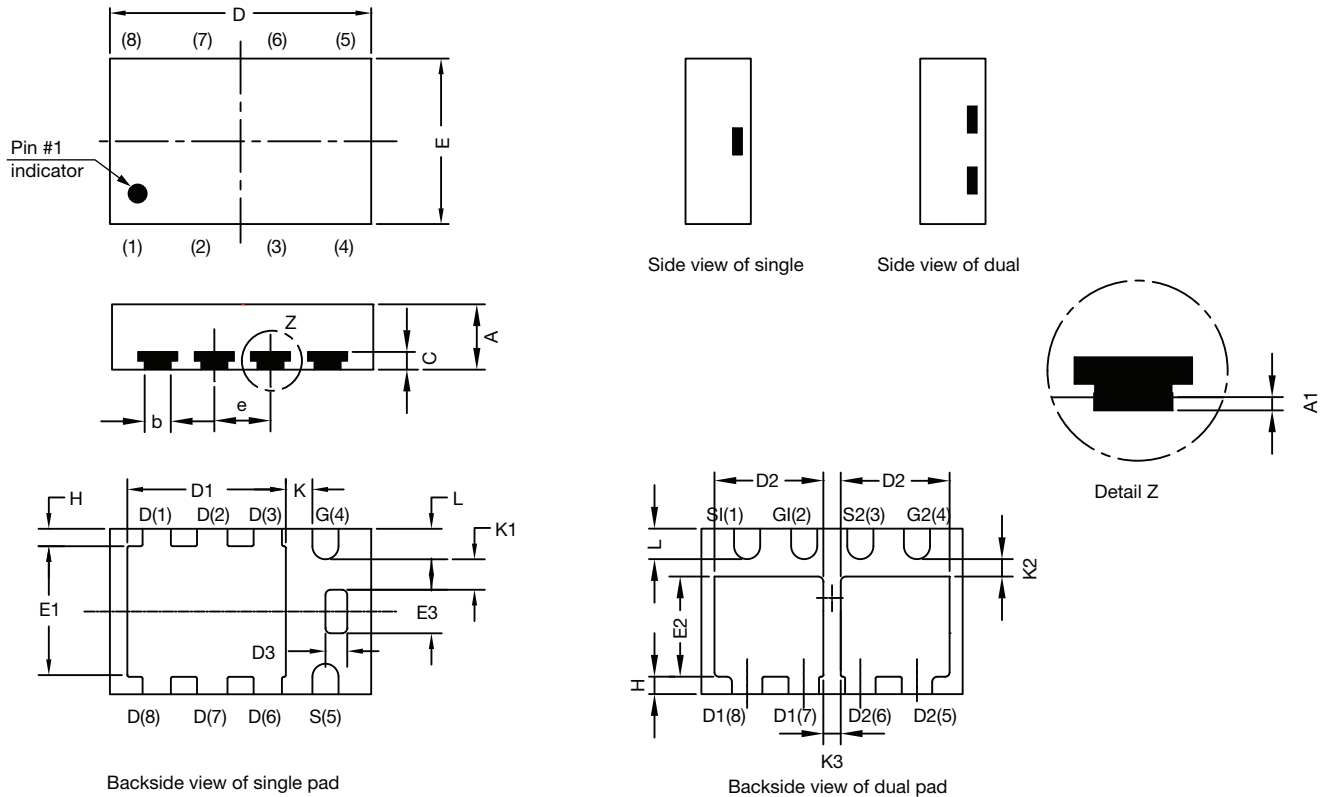
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62837](http://www.vishay.com/ppg?62837).

### PowerPAK® ChipFET® Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

C14-0630-Rev. E, 21-Jul-14  
DWG: 5940

**Note**

- Millimeters will govern

## RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads  
Dimensions in mm/(Inches)

[Return to Index](#)





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