



PJD50N10

100V N-Channel Enhancement Mode MOSFET

Voltage

100 V

Current

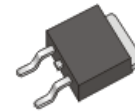
50 A

Features

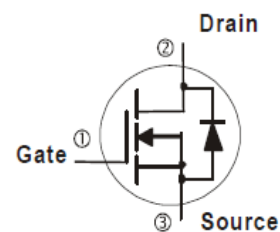
- $R_{DS(ON)}, V_{GS}@10V, I_D@20A < 25m\Omega$
- $R_{DS(ON)}, V_{GS}@4.5V, I_D@20A < 28m\Omega$
- High switching speed
- Improved dv/dt capability
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case : TO-252 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0104 ounces, 0.297grams



TO-252



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

| PARAMETER | | SYMBOL | LIMIT | UNITS |
|---|-------------------------|-----------------|------------------------|--------------------|
| Drain-Source Voltage | | V_{DS} | 100 | V |
| Gate-Source Voltage | | V_{GS} | ± 20 | V |
| Continuous Drain Current | $T_C=25^\circ\text{C}$ | I_D | 50 | A |
| | $T_C=100^\circ\text{C}$ | | 35 | |
| Pulsed Drain Current ^(Note 1) | | I_{DM} | 100 | |
| Power Dissipation | $T_C=25^\circ\text{C}$ | P_D | 125 | W |
| | $T_C=100^\circ\text{C}$ | | 63 | |
| Continuous Drain Current | $T_A=25^\circ\text{C}$ | I_D | 6.3 | A |
| | $T_A=70^\circ\text{C}$ | | 5.3 | A |
| Power Dissipation | | P_D | 2.0 | W |
| Power Dissipation | | | $T_A=70^\circ\text{C}$ | |
| Single Pulse Avalanche Energy ^(Note 6) | | E_{AS} | 68.5 | mJ |
| Operating Junction and Storage Temperature Range | | T_J, T_{STG} | -55~175 | $^\circ\text{C}$ |
| Typical Thermal resistance ^(Note 4,5) | Junction to Case | $R_{\theta JC}$ | 1.2 | $^\circ\text{C/W}$ |
| | Junction to Ambient | $R_{\theta JA}$ | 75 | |

- Limited only By Maximum Junction Temperature



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNITS |
|---|--------------|---|------|------|-----------|------------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V, I_D=250\mu A$ | 100 | - | - | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250\mu A$ | 2.0 | 2.6 | 3.5 | V |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=20A$ | - | 22 | 25 | m Ω |
| | | $V_{GS}=6V, I_D=20A$ | - | 23 | 28 | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=100V, V_{GS}=0V$ | - | - | 1.0 | μA |
| Gate-Source Leakage Current | I_{GSS} | $V_{GS}=\pm 20V, V_{DS}=0V$ | - | - | ± 100 | nA |
| Dynamic (Note 7) | | | | | | |
| Total Gate Charge | Q_g | $V_{DS}=50V, I_D=20A,$ $V_{GS}=10V$ (Note 1,2) | - | 53 | - | nC |
| Gate-Source Charge | Q_{gs} | | - | 13 | - | |
| Gate-Drain Charge | Q_{gd} | | - | 14 | - | |
| Input Capacitance | C_{iss} | $V_{DS}=50V, V_{GS}=0V,$ $f=1.0\text{MHz}$ | - | 3152 | - | pF |
| Output Capacitance | C_{oss} | | - | 110 | - | |
| Reverse Transfer Capacitance | C_{rss} | | - | 66 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DS}=50V, R_L=2.5\Omega,$ $V_{GS}=10V, R_G=3\Omega$ (Note 1,2) | - | 18 | - | ns |
| Turn-On Rise Time | t_r | | - | 45 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 53 | - | |
| Turn-Off Fall Time | t_f | | - | 15 | - | |
| Drain-Source Diode | | | | | | |
| Maximum Continuous Drain-Source Diode Forward Current | I_S | --- | - | - | 50 | A |
| Diode Forward Voltage | V_{SD} | $I_S=1A, V_{GS}=0V$ | - | 0.7 | 1.2 | V |

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.
4. The maximum current rating is package limited.
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz. square pad of copper.
6. The test condition is $L=0.1\text{mH}$, $I_{AS}=37A$, $V_{DD}=25V$, $V_{GS}=10V$
7. Guaranteed by design, not subject to production testing.



PJD50N10

TYPICAL CHARACTERISTIC CURVES

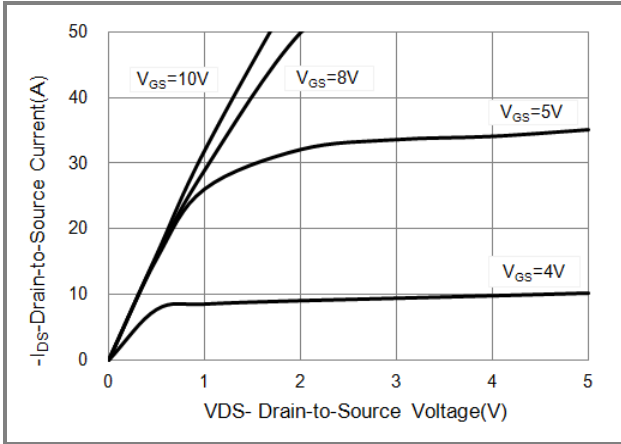


Fig.1 Output Characteristics

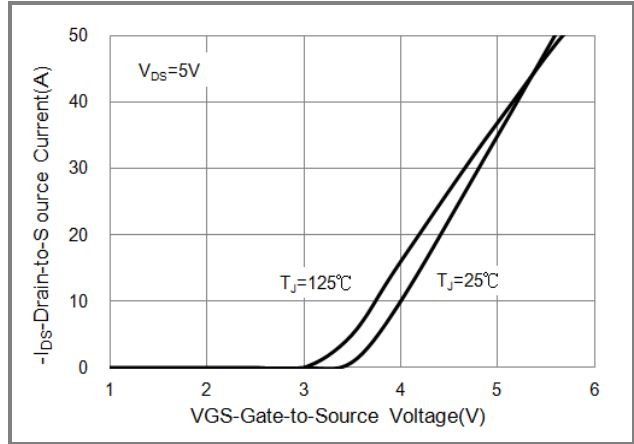


Fig.2 Transfer Characteristics

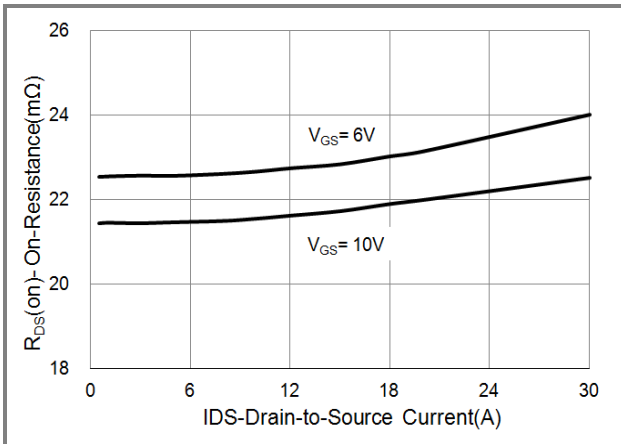


Fig.3 On-Resistance vs. Drain Current

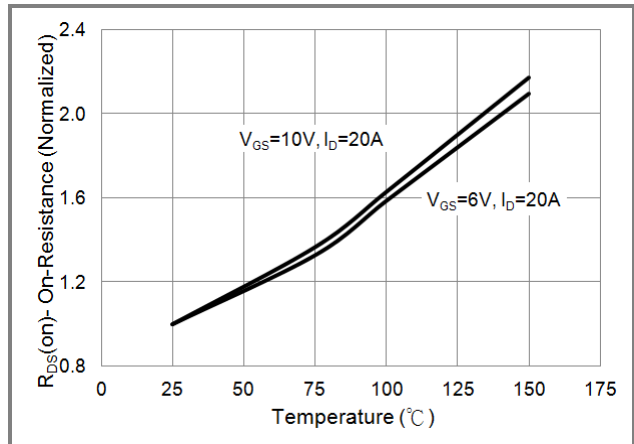


Fig.4 On-Resistance vs. Junction temperature

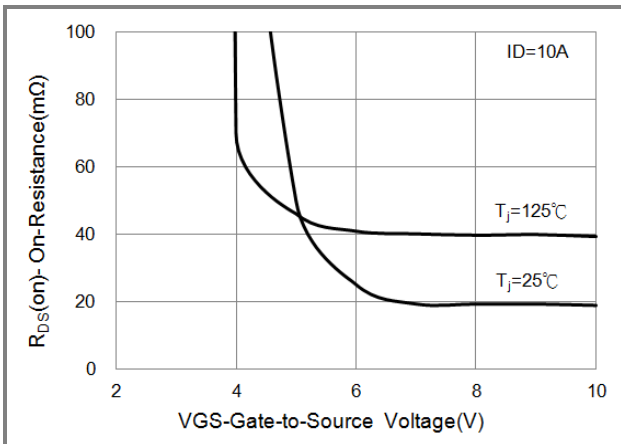


Fig.5 On-Resistance Variation with VGS.

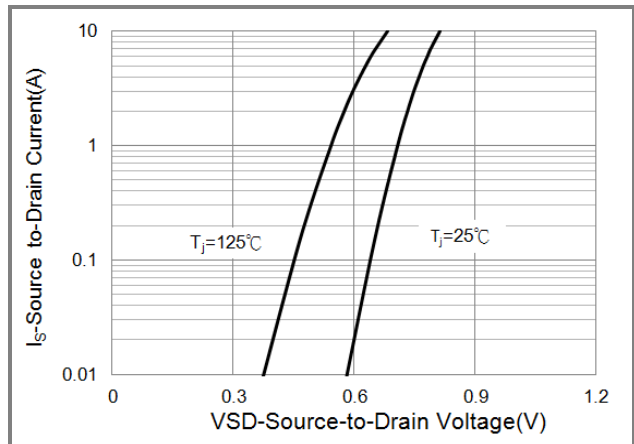


Fig.6 Source-Drain Diode Forward Voltage



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TYPICAL CHARACTERISTIC CURVES

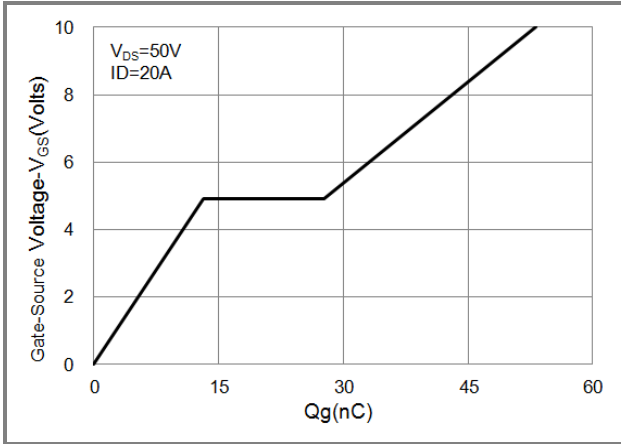


Fig.7 Gate-Charge Characteristics

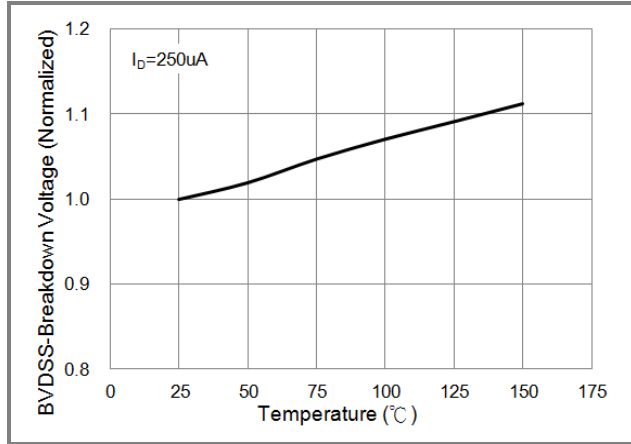


Fig.8 Breakdown Voltage Variation vs. Temperature

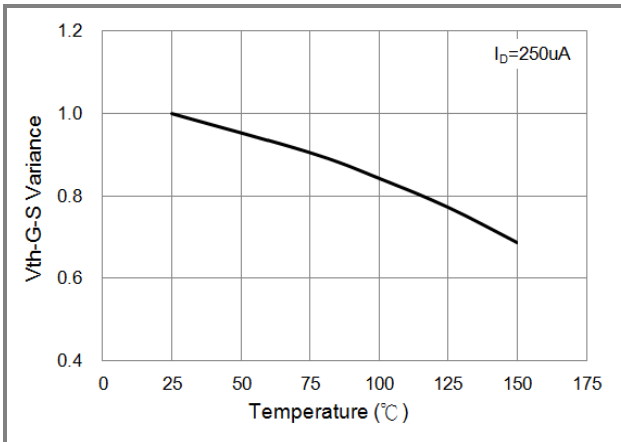


Fig.9 Threshold Voltage Variation with Temperature

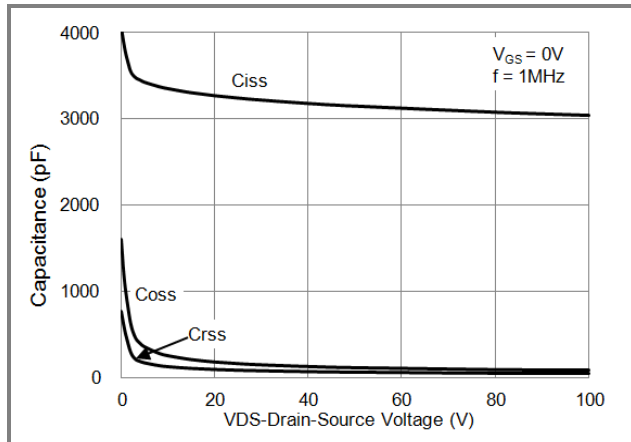


Fig.10 Capacitance vs. Drain-Source Voltage

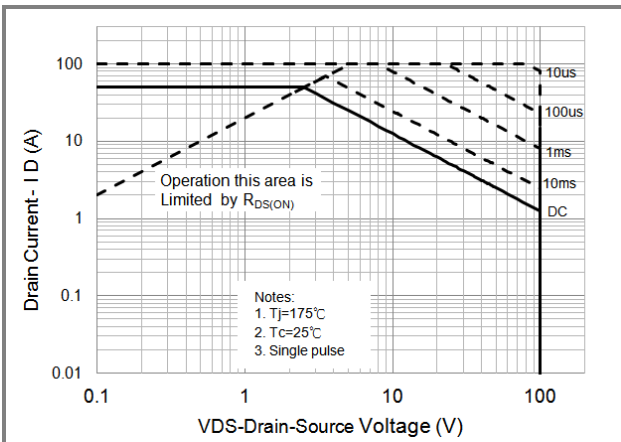


Fig.11 Maximum Safe Operating Area



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TYPICAL CHARACTERISTIC CURVES

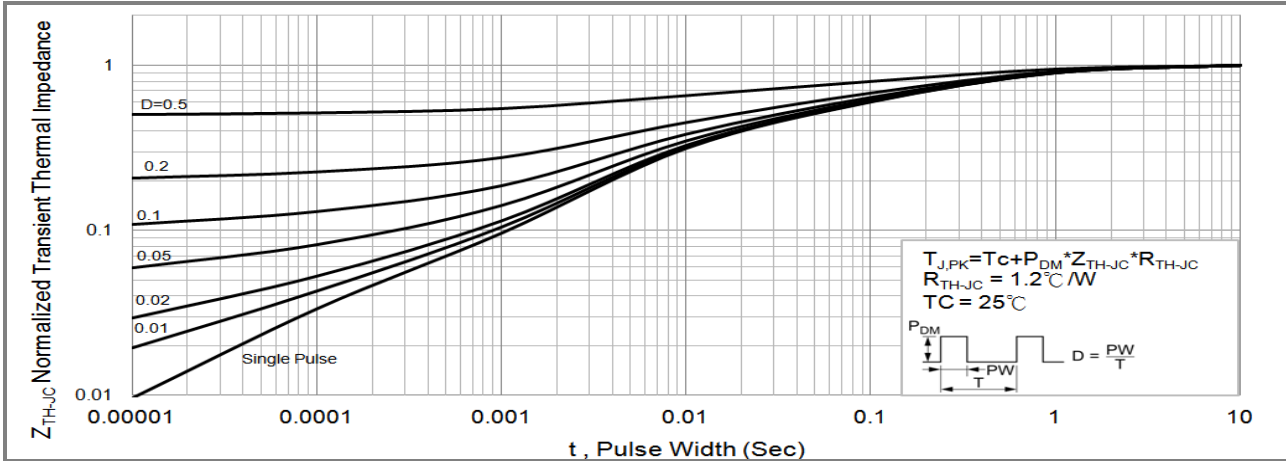
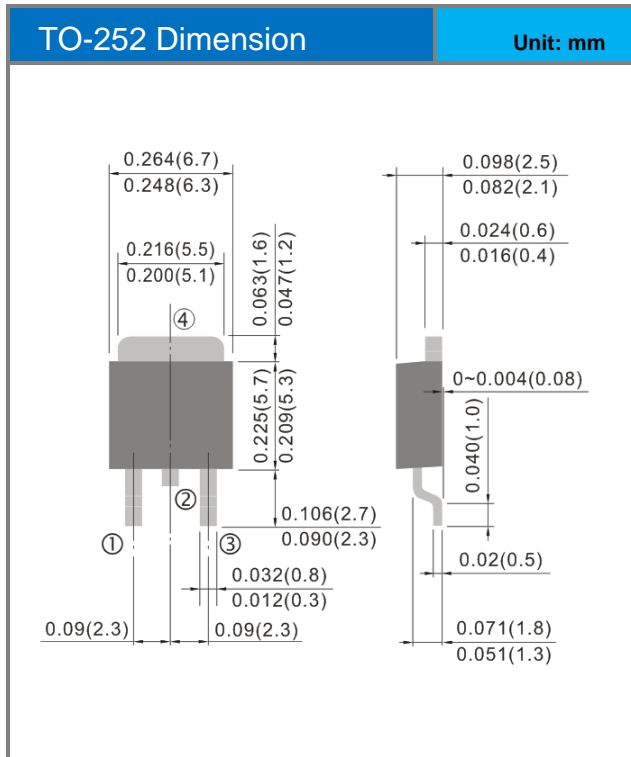


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width



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Packaging Information



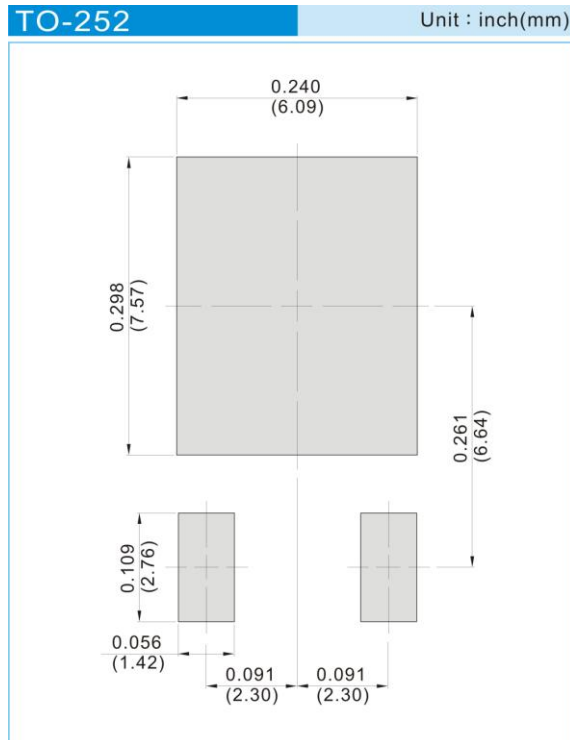


PJD50N10

PART NO PACKING CODE VERSION

| Part No Packing Code | Package Type | Packing type | Marking | Version |
|----------------------|--------------|---------------------|---------|--------------|
| PJD50N10_L2_00001 | TO-252 | 3,000pcs / 13" reel | D50N10 | Halogen free |

MOUNTING PAD LAYOUT





PJD50N10

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