

SPECIFICATION

Customer: _____
Model Name: SAT101CP40D36B1-50143L058KN
SPEC NO.: _____
Date: _____
Version: _____

Preliminary Specification
 Final Specification

Approved by	Comment

Prepared by	Reviewed by	Approved by

Record of Revision

Version	Revise Date	Page	Content
Pre-spec.A	2015/08/05		Initial Release

视安通集团 SAT GROUP

Contents

1. General Specifications.....	4
2. Pin Assignment	5
3. Operation Specifications	7
3.1. Absolute Maximum Rating	7
3.1.1. Typical Operation Conditions	8
3.1.2. Current Consumption	8
3.1.3. Backlight Driving Conditions	9
3.2. Power Sequence	10
3.3. Timing Characteristics.....	12
3.3.1.LVDS mode AC electrical characteristics	12
3.3.2.LVDS mode DC elec trical characteristics	14
3.4. Data Input Format	15
3.5. Parallel RGB Input Timing TABLE	16
3.6. Timing Diagram	16
4. Optical Specifications.....	17
5. Mechanical Drawing.....	18

1. General Specifications

No.	Item	Specification	Remark
1	LCD size	10.1 inch(Diagonal)	
2	Driver element	a-Si TFT active matrix	
3	Resolution	1024 × 3(RGB) × 600	
4	Display mode	Normally White, Transmissive	
5	Pixel pitch	0.2175(H) X 0.2088(V) X RGB mm	
6	Active area	222.72(H) X 125.28(V) mm	
7	Outline dimensions	235(H) X 143(V) X 5.0(D) mm	
8	Surface treatment	Anti-Glare	
9	Color arrangement	RGB-stripe	
10	Interface	LVDS	
11	Backlight Power consumption	TBD	
12	Panel Power consumption	TBD	
13	Weight	TBD	

2. Pin Assignment

No.	Symbol	I/O	Function
1	VCOM	P	Common voltage
2	VDD(3.3V)	P	Digital power
3	VDD(3.3V)	P	Digital power
4	NC	-	Not connect
5	REST(3.3V)	I	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high. (R=100K _Ω , C=1μF)
6	STBYB(3.3V)	I	Standby mode, normally pull high STBYB="1", normal operation STBYB="0", timing control, source driver will turn off, all output are high-Z
7	GND	P	Ground
8	RXIN0-	I	Negative LVDS differential data inputs
9	RXIN0+	I	Positive LVDS differential data inputs
10	GND	P	Ground
11	RXIN1-	I	Negative LVDS differential data inputs
12	RXIN1+	I	Positive LVDS differential data inputs
13	GND	P	Ground
14	RXIN2-	I	Negative LVDS differential data inputs
15	RXIN2+	I	Positive LVDS differential data inputs
16	GND	P	Ground
17	RXCLKIN-	I	Negative LVDS differential clock inputs
18	RXCLKIN+	I	Positive LVDS differential clock inputs
19	GND	P	Ground
20	RXIN3-	I	Negative LVDS differential data inputs
21	RXIN3+	I	Positive LVDS differential data inputs
22	GND	P	Ground
23	NC	-	Not connect
24	NC	-	Not connect
25	GND	P	Ground
26	NC	-	Not connect
27	NC	-	Not connect

28	SELB(3.3V)	I	6bit/8bit mode select H : 6bit / L : 8bit
29	AVDD	P	Power for Analog Circuit
30	GND	P	Ground
31	LED-	P	LED Cathode
32	LED-	P	LED Cathode
33	L/R(3.3V)	I	Horizontal inversion
34	U/D(3.3V)	I	Vertical inversion
35	VGL	P	Negative power for TFT
36	NC	-	Not connect
37	NC	-	Not connect
38	VGH	P	Positive power for TFT
39	LED+	P	LED Anode
40	LED+	P	LED Anode

I : input , O : output , P : Power

【Note】

- *1) : When L/R="0" , set right to left scan dirction
 When L/R="1" , set left to right scan dirction
 When U/D="0" , set top to bottom scan dirction
 When U/D="1" , set bottom to top scan dirction

I: input, O: output, P: Power

3. Operation Specifications

3.1. Absolute Maximum Ratings

(Note 1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power voltage	DV_{DD}	-0.3	5.0	V	
	AV_{DD}	-0.5	15	V	
	V_{GH}	-0.3	40.0	V	
	V_{GL}	-20.0	0.3	V	
	$V_{GH}-V_{GL}$	-	40.0	V	
Operation Temperature	T_{OP}	-20	70	°C	
Storage Temperature	T_{ST}	-30	80	°C	

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

3.1.1. Typical Operation Conditions

(Note 1)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	DV _{DD}	3.0	3.3	3.6	V	
	AV _{DD}	9.40	9.60	9.80	V	
	V _{GH}	17	18	19	V	
	V _{GL}	-6.6	-6.0	-5.4	V	
Input signal voltage	V _{COM}	3.8	4.0	4.2	V	

 Note 1: Be sure to apply DV_{DD} and V_{GL} to the LCD first, and then apply V_{GH}.

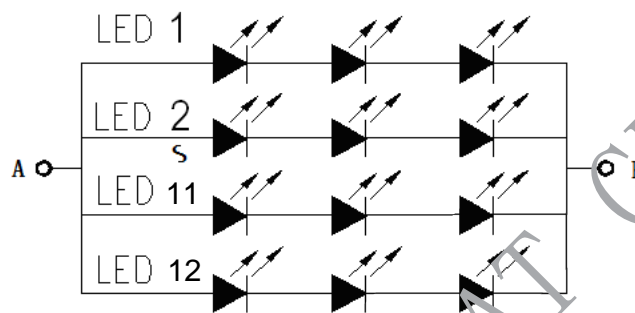
 Note 2: DV_{DD} setting should match the signals output voltage (refer to Note 3) of customer's system board.

3.1.2. Current Consumption

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current for Driver	I _{GH}	-	0.5	5.5	mA	V _{GH} =18V
	I _{GL}	-	4.8	9.8	mA	V _{GL} =-6.0V
	IDV _{DD}	-	17.9	22.9	mA	V _{DD} =3.3V
	I _{AV} _{DD}	-	29.1	34.1	mA	AV _{DD} =9.60V

3.1.3. Backlight Driving Conditions (36 White Chips)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage of white LED backlight	VL	8.7	9.6	10.5	V	Note 1
CurrentforLEDbacklight	IL	180	240	300	mA	
Luminance (on the module surface,BM-7)		230	280	-	Lux	
LED life time	-	50,000	-	-	Hr	Note 2



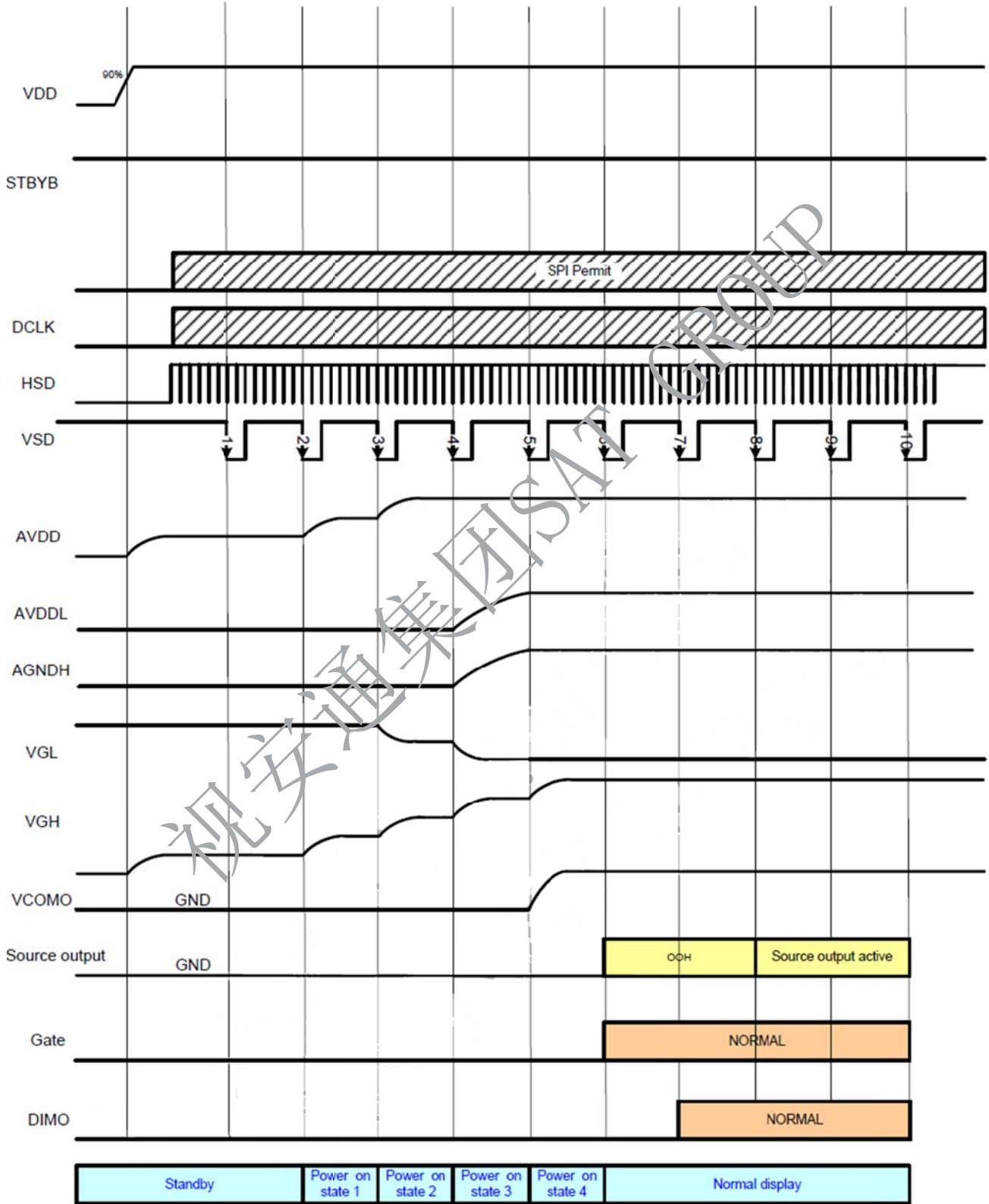
視安通集團SAT GROUP

3.2. Power Sequence

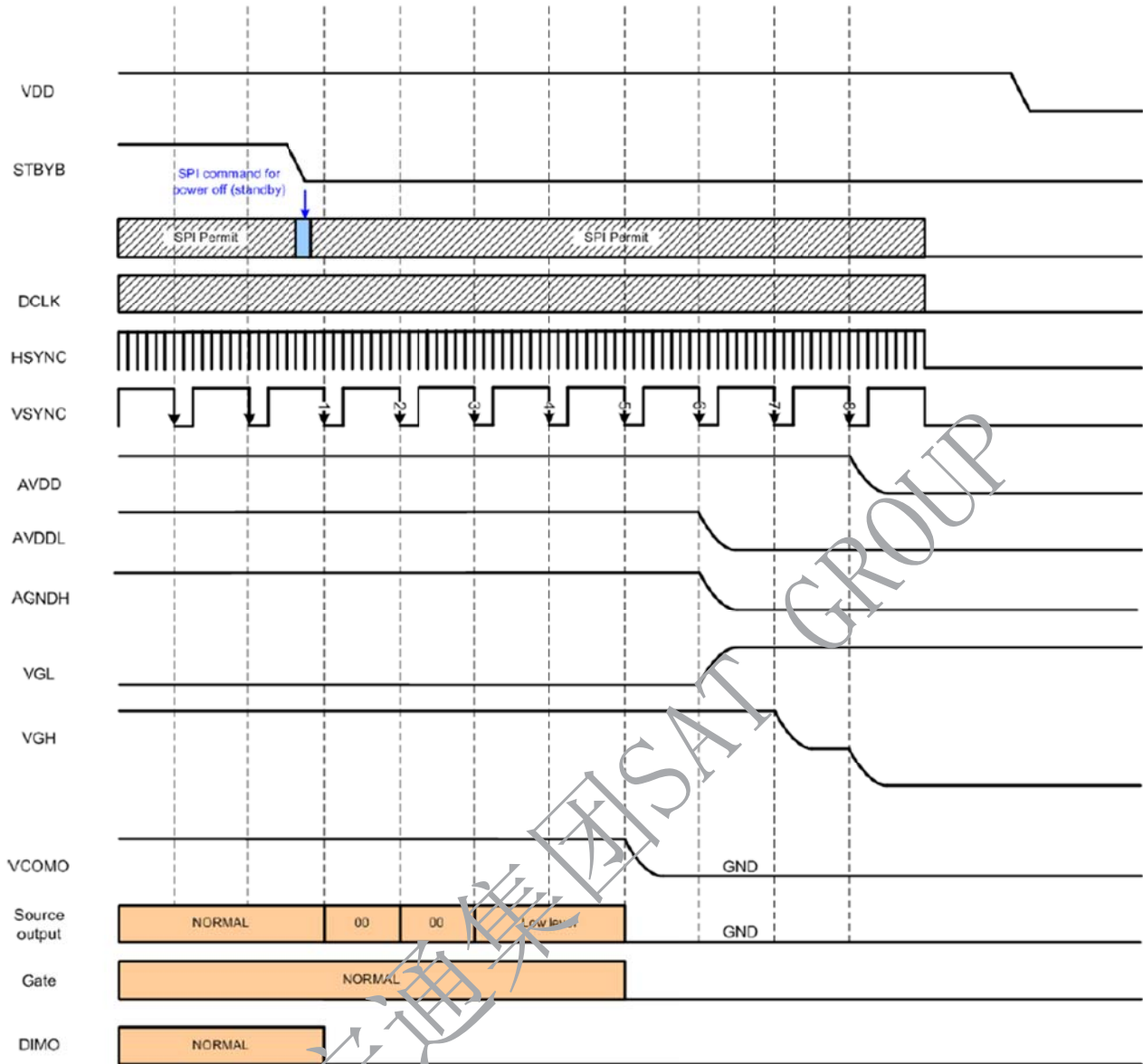
To prevent the device damage from latch up, the power on/off sequence shown below must be followed.

Power on: VDD, GND → AVDD, AGND → V1 to V14

Power off: V1 to V14 → AVDD, AGND → VDD, GND



Power on timing sequence



Power off timing sequence

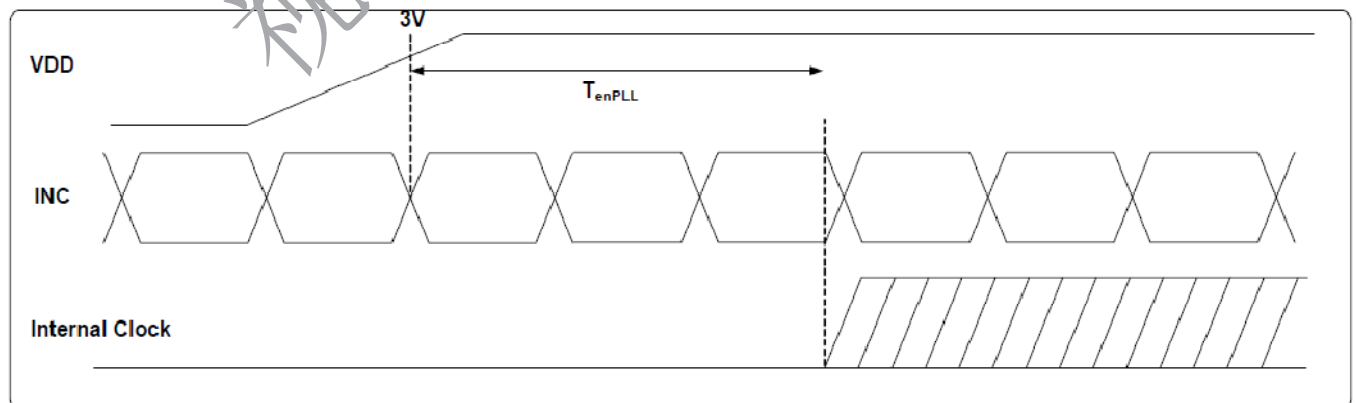
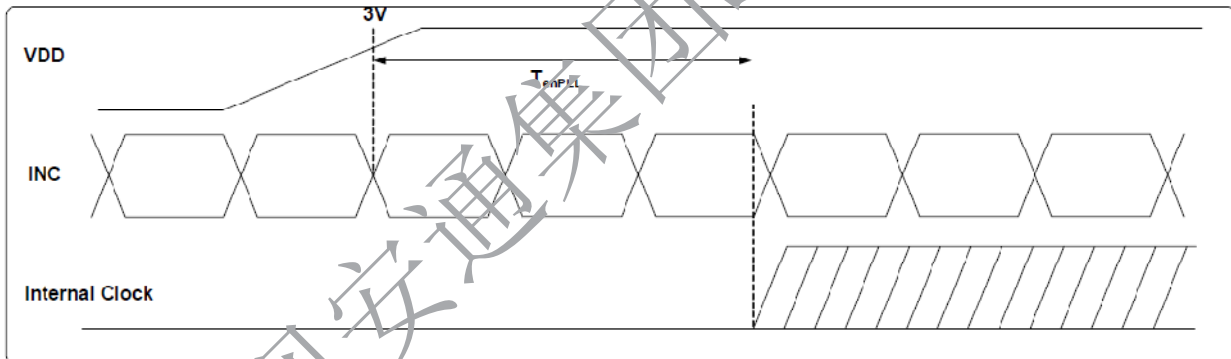
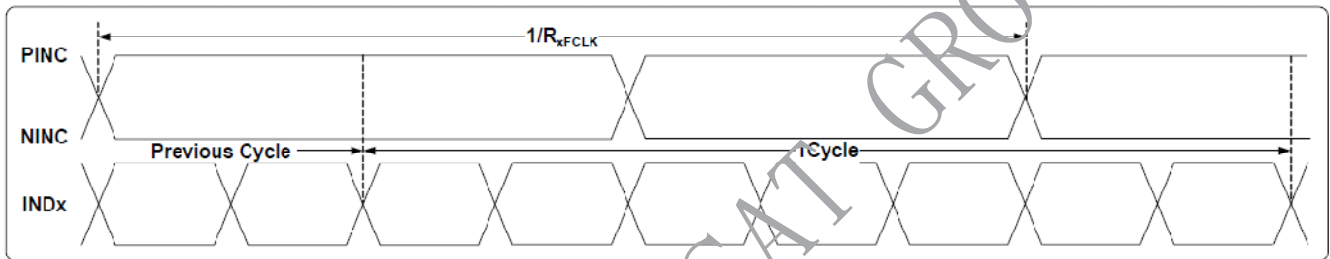
Note: Low level=3FH, when NBW=L (Normally white)

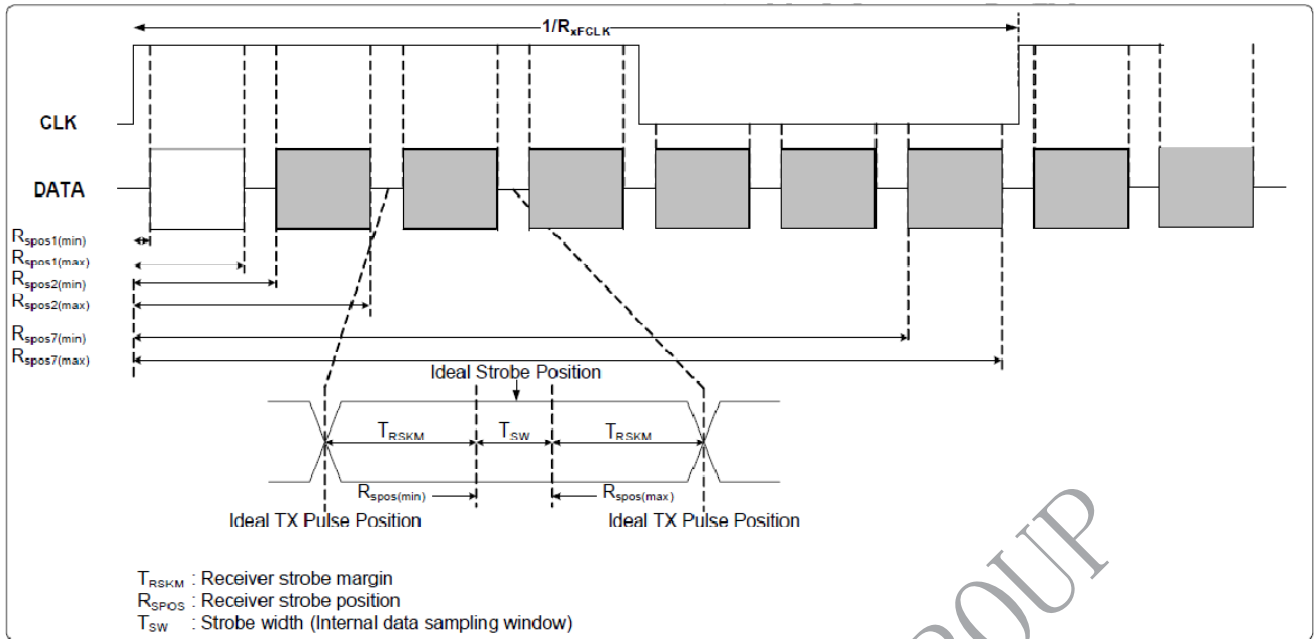
Low level=0CH, when NBW=H (Normally black)

3.3. Timing Characteristics

3.3. 1. LVDS mode AC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	RXFCLK	20	-	71	MHz	-
Input data skew margin	TRSKM	500	-	-	pS	VID =400mV RXVCM =1.2V RXFCLK =71MHz
Clock high time	TLVCH	-	$4/(7 * \text{RXFCLK})$	-	ns	-
Clock low time	TLVCL	-	$3/(7 * \text{RXFCLK})$	-	ns	-
PLL wake-up time	TemPLL	-	-	150	μs	-



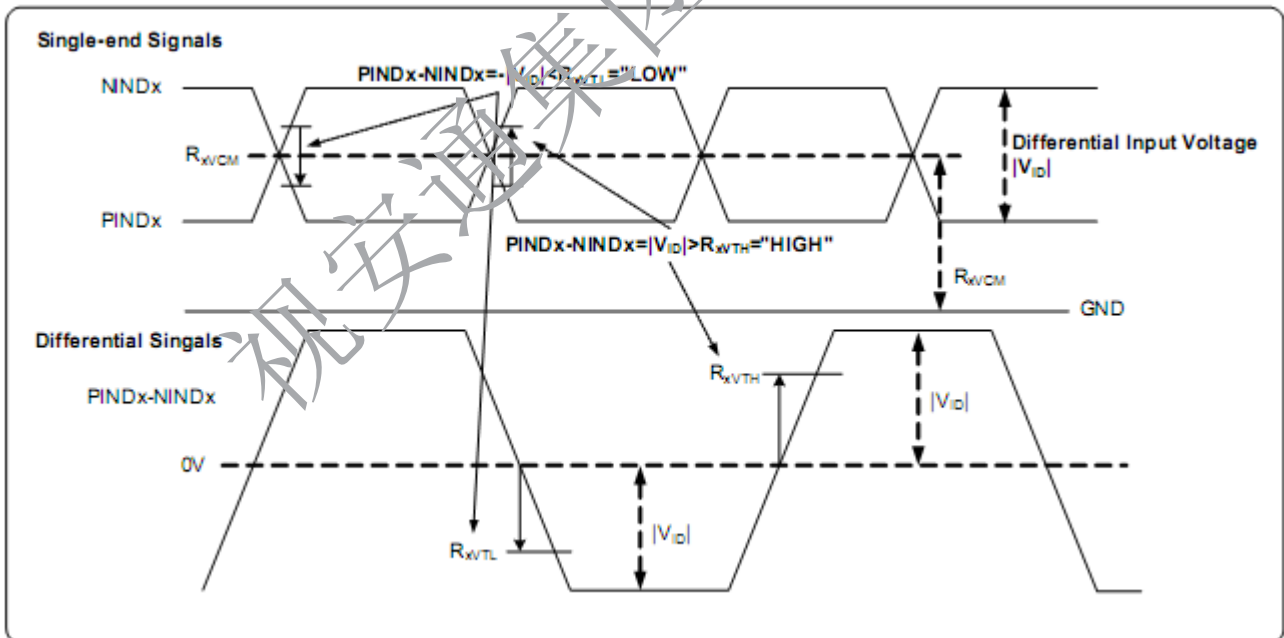


LVDS figure

視安通集團SAT GROUP

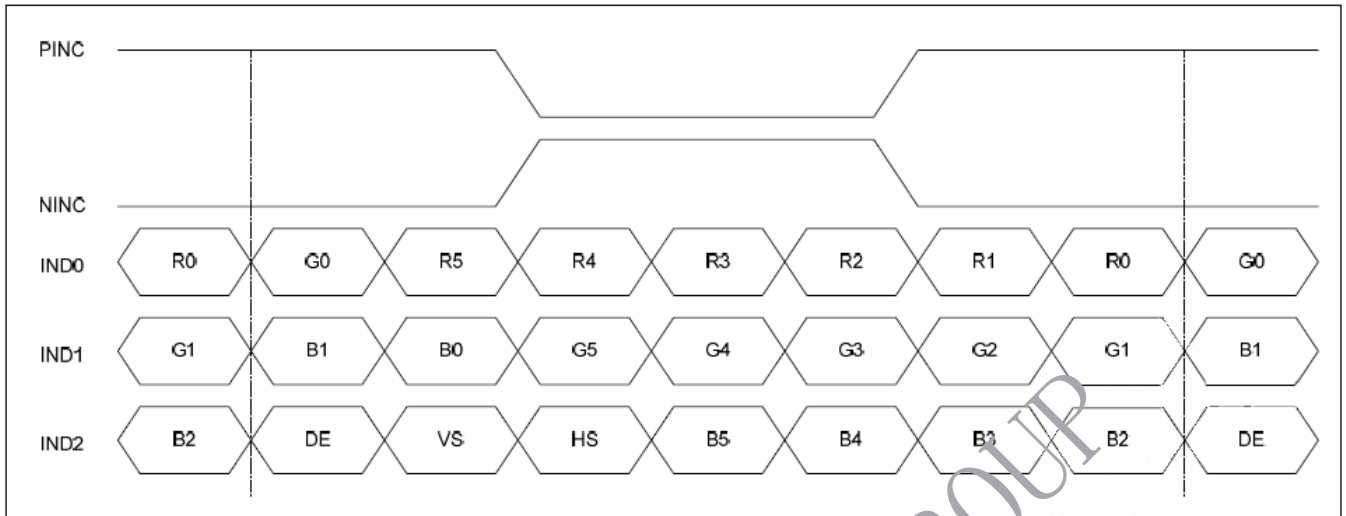
3.3.2.LVDS mode DC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Differential input high Threshold voltage	RXVTH	-	-	+0.1	V	RXVCM=1.2V
Differential input low threshold voltage	RXVTL	-0.1	-	-	V	
Input voltage range (singled-end)	RXVIN	0	-	VDD-1.2+ VID /2	V	-
Differential input common Mode voltage	RXVCM	VID /2	-	VDD-1.2	V	-
Differential input voltage	VID	0.2	-	0.6	V	-
Differential input leakage Current	RVLiz	-10	-	+10	μA	-
LVDS Digital Operating Current	Iddlvds	-	15	30	mA	Fclk=65MHz, VDD=3.3V
LVDS Digital Stand-by Current	Istlvds	-	10	50	μA	Clock & all Functions are stopped

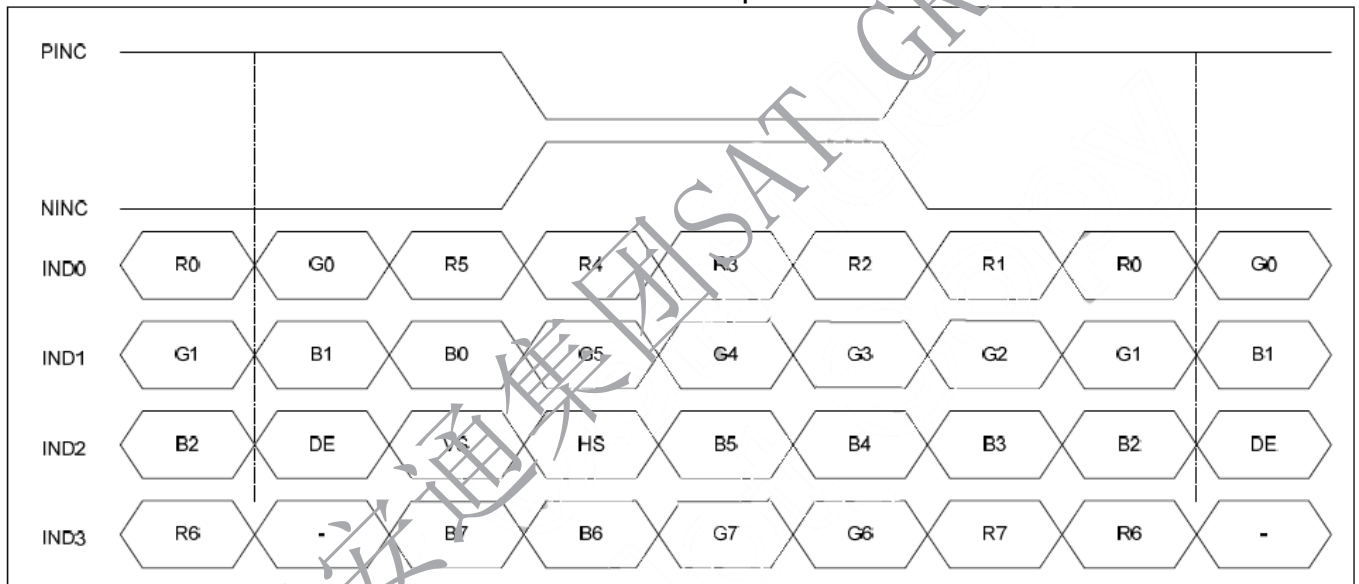


3.4. Data Input Format

3.4.1 LVDS mode data input format



6-bit LVDS input



8-bit LVDS Input

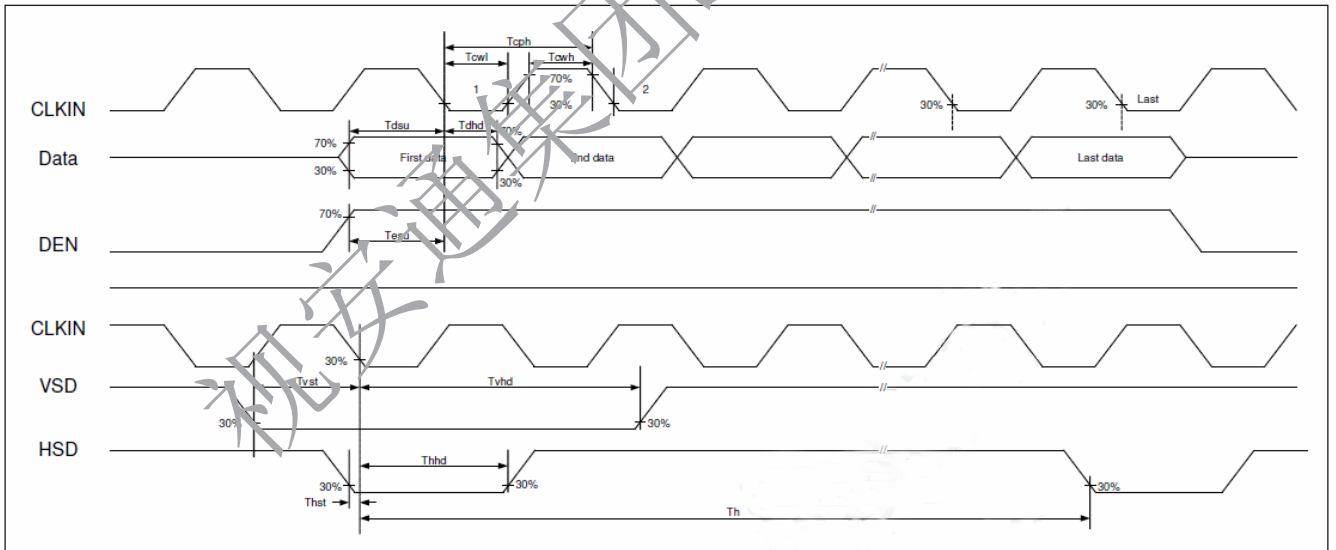
3.5. Parallel RGB Input Timing TABLE

3.5.1DE mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	40.8	51.2	67.2	MHz
Horizontal Display Area	thd	1024			DCLK
HSD Period	th	1114	1344	1400	DCLK
HSD Blanking	thb+ thfp	90	320	376	DCLK
Vertical Display Area	tvd	600			TH
VSD Period	tv	610	635	800	TH
VSD Blanking	tvbp+ tvfp	10	35	200	TH

3.6. Timing Diagram

3.6.1 Input Clock and Data Timing Diagram



4. Optical Specifications

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark	
View Angles	θT	$CR \geq 10$	60	70	--	Degree	Note1	
	θB		40	50	--			
	θL		60	70	--			
	θR		60	70	--			
Contrast Ratio	CR	$\theta=0^\circ$	500	600	--		Note4	
Response Time	$T_{ON} + T_{OFF}$	25°C	--	8	--	ms	Note3	
Chromaticity	White	Backlight is on	x	0.253	0.293	0.333		Note2 Note5 Note6
			y	0.295	0.335	0.375		
	Red		x	0.550	0.590	0.630		
			y	0.300	0.340	0.380		
	Green		x	0.301	0.341	0.381		
			y	0.554	0.594	0.634		
	Blue		x	0.117	0.157	0.197		
			y	0.075	0.115	0.155		
Uniformity	U		70	80	--	%	Note7	
NTSC			--	50	--	%		
Luminance	L		230	280	--	Lux	Note6	

Test Conditions:

1. $DV_{DD}=3.3V$, $I_b = 240mA$ (Backlight current),the ambient temperature is 25°C.
2. The test systems refer to Note 2.

5. Mechanical Drawing

